# Nonvolatile Analog Switch for Low-Voltage Applications 

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#### Abstract

In this paper, a nonvolatile switch based on n-type floating-gate transistors is described. The switch states are programmed through the memory cell floating-gate voltage, allowing higher levels than the application supply. Furthermore, due to its nonvolatile nature, the power consumption is reduced. The on-state resistance, which does not depend on the supply voltage, is one of the greatest advantages of this type of switch in comparison to conventional switches. This benefit can be successfully exploited in low-voltage applications. The switch on-resistance can be increased without the need for increasing the switch area. The characteristics of the proposed switch were confirmed by the experimental results obtained on a test chip fabricated in a $0.18 \mu \mathrm{~m}$ EEPROM process. Measured on-resistance values between 45 and $70 \Omega$ were obtained for a floating-gate voltage of 6.2 V and input source levels below 2 V . The required programming voltage was 18 V . The maximum off-state leakage current was measured at 5 nA .


Keywords: analog switch; floating-gate transistor; Fowler-Nordheim tunneling; low voltage

## 1. Introduction

Designing circuits that operate at low voltages is becoming a stringent requirement, as the number of portable electronic devices is continuously growing. This demand is also encouraged by process down scaling [1,2].

Analog switches represent basic circuits in analog signal processing. They are used in signal routing circuits [3,4], programmable gain amplifiers [5,6], reconfigurable filters [7], switching demodulators [8], sample and hold circuits [9-12], digital potentiometers [13], and many other circuits.

An analog switch can be implemented as an nMOS transistor, a pMOS transistor, or as a parallel combination of these two (CMOS switch or transfer gate). However, the most frequently used is the nMOS switch. A very important parameter of this switch is the on-resistance. Its value depends on technology, transistor aspect ratio, and overdrive voltage [14].

The nMOS switch gate voltage is limited to the supply voltage, and this causes strong degradation of its performances when used in low-voltage applications. The low-voltage handling solution is to increase the transistor gate voltage. Actual methods of this employ the boosting and bootstrapping techniques [9-12,15]. The boosting method involves the use of a charge pump to raise the gate voltage to a value proportional to the supply [9,15]. In the bootstrapping method, the voltage at the switch transistor gate is capacitively enhanced above the supply voltage so that it equals the sum of the input voltage and the supply voltage [10-12]. In both cases, the value of the gate voltage is dependent on the supply voltage.

In this paper, a method to increase the switching device gate voltage to a value independent of the system supply is developed. A floating-gate transistor (FGMOS) [16-18] is proposed as the switch. The on-resistance of the switch can be controlled through the floating-gate voltage, programmed using a memory cell. Thus, a nonvolatile switch is obtained, which implicitly has isolated terminals when programming. Furthermore, its floating gate does not draw current after it is programmed, reducing the switch's overall power consumption.

These nonvolatile switches are suitable for digital potentiometers supplied at voltages less than 2 V . In this situation, it is difficult to ensure both small on-resistance and a reasonable area with conventional switches. In addition, common requirements of digitally programmable potentiometers are the memorizing of the last wiper position and being able to restore it when powered up. Under these conditions, a conventional switch-based potentiometer would demand a dedicated memory block, while the proposed solution would not need it anymore. This configuration was implemented in a $0.18 \mu \mathrm{~m}$ EEPROM process using n-type floating-gate transistors. Its functionality was experimentally proven in this paper. The measurements confirm the nonvolatile switch simulations previously presented in [19].

## 2. Proposed Nonvolatile Switch Description

The proposed nonvolatile switch has the schematic presented in Figure 1. The switching device (NSW) is built in a deep n-well connected to terminal D_SW. The memory cell is formed by NL and NR transistors, both placed in a separate deep n-well. Thus, the isolation of the transistors from the p-substrate of the wafer is achieved. Furthermore, the bulks can be connected to the sources and biased with different voltages. Since the bulk-to-source voltage of the switching transistor (NSW) is zero, its on-state resistance is not affected by the body effect.


Figure 1. The nonvolatile switch schematic [19]. NL and NR are the memory cell transistors with SL, DL, SR and DR their corresponding source and drain terminals. NSW is the switch transistor and S_SW its source and D_SW its drain terminals, sharing its floating gate FGR with NR.

All devices in the proposed schematic (Figure 1) are high-voltage n-type FGMOS transistors.

Floating-gate transistors are MOS transistors that have two polysilicon gates (a control and a floating gate). Because the floating gate is surrounded by dielectric oxides, it is completely isolated from the rest of the device and can store charges [16-18].

NR and NSW transistors share a common floating gate (FGR), which enables the switch transistor programming to be performed by the NR transistor. The purpose of the NL transistor is to provide a means for differentially reading the memory cell [20,21].

NSW transistor channel conductivity is controlled only by the floating gate potential, as the control gate is grounded (Figure 1).

In order to remove the electrons from the FGR (Figure 2a), a positive high-voltage programming pulse (+VPP) is applied to the NR transistor source (SR), while its control gate (SL) is kept to ground. In this way, the FGR potential becomes positive, causing the
switch transistor to turn on and allow the current to flow between its drain and source. This is called the on-programming procedure.


Figure 2. NSW (a) on- and (b) off- programming conditions. +VPP, positive high-voltage programming pulse. GND, ground.

To charge the floating gate with electrons (Figure 2b), the positive high-programming voltage is now applied on the NR transistor control gate (SL), while its source (SR) is kept to ground ( $0 \mathrm{~V}, \mathrm{GND}$ ). By negatively charging the FGR, NSW becomes nonconductive (turned off). This is called the off-programming procedure.

Both on- and off- programming are ensured through Fowler-Nordheim tunneling, a mechanism that involves the tunneling of electrons through a surface barrier due to the application of an intense external electric field across a thin oxide [17].

In both cases, the NL and NR drains are left floating, and their deep n-well (DNW) is biased with +VPP in order to ensure that parasitic diodes are kept reverse biased [19].

Table 1 summarizes both the on- and off- programming conditions.
Table 1. Programming conditions. DNW, deep n-well.

| Target Switch State | DL | SL | DNW | DR | SR |
| :---: | :---: | :---: | :---: | :---: | :---: |
| ON | floating | GND | VPP | floating | VPP |
| OFF | floating | VPP | VPP | floating | GND |

The value of the FGR voltage depends on the value of the voltage programming pulse (VPP) and not on the system supply voltage, as is the case for conventional switches or switches where boosting [9,15] and bootstrapping [10-12] methods are used.

In order to activate the tunneling of the electrons and to control the floating gate of the switch, a minimum value for VPP is required, usually greater than 10 V [22]. Thus, when the switch is embedded within a low-voltage system a charge pump is needed for VPP generation [23]. Ultimately, the charge pump is the one that establishes the minimum supply voltage requirements. It is also responsible for the power consumption of the switch, but this happens only during the programming procedure. Once programmed in a particular state, the nonvolatile switch does not consume power (zero quiescent current).

## 3. Experimental Results and Discussion

The described switch configuration (Figure 1) was included in a test chip produced in a $0.18 \mu \mathrm{~m}$ EEPROM process. Figure 3 presents a small portion of the test chip layout. Within this test chip, the switch occupied a total area of about $2400 \mu \mathrm{~m}^{2}$.


Figure 3. Test chip layout with included nonvolatile switch structure and associated pads.
Figure 4 illustrates the measurement setup used for testing the functionality of the nonvolatile switch on the wafer. It included a micromanipulator for placing the four available needle probes onto the desired pads, a semiconductor parameter analyzer (HP4145B) responsible for biasing and measurements, and a PC for data processing.


Figure 4. Measurement setup.
Two configurations (Figure 4A,B) were employed during the measurements. In configuration A, the four needle probes were connected on the SL, SR, DNW, and GND pads to enable the programming procedure. In configuration $B$, three needle probes were connected on the S_SW, D_SW, and GND pads in order to determine the effects of programming on the switch state. The measurement method followed the steps indicated in the diagram shown in Figure 5.


Figure 5. Diagram of the measurement steps.
First, the inherent state of the nonvolatile switch was determined to be off by measuring a current in the order of nA through the NSW transistor.

Then, in order to program the nonvolatile switch in the on state, a step voltage varying from 0 V to a variable high voltage level (VPP between 16 and 20 V ) was set for the SL pad. The same VPP was applied to the DNW pad, while SR was grounded. For each case, the responsiveness of the FGR potential was assessed using the setup in Figure 6. The V_sw source was varied between 0 and 7 V , while $\mathrm{V}_{\mathrm{D}}$ Sw was kept constant at 7 V .


Figure 6. Switch drain current test setup.
Figure 7 depicts the NSW drain current variation with the voltage applied on its source (S_SW) for different VPPs. Note that the maximum switch current value was limited
to $10 \mu \mathrm{~A}$, since the aim of this measurement was only to identify how the programming voltage influences the floating-gate potential.


Figure 7. Switch drain current versus source voltage for different voltage programming pulse (VPP) values.

NSW behaves like a standard nMOS transistor, having its gate biased with the floatinggate potential. As $V_{S_{-}}$SW rises the overdrive voltage of NSW decreases until its channel is cut off (and the drain current sharply decreases to zero).

The increase in VPP causes the floating-gate potential to increase, so the cut off occurs at a higher $\mathrm{V}_{\mathrm{S}}$ SW. Even though there is the same 1 V difference between the VPP values corresponding to each two consecutive curves, we can observe from Figure 7 that the tunneling effect starts to saturate with the VPP increase. Thus, there is a limit value for the VPP voltage from which the transistor channel conductivity cannot be further increased.

In order to measure the on-state resistance of the nonvolatile switch, a constant current (I) was sourced into the drain of the NSW transistor, while its source was connected to a variable voltage source from 0 to 7 V . Figure 8 illustrates the switch on-resistance test setup. The on-state resistance measurement was made after the switch was programmed using $\mathrm{VPP}=18 \mathrm{~V}$.


Figure 8. Switch on-resistance test setup.

In this configuration, the drain voltage was measured, and the on-resistance was determined using the following equation:

$$
\begin{equation*}
\mathrm{R}_{\mathrm{ON}}=\left(\mathrm{V}_{\mathrm{D} \_\mathrm{SW}}-\mathrm{V}_{\mathrm{S} \_\mathrm{SW}}\right) / \mathrm{I} \tag{1}
\end{equation*}
$$

Different values were used for the current I, but for small currents, we observed that measurements were strongly affected by the precision of the HP4145B semiconductor parameter analyzer. Thus, in order to minimize the errors introduced by this instrument, a value of 1 mA was chosen for the current sourced to the drain, also taking into consideration a safe power dissipation.

Unfortunately, because of the small-sized pads in the test chip, the four-point resistance measurement method could not be employed, so the measured resistance value was subject to both contact and wire resistance influence.

The on-resistance of the switch varies with the overdrive voltage variation. Because the sourced current through the drain is constant, the $\mathrm{R}_{\mathrm{ON}}$ variation also causes the drain voltage to change. For $\mathrm{V}_{\mathrm{DS}}$ SW values below 0.1 V , the $\mathrm{R}_{\mathrm{ON}}$ is situated between 45 and 100 $\Omega$, as shown in Figure 9. As expected, the relationship between the on-resistance and the switch drain-to-source voltage is linear.


Figure 9. On-resistance measured variation for drain-to-source voltages smaller than 0.1 V .
Figure 10 shows NSW on-resistance variation with $\mathrm{V}_{\text {S_SW }}$. At high overdrive voltages, the on-resistance has low values, varying from 45 to $70 \Omega$ for $V_{\text {S_sw }}$ under 2 V (see inset of Figure 10). This small variation makes this switch ideal for low-voltage applications. A "knee" shape can be observed in Figure 10 when $\mathrm{V}_{\mathrm{S} \text { _SW }}$ is around 3 V. This effect was observed on all measured structures. After the source voltage reaches 5 V , the onresistance abruptly increases in response to the fact that the transistor starts to turn off $\left(\mathrm{V}_{\mathrm{FGR}}-\mathrm{V}_{\mathrm{S}_{-} \mathrm{SW}} \leq \mathrm{V}_{\mathrm{T}}\right)$.


Figure 10. Measured on-resistance variation with the input voltage.
Simulations were also performed on the nonvolatile switch considering multiple values for the floating-gate voltage in order to estimate the real FGR value at VPP $=18 \mathrm{~V}$. The simulated results are plotted in Figure 11, together with the measured characteristics presented in Figure 10. Matching was sought in the portion of the curves where $\mathrm{R}_{\mathrm{ON}}$ exhibited an abrupt increase, corresponding to the transition between on and off states. Thus, the real value for the FGR potential was estimated at around 6.2 V . The measured on-resistance variation is larger than its simulated counterpart for a $\mathrm{V}_{\mathrm{S}}$ SW lower than 5 V .


Figure 11. On-resistance variation with the input voltage. The red curve corresponds to the measured on-resistance, while the rest of the curves correspond to simulated results obtained for multiple $\mathrm{V}_{\mathrm{FGR}}$ values.

For instance, in a 4 V application, the proposed nonvolatile switch has a maximum on-resistance of $300 \Omega$ regardless of input voltage (Figures 10 and 11). An identically sized conventional nMOS, however, has an $R_{\mathrm{ON}}$ in excess of $1 \mathrm{k} \Omega$ once the input voltage exceeds 2.7 V . Therefore, for the same on-resistance performances, the area consumed by the nonvolatile switches is lower if the floating-gate voltage is larger than the gate command of the conventional switches. Moreover, the proposed switch performances may be improved through the programming tunneling voltage without increasing the required area, unless the programming limit mentioned before is reached.

However, the EEPROM technology required by the nonvolatile switch needs additional process steps compared to CMOS processes, where conventional switches are usually built in. Therefore, a final estimation about the cost depends on both the switch area and the technology expenses.

NSW was switched off by programming. Thus, a voltage step of 0 to 18 V was applied to the SL pad. SR was grounded while the DNW pad was connected to 18 V . The current measured through NSW after applying this programming sequence on NR was of max. 5 nA , confirming the switch's off state.

The functionality for the nonvolatile switch was also proven by simulations for both on and off states [19].

Additionally, simulations were also carried out in order to determine the bandwidth of the NSW transistor. A 10 mV AC generator was applied to the source, while its drain was connected to a load impedance consisting of a $50 \Omega$ resistor in parallel with a 5 pF capacitor. The cut-off frequency was determined to be around 4 GHz .

## 4. Conclusions

In this paper, a nonvolatile switch for low-voltage applications was proposed, comprising common FGMOS transistors, used as the effective switch and a memory cell, respectively. The switch states are programmed through the memory cell floating-gate voltage. Thus, the FGR level can be higher than the application supply in order to optimize the on-resistance of the switch. Furthermore, due to its nonvolatile nature, the power consumption is reduced.

The switch performance was proven by experimental measurements made on a test chip fabricated in a $0.18 \mu \mathrm{~m}$ EEPROM process.

The measured on-state resistance had a small variation (from 45 to $70 \Omega$ ) for a floatinggate voltage of 6.2 V and input source levels below 2 V . It remained reasonably small ( $<300 \Omega$ ) until input voltages of 4.3 V . Moreover, there was no need for increasing the switch area in order to obtain smaller on-resistances. The FGR value was obtained using a programming of 18 V , representing a significant amount in low-voltage systems, where the conventional nMOS transistor gate potential is limited by the power supply.

In the off state, the maximum leakage current was measured at 5 nA .
The small on-resistance variation, reduced power consumption, and nonvolatility indicate the potential of the proposed switch for low-voltage potentiometer applications such as hearing aids.

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