



## Review

# Design Topologies of a CMOS Charge Pump Circuit for Low Power Applications

Labonnah Farzana Rahman <sup>1,\*</sup> , Mohammad Marufuzzaman <sup>2</sup> , Lubna Alam <sup>1,\*</sup> and Mazlin Bin Mokhtar <sup>1</sup><sup>1</sup> Institute for Environment and Development, Universiti Kebangsaan Malaysia, 43600 Bangi, Malaysia; mazlin@ukm.edu.my<sup>2</sup> Institute of Energy Infrastructure, Universiti Tenaga Nasional, 43000 Selangor, Malaysia; marufsust@gmail.com

\* Correspondence: labonnah.deep@gmail.com (L.F.R.); lubna@ukm.edu.my (L.A.)

**Abstract:** Applications such as non-volatile memories (NVM), radio frequency identification (RFID), high voltage generators, switched capacitor circuits, operational amplifiers, voltage regulators, and DC–DC converters employ charge pump (CP) circuits as they can generate a higher output voltage from the very low supply voltage. Besides, continuous power supply reduction, low implementation cost, and high efficiency can be managed using CP circuits in low-power applications in the complementary metal-oxide-semiconductor (CMOS) process. This study aims to figure out the most widely used CP design topologies for embedded systems on the chip (SoC). Design methods have evolved from diode-connected structures to dynamic clock voltage scaling charge pumps have been discussed in this research. Based on the different architecture, operating principles and optimization techniques with their advantages and disadvantages have compared with the final output. Researchers mainly focused on designing the charge pump topologies based on input/output voltage, pumping efficiency, power dissipation, charge transfer capability, design complexity, pumping capacitor, clock frequencies with a minimum load balance, etc. Finally, this review study summarizes with the discussion on the outline of appropriate schemes and recommendations to future researchers in selecting the most suitable CP design methods for low power applications.

**Keywords:** charge pump; topologies; CMOS; high voltage; low power



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## 1. Introduction

In radio frequency identification (RFID) systems, a reader, tag and antenna are the main elements to track or identify any product information using radio-waves. RFID is a technology, which requires radio waves to track or identify any tagged object. By using the tag to any product or object allows users to track that item automatically, uniquely to track any inventory system. RFID uses readers to read the tag information attached to any entity, human, animals, fishes, products, etc. As a result, RFID-based systems are widely implemented in commercial and industrial applications for tracking product information and the supply chain management system [1–3].

A tag is typically a small chip subdivided into three main blocks: analog, logic, and memory blocks, where tag memory holds the product information data. Depending on application features, tag memory can be a read-only memory (ROM), random access memory (RAM) or electrically erasable programmable read-only memory (EEPROM), or flash memory and data buffers [4–6]. As the tag is a tiny chip, so it requires an internal power supply generator, which produces higher voltage than the power supply voltage [2,6,7]. Therefore, charge pump (CP) circuits are necessary for low power designs to generate the higher output voltage from a small supply voltage (VDD) in a memory chip [7–9]. Sometimes CP circuits are used as voltage doublers to generate the bias voltages in both analog and digital devices [10–12].

On the other hand, the charge transfer process in and out by the charge transfer capacitors is affected by transistor switches, which operated from few kilohertz to megahertz range. In non-volatile memories (NVM)-based applications, the CP circuit needed to produce higher output voltage for erasing and programming operations [13,14]. In this type of application, the higher voltage generated by the CP circuit requires voltage regulation. However, most of the research found in recent years mainly focuses on bias voltage generation function rather than a regulated voltage supply. Consequently, they deal with driving heavy loads instead of gates. In 1976, Dickson (1976) first proposed the integrated CP circuit with a static behavior model, which was again modified and further developed as a MOS diode by Witters et al. (1989), where the CP circuits dynamic behavior was described [15–20]. Previous research has been discussed with reducing power dissipation and proposed in a general way; still, there was no such literature to minimize the power dissipation, especially memory applications [21–24]. Therefore, a typical scheme to design the CP circuit with reduced power dissipation was independent of any specific topological implementation presented by Palumbo et al. (2002). To define the output voltage, the numbers of stages are related and the following equation defines this relation:

$$V_{out} = N \times V_{\phi} + V_{in} - (N + 1) \times V_t, \quad (1)$$

where  $V_{\phi}$  is the clock amplitude,  $N$  is the number of stages,  $V_{in}$  is the input supply voltage,  $V_t$  is the threshold voltage [25]. The performance of the charge pump circuit degrades due to the body bias effect of higher pumping stages. The threshold voltage value is also increased more than two because of the higher source to bulk voltage. Moreover, some parameters such as parasitic capacitance also hold some charge and improve the CP circuit's internal impedance [26]. The output drive current  $I_{out}$  can be calculated using the following equation:

$$I_{out} = C_{Load} \times \frac{V_{out}}{T_{ramp-up}}, \quad (2)$$

where  $C_{Load}$  is the load capacitance,  $V_{out}$  is the output voltage of the charge pump and  $T_{ramp-up}$  is the time required by the charge pump to reach the output voltage [26]. On the other hand, power dissipation in CP circuit is another rising demand for low power applications. Whenever the voltage step value is amplified, the efficiency decreases, which is a substantial part of the circuits. The following equation gives the power consumption in the charge pump circuit,

$$P_D = C \times V_{DD}^2 \times F_{clk}, \quad (3)$$

where  $P_D$  is the power dissipation,  $C$  is capacitor size and the clock frequency is  $F_{clk}$ . From the equation, it is clear that a significant size capacitor and frequency can increase the output voltage but, at the same time, can increase the overall power dissipation of the CP circuit. Therefore, there is a significant trade-off between the performance and the CP circuit's power dissipation [26].

Nevertheless, research-based on minimizing the power consumption by any CP circuit firmly focused on simple and basic design schemes. Researchers never mentioned low voltage strategies and topologies for low power applications. As a result, the generation of higher voltage from the lower power supply voltage has been an expedition to discover energy. Initially, engineers came up with the idea of transformers that can up and down-convert the supply voltage. The auxiliary circuits to the CP can help progress the performance [27]. On the other hand, information or data is characterized by charge, trapped in an insulator, or inserted into the floating gate transistors through a tunnel controlled by this F-N mechanism [26].

This article will give a brief illustration of the CP circuit topologies design considerations. Moreover, the most widely used CP design topologies have been discussed, along with design specification and performance analysis. Finally, a summary table was plotted, illustrating the advantages and disadvantages of the CP design topologies that have intervened in the last decade with their performance comparison. Hence, this review

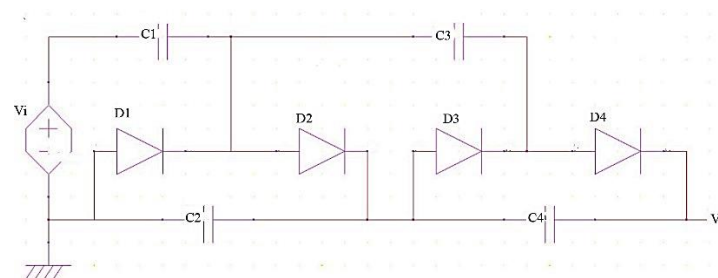
article will discuss recent CP research trends, challenges and recommendations for future researchers to find suitable CP design topology for any specific design criteria, especially for low power applications.

## 2. Topologies for CP Circuits

In the last decade, CP design topologies have been analyzed with different design and process schemes. In this literature, some of the principal structures of CP circuits have been presented, based on the basic design methods of Dickson and Cockcroft and Walton's CP circuit. The increment in power supply voltage can achieve by voltage multiplication and integrating an additional one diode-capacitor voltage stage in series. In this study, different topologies, which have evolved in the last couple of years, have been discussed based on their applicability in other applications with the comparative analysis. Thus, different design schemes are classified as compatibility in-memory application, DC–DC converters and energy harvesting purposes.

### 2.1. Basic CP Circuits

Cockcroft and Walton (1932), at the Cavendish Laboratory in Cambridge, England, needed higher particle energies to accelerate sub-atomic particles along a straight discharge tube. A voltage multiplier circuit designed using a stack of capacitors connected to diodes acting as switches. By asserting and de-asserting the switches in proper sequence, they built up a potential of 800 kV [28]. This voltage multiplier circuit was far lighter and cheaper than transformers. Cockcroft and Walton designed a voltage multiplier, which converted low AC power or DC pulses to a higher DC voltage level as shown in Figure 1. In this design, capacitors were connected in series, where diodes were employed to produce high voltage.

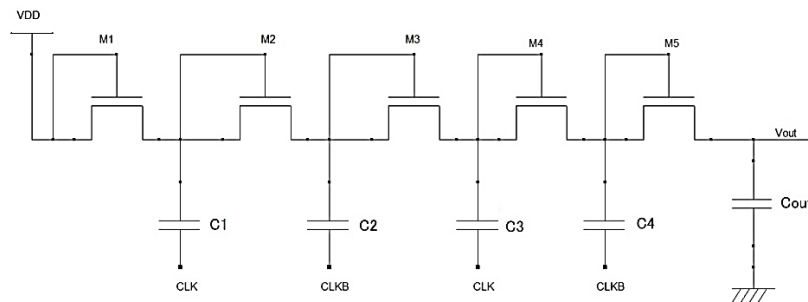


**Figure 1.** Schematic diagram of Cockcroft–Walton voltage multiplier [28].

Moreover, this scheme eliminated the heavy core as transformers did. In this method, the bulk of insulation/potting is required. A higher voltage was achieved from a low supply voltage using these capacitors and diodes as a multiplier. It had the advantage of low-cost materials requirement with an easy setup method [29]. However, this scheme suffered from some drawbacks; if the number of stages increased, then the higher stage's voltage started to "sag" due to capacitors' electrical impedance and the small number of steps. Moreover, when the output current is injected, a large voltage ripple is produced to increment the stages.

Dickson (1976) used the same concept as the Cockcroft–Walton voltage multiplication circuit and implemented it in IC's. It was very similar to the CP voltage multiplier, where the diode-connected chains are coupled to the input through several capacitors connected in parallel. Therefore, all the capacitors needed to withstand storing the full voltages produced by these chains. The system could achieve efficient multiplication by involving many capacitors. However, involving many capacitors in the circuitry increased the power dissipation and decreased pumping efficiency [16]. The primary Dickson CP circuit was very robust with different high voltage generation issues until sub-micron design technology. When the diode-connected MOSFET was turned on in the Dickson CP circuit, the threshold voltage was the voltage difference between the drain and source terminal of

the diode-connected MOSFET. The conventional Dickson CP circuit structure had a low pumping capacity due to the large threshold voltage and the body-effect in each stage to generate the high voltages as shown in Figure 2. Additionally, all the steps suffered from a high-voltage overstress and a voltage difference, which was  $2 \times V_{DD}$  in each node caused by each node's gate oxides. Consequently, when the number of pumping stages increases, the body effect degrades the Dickson CP circuit's pumping efficiency.



**Figure 2.** Dickson charge pump (CP) circuit with diode-capacitor [16].

Dickson CP circuit could not generate the desired output voltage as it was suffering from the body effect on the diode-connected MOSFETs. Therefore, Witters et al. (1989) proposed a new mechanism for designing a triple-well process CP [17]. In complementary metal-oxide-semiconductor (CMOS) circuit design, voltage multiplier circuits used a transistor, which performed as diodes. However, threshold voltage arises to the transistor in this circuit's chain due to the body effect problem the performance affected slightly. The output voltage level could not meet the requirements compared to a diode configuration, which eventually reduced the circuit's internal resistance. This difference between these methods got worse when any circuit implementation required more stages. Any multiplier or boosting circuit's output voltage was limited, regardless of the necessary number of steps.

Moreover, the substrate current produced in the floating-well technique affects other circuits in the same chip. Therefore, this scheme for multiplying circuit was proposed and verified for implementation. Nevertheless, this technique predicted the characteristics of a wide variety of voltage multipliers.

Atsumi et al. (1994) designed a striking and widely-implemented CP circuit named bootstrap CP. In this scheme, a simple MOS transistor or transmission gate have utilized as a switching terminal to generate higher voltage than the power supply voltage. Therefore, the MOS transistor has to switch on with a suitable supply voltage to the gate terminal, higher than the source terminal voltage. These required high gate voltages were attained from each stage to another capacitor and MOS transistor, forming the bootstrap circuit. Though the circuit generated higher output voltage, it is also clear from the complex circuit structure that it required higher implementation cost for a more complex clocking scheme and control section, which has four phases and double amplitude of the supply voltage [30,31].

## 2.2. CP for Memory Application

Lauterbach et al. (2000) illustrated a novel idea of power saving in boosted CP circuits, which doubles the power efficiency by integrating two-step adiabatic switching, charge sharing, and a simplified clocking arrangement. As this scheme shares the charges, so clock driver strengths declined. Therefore, the maximum value of the charging current dropped by a factor of three. On the other hand, combining the tri-state drivers and the clocking circuits removed the parasitic charge current peaks. As a result, the electromagnetic emission of the CP circuit condensed considerably. However, the charge-sharing concept necessitates this external clock generator to pump the voltage, ultimately increasing power dissipation [24].

Lai and Wang (2001) proposed a CP circuit where source-bulk-connected techniques were utilized with two associated courses, which solved the limitation of charge sharing methods. These circuits are involved in the primary CP circuit to reduce the body effect while avoiding the forward-biased PN junction. The body of each charge transfer transistor in the primary pumping circuit is connected to the body bias circuit. When pumping begins, the CP circuit draws the current from CL and the internal node voltage becomes lower. However, in the source-bulk connected techniques, the large bulk-to-well PN-junction capacitance increased the parasitic capacitance at each pumping node. Second, to control the diode-connected MOSFETs' body terminals dynamically, auxiliary MOSFETs are used in the source-bulk scheme, which generated the substrate current floating-well devices. However, using these extra circuitries caused large power dissipation with a large chip area [32].

Tanzawa et al. (2002) proposed a CP based on Umezawa et al.'s design principle. The proposed CP configuration required several logic circuits and PC2 switches. In this design, an additional circuit is added, which reduces the number of PC1 elements to only four. Moreover, most of the capacitors in the PC1 scheme only added a 10% increment of the total area in the PC2 method. Additionally, in this design, only high voltage transistors are included with intrinsic capacitors [8].

Pelliconi et al. (2003) proposed a power-efficient charge pump in 2003, including low-voltage transistors and a simple two-phase clocking scheme. In this method, higher operating clocks have engaged compared to other conventional methods. As a result, it has obtained high-current, high-efficiency and small-chip area. Around 100 MHz clock frequency has been received from the measured results. However, the circuit has secured fast switching times on low resistance and low capacitors. However, the circuit could not manage higher efficiency and boosted output voltage [33].

In 2005, Yan and Min proposed a CP method based on all P-channel metal–oxide–semiconductor (PMOS) transistors, suitable for the standard CMOS process. In this scheme, only low voltage PMOS transistors are used with the switching substrate technique to boost the transistors. Moreover, in this design, body effects have been eliminated to increase the output voltage and threshold voltage loss. This body effect was also reduced by employing the linear operation of PMOS based charge transfer switches. Therefore, this scheme has become compatible with low voltage memory applications. However, using all the PMOS transistors for transferring charge from one stage to another substrate current increased, resulting in higher power dissipation [34].

In 2008, Su and Ma proposed a four-phase CP circuit to reduce the reversion and conduction loss in each step. In this scheme, the voltage drop method is reduced in each sub-cell during the power stage. As a result, higher efficiency has been achieved with a low ripple and lower fabrication cost. Moreover, involving a subthreshold clock generator reduced the power loss in the controller. Therefore, it has provided an effective solution to the applications related to low voltage and low-power system-on-chip power converters. However, due to many capacitors, the proposed CP is not entirely free from parasitic effects [35].

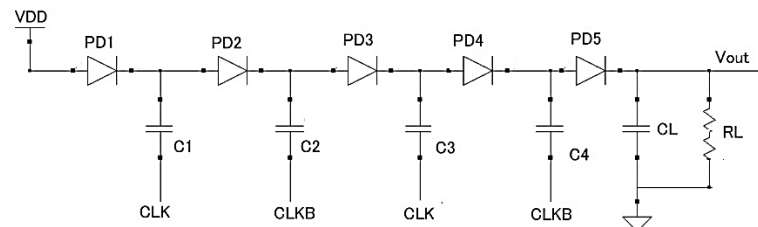
Richelli et al. presented two CP methods for NVM with dynamic biasing of the gate and the body voltages. In this scheme, the device voltage loss problem created due to the device threshold has been controlled through gate and body biasing of every pass transistor. By using this scheme, a charge was pumped with minimal voltage drop and high conductivity. This scheme provided higher output voltage and pumping efficiency with involving only a two-phase clocking scheme. However, this design occupied a large chip area due to two pumping stages [36–38].

### 2.3. CP for DC–DC Converter

Shiau et al. (2007) implemented a polysilicon diode-based low voltage CP. There is no limitation of the boosted output voltage in this scheme, as polysilicon diodes are fully isolated from the silicon substrate as shown in Figure 3. Moreover, in this design method,



CP is not limited by MOSFETs junction breakdown voltage, which can implement in a standard CMOS process. However, in this scheme, the body effect has not been eliminated, which is the main disadvantage of a diode-based CP circuit [39].



**Figure 3.** Static charge transfers switch based CP circuit [39].

Huang et al. proposed a CP circuit based on dual-phase mode [40]. In this scheme, several phases have been observed with the completely compact CP circuit with multiphase current-mode control. This structure involved the sensor stage, the buffer stage, the power stage, the automatic body switching (ABS) circuit, and the non-overlap circuit. The proposed structure claimed to have low ripple voltage, small chip area with high system stability. However, due to several phases, parasitic capacitance and resistance effect have not been controlled correctly in this structure.

In 2010, Peng et al. proposed a CTS-based CP circuit, where auxiliary capacitors and transistors were used to dynamically bias the CTSs to the influence of the switch's threshold voltage transistor. Moreover, this design aims to improve the pumping efficiency and lower the threshold voltage when it is turned on during charge transfer and acquires higher when turned off [41]. However, the power dissipation was high, and the pumping efficiency or voltage gain was still lower owing to the complex switching mechanism.

To remove the body effect of the diode-connected CP circuit and direct the flow of charges in pumping operation, MOSFET switches with proper on/off cycles, referred to as charge transfer switch (CTS) used to design the charge pump circuit. The CTS was able to produce better pumping gain than the diodes. Many researchers developed the CP with CTS, which required an auxiliary pass transistor to turn off the CTS entirely in the designated period [42]. Dong-Sheng et al. (2006) designed a CP circuit using the CTS topology, which had parasitic capacitors at each pumping node. The CTS method is widely used as with proper dynamic control technique of the MOSFETs to turn on/off entirely in the desired period [43].

Moreover, there was no voltage drop between the drain and source terminal. Hence, the MOSFET switch could shift the charge without suffering the constraint of the threshold voltage. The dynamic control circuit-controlled CTS to transfer the amounts from one stage to another without the threshold voltage drop [42]. However, the extra power dissipation of the parasitic capacitance caused the high-power indulgence in this scheme.

Yan et al. (2012) designed a CP circuit using an improved charge sharing method, which had six stages with six pumping capacitors at each pumping node. In this design, Yan et al. improved the charge pump circuit's performance based on the CTS method. Moreover, a zero  $V_{th}$  MOSFET was adopted to overcome the  $V_{th}$  drop at every node. Furthermore, the charge transfer switches can turn on/off completely, and feedback current reduced. However, this design dissipated an enormous power with a small number of stages due to complex circuitry [44].

Wei et al. (2013) proposed an enhanced or NCP-2 CTS CP circuit to the shortest charge flow with improved voltage pumping gain. In this design, the diode-configured design limitations were managed using a proper clock scheme and the pumping capacitors' sizing. Moreover, the strategy had the least parasitic capacitance effects. However, the system had low output voltage, higher power dissipation, and increase pumping efficiency [45].

In 2016, Zucchelli et al., proposed an inductor-based CP design scheme, fully integrated into DC/DC converter. Though the design was the modified version of the primary

Dickson CP circuit, it provides enhanced performances due to small inductors' involvement in the first stage of the charge transfer process as shown in Figure 4a,b. Therefore, the proposed design able to reduce power dissipation, rise time and output voltage ripple. Besides, this design was free from external components, making it compatible with CMOS technology [46].

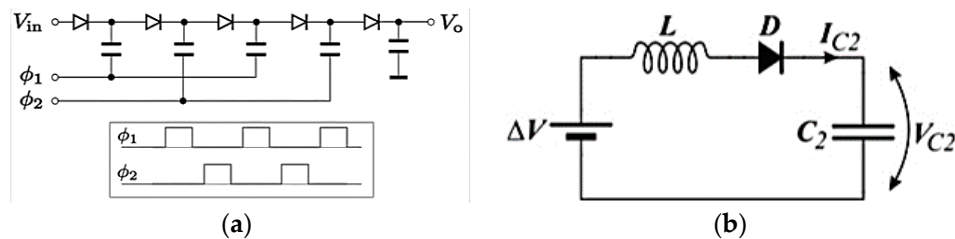


Figure 4. (a) Schematic of the inductor-based CP circuit (b) first stage of the CP [46].

Rumberg et al., in 2017, came up with a new regulated CP circuit, which has designed based on floating-gate transistors. This type of structure is suitable for applications that required tunneling voltages to program floating-gate transistors. Due to its compact architectural design, the CP has leveraged variable frequency regulation and minimized short-circuit current to provide stable tunneling voltages. This design can reduce power dissipation. However, this circuit is not suitable for applications that needed standard CMOS transistors [47].

A high voltage generator based on the CP scheme has demonstrated by Abdi et al. in 2018, which features novel voltage regulation with a variable clock frequency. In this topology, an input voltage modulation has been added to a low-dropout regulator at the input stage to forward the input voltage to the next node. As a result, higher output voltage with stable voltage regulation has been achieved in this method. Moreover, thick-oxide transistors are employed to enhance the pumping efficiency and maintain the substrate/n-well voltage level during operation [48].

Rahman et al. proposed a modified charge transfer switch-based CP circuit in 2020 to be compatible with RFID tag EEPROM as shown in Figure 5. In this design, instead of diode-configuration, all NMOS switches in the charge transfer nodes. As a result, this topology could manage to reduce the substrate current and overall power dissipation. Additionally, in this design, the researchers can minimize the output ripple voltage and the chip layout area. This scheme has also integrated with a voltage regulator to produce a steady-boost voltage, the RFID tag memories requirement [1].

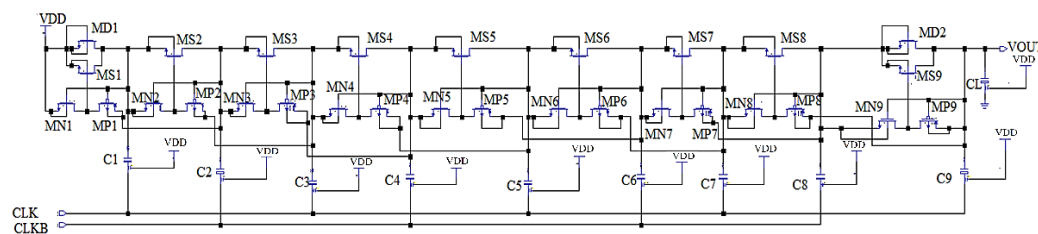


Figure 5. Schematic diagram of the CTS CP [1].

#### 2.4. CP for Energy Harvesting

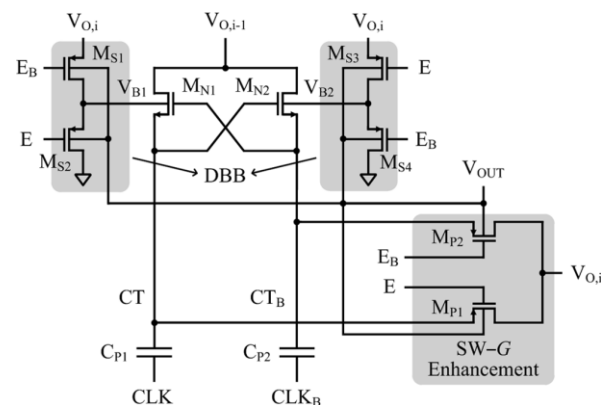
In 2008, Richelli et al. proposed a boosted CP design scheme suitable for energy harvesting. It has the feature of increasing output voltage from a very low supply voltage of about 150 mV. This scheme was designed using the new hybrid inductive and capacitive architecture. In particular, this method only consists of NMOS transistors, which were

utilized as pass-transistors. Therefore, this scheme has a low threshold voltage compared to a PMOS-based CP circuit [49].

Shih and Otis et al. presented a modified four-phase CP circuit suitable for a fully integrated dc-dc converter for micropower energy harvesting. This modified CP can boost the voltage up to  $3 \times V_{DD}$  in free-running mode even if the input voltage automatically running down up to 270 mV. To do this autonomous voltage control, this modified CP did not use any external extraction. As a result, this adjusted CP ensured a regulated voltage supply at 1.4 V with only three  $\mu\text{W}$  power dissipation. However, this topology was unable to provide higher pumping efficiency with a higher chip area. Simultaneously, this mechanism is not compatible with many applications as the circuit modified to be compatible with DC–DC converter for micropower energy harvesting applications with stringent size constraints [50].

Recently, Peng et al. (2014) proposed a cross-coupled-based CP circuit following the Ker et al. design [51,52]. The body biasing and backward charge pump scheme was introduced in this method, which could completely turn off/on the MOS transistors. As a result, voltage loss during switching reduced and the reverse charge sharing problem decreased. Moreover, low voltage operation was arisen due to the involvement of the sub-threshold organization. Nevertheless, two branch CP circuits designed by Peng et al. resolved all the boundaries of the Ker et al. CP circuit, where the pumping effectiveness was found 89% and 0.1 mS pumping speed was delivered. However, this designed CP required 320 mV for start-up, which was higher than other designs with high power dissipation due to its complex circuitry. Moreover, immense leakage current occurred due to unsuitable body biasing and controlling scheme.

Kim et al. (2015) proposed a CP circuit with dynamic body-biasing (DBB) to solve the limitations of high current transfer and high body leakages as shown in Figure 6. In this scheme, dead-time restrictions, conduction loss, and constraints were taking into concern during the design process regarding high voltage adaptation efficacy (VCE) and cut the power conversion efficiency (PCE) of [53].



**Figure 6.** Dynamic-body-biasing CP [53].

In 2016, Mondal et al. proposed an inductor-less switching CP circuit suitable for solar energy harvesting. In this method, the charge transfer capability has improved and the charge sharing time to load. Moreover, in this scheme, a new single-clock tree-topology has been introduced to design the CP circuit, which has provided better charge transfer capability and sharing time. This proposed method has produced higher pumping efficiency for applications like the microscale energy harvesting system [54].

In 2019, Li et al. proposed a temperature-insensitive CP circuit, where the output voltage included a linear adjustment range. In this method, no bipolar-CMOS-DMOS (BCD) technology has been added to generate the output voltage higher than the n-well/substrate diode's breakdown voltage, which has utilized triple-well NMOS. Besides, the pumping clock's amplitude has been controlled continuously to produce a closed-loop regulation of



voltage to make it insensitive to temperature changes. In a closed-loop control mechanism, the CP output has steady voltage regulation with a voltage deviation of only 1.1%. As a result, the proposed CP scheme has the compatibility of sensor accuracy for controlling micro gyroscopes. No external high voltage device must be integrated with the gyroscope measurement system [55].

### 3. Discussion

This review summarized different CP design methods based on their applications, as presented in Table 1. At present, low power, low ripple, higher efficiency, higher output voltage, and high-performance CP circuits are in high demand to NVMs, DC–DC converters, RFID systems, PLL-based design, energy harvesting, and many other applications. During any CP circuit design process, the main concern is to ensure that the method can produce a higher output voltage from a very low supply voltage. Another critical feature of designing a CP circuit is maintaining a low power dissipation, which made it compatible with low power applications, as mentioned earlier. These applications also required a highly efficient CP design method, which could be degraded by increasing the number of CP design stages with large output ripple voltage. Additionally, a highly stable and regulated high voltage generation process is desirable to the researchers who deal with low power design specifications in CMOS.

**Table 1.** Performance comparison of different CP design topologies based on DC–DC converters and memory devices.

Source	Design Topology	Process ( $\mu\text{m}$ )	Supply Voltage VDD (V)	Frequency $f_{clk}$ (MHz)	Output $V_{out}$ (V)	Pumping Efficiency (%)	Die Area ( $\text{mm}^2$ )	Applications
[1]	CTS	0.13	1.2 ~ 1.8	11.3	9.6~14.59	88~90	0.044	RFID tag EEPROM RFID
[2]	enhanced-NCP2CTS	0.18	1.8	20	5.95	66	2.4	transponder Memory Flash memories
[8]	intrinsic high-voltage transistors	0.18	1.8	-	4–18	40	-	EEPROM and Flash memories
[24]	two-step adiabatic switching	0.25	2.5	-	9.16	57	-	NVM Flash memories
[32]	body bias technique	0.35	3	10	6	-	-	NVM Flash memories
[33]	clocking scheme	0.18	1.8	100	10.1	55	-	Memory application
[34]	all PMOS CP	0.35	2	3	15.5	-	-	DC– DCconverter
[35]	4-phase complementary charge pump.	0.18	1.8	4	1.89	92.01	-	DC– DCconverters
[39]	static CTS	0.35	1.5	1.5	7.5	-	20	DC– DCconverter
[40]	switched-capacitor-based	0.35	2.9	0.25	5.5	90	2454.8	NVM
[41]	dynamically bias the CTS's	0.18	2	0.78	9.8	54	15.75	NVM DC– DCconverter
[43]	dynamic CTS	0.35	3.3	3	2.5–5	-	0.6	NVM DC– DCconverter
[44]	improved charge sharing method	0.35	3.3	5	14	83.3	-	NVM DC– DCconverter
[47]	regulated CP	0.35	2.5	30	16	34	69	NVM DC– DCconverter
[48]	frequency modulation	0.18	2.8	10	12.8	80	0.6	

Therefore, from Table 1, it is being found that many proposed CP topologies are focused on reducing ripple voltage, simple design architectures, lower chip area while generating higher output voltage from a very low power supply voltage. CP circuit design schemes are classified based on voltage-controlled or current controlled approaches. Table 1 shows that all the researchers have presented their design topologies considering and maintaining the design mentioned above parameters while designing the CMOS CP circuits. Conventionally, any memory devices required comparatively higher output voltage (around 5 V to 23 V) generated from the low power supply voltage (about 1.2 V to 3.3 V) to perform their read/write/erase operations. In this application, a regulated voltage supply is in demand, so selecting a CP scheme that has the option for voltage

regulation would benefit the researchers. Many topologies managed to overcome the threshold voltage drop, reversion and conduction loss by maintaining the proper transistor sizing. By reducing the transistor's parasitic effects, some have achieved higher pumping efficiency (more than 80%) with lower chip areas and reduced ripple voltages.

Besides, [1,2,8,24,33,34] proposed CP design schemes, which are suitable for RFID tag memory, flash memories and EEPROM. It is necessary to produce higher output voltage with low ripple and low power dissipation for EEPROM/flash memories to do the read/write/erase operations. Therefore, it is clear from Table 1 that if anyone wanted to design CP circuit for RFID tag memory, then the CTS based modified CP would be the solution [1]. In this method, the design achieved low power, high efficiency, and low output ripple. If all the transistors are appropriately matched, then the parasitic capacitor's effect can be eliminated, generated from this design. Furthermore, this design reduced the chip layout area. This method has successfully integrated into other devices to form the integrated high voltage generator from a very low power supply voltage for RFID tag EEPROM. Eventually, considering flash memory specification, this CP circuit can be one solution for future researchers.

It is summarized in Table 1 that, though [32,41,43,47] proposed different schemes for designing CP circuits, but all of these methods are compatible with NVM. In terms of higher output voltage, [41] can generate the higher output voltage, improved pumping efficiency and lower the threshold voltage. However, this design consumed much power due to the intricate design scheme and the chip layout size is more extensive compared to others. On the other hand, the CP design scheme proposed by [47] has the advantages of minimized short-circuit current, compact design, small chip area and low power consumption. This design is not compatible with all low power applications. Instead, it is only suitable for floating gate tunneling based transistors like NVM and MEMS devices. In Table 1, it is shown that [35,39,40,44,48] also proposed a CP design method for generating boosted output voltage for DC–DC converters. Based on the comparison as shown in Table 1, it can be suggested that if future researchers wanted to design a CP circuit for generating a high voltage converter or DC–DC converter, they could easily choose the topology proposed by [48]. This proposed topology managed to generate a higher output voltage from the low power supply voltage and higher pumping efficiency (80%) and a low chip area of only 0.6 mm<sup>2</sup>. Among these schemes, [44] has produced higher output voltage and this design has the benefit of eliminating the reverse charge sharing problem. Table 1 also found that the CP circuit proposed by [44] has ensured higher pumping efficiency with the compensations with zero  $V_{th}$  MOSFET and CTS's can turn on/off completely. Though this design can reduce feedback current, it necessitates increased power dissipation if the stage number grows along with complex circuitry. This design required a larger chip layout area, which is considered a drawback in the CMOS process.

On the other hand, energy harvesting devices also require a CP circuit to boost voltages to perform the process. This sector does not need much higher voltage compared to memory devices. Thus, the pumping efficiency levels are not that much higher in these topologies than other CP circuits based on low voltage applications, i.e., RFID transponder memory, NVM, DC–DC converters, PLL devices, etc. Moreover, these topologies have also required extra circuitry, which eventually increases the overall chip area and power dissipation. Table 2 shows the summary of the topologies used recently for CP circuit design.

**Table 2.** Performance comparison of different CP design topologies based on energy harvesting.

Source	Design Topology	Process ( $\mu\text{m}$ )	Supply Voltage VDD (V)	Frequency $f_{clk}$ (MHz)	Output $V_{out}$ (V)	Pumping Efficiency (%)	Die Area ( $\text{mm}^2$ )	Applications
[50]	boost converter scheme	0.13	0.27	0.80	1.4	58	0.42	energy harvesting with PV cell
[51]	cross-coupled body bias	0.18	0.32	0.45	2.04	89	1376	energy harvesting
[53]	cross-coupled with DBB	0.13	0.15	0.25	0.619	54	66	low voltage energy harvesting
[54]	single-clock tree topology	0.18	0.39 – 0.43	17 – 23	1	70	0.48	microscale solar energy harvesting
[55]	closed loop control	0.18	5	0.01	16.95	-	2.53	sensor based microgyroscope

Table 2 shows that the CP circuit scheme designed by [50] generates  $3\times$  higher output voltage than the supply voltage. This design requires less chip area. However, this method is unable to provide higher pumping efficiency. On the other hand, [51] has a fast-pumping rate at 0.1 ms and reduces leakages with body biasing for PMOS only. However, this design required interleaved inverters and extra stages, increasing the power dissipation. In [53], the method works in very low supply voltage with higher output voltage and higher efficiency. This design has the disadvantage, too, as it required off-chip capacitors and extra complex circuitry for clocking and dynamic bulk-biasing. Instead, the CP topology proposed by [54] has achieved a higher output voltage with a lower chip area. Though the pumping efficiency is not highest than other researchers, future researchers would pick this topology if there is any place for the trade-off between efficiency and implementation cost. Finally, [55] proposed CP scheme has the advantages of linear output voltage, stable voltage regulation, and temperature insensitive output voltage. Still, it lacks lower temperature variations, which is considered the disadvantage of this topology.

Therefore, this review illustrates various CP design topologies for low power applications, which have recommended the considerations and trade-off between low voltage, low power and higher pumping efficiency to select the optimum CP method. This research also suggested that numerous CP design schemes be compatible with low power applications, especially in RFID tag memory, DC–DC converters and energy harvesting devices. Hence, this review article would be the future guideline to find a better option and scheme to design a CMOS based CP circuit by considering the critical performance parameters mentioned above for low power applications.

#### 4. Conclusions

In this article, various topologies of designing CP circuits for low power applications are reviewed based on different design schemes. CP's essential features, i.e., output voltage gain, power efficiency, die area occupation, handling frequency levels, input supply voltage, CMOS process and the charge pumping capabilities, are compared in detail and based on the reviews, suitable applications for these topologies are also illustrated. The three commonly used applications, such as memory, DC–DC converters and energy harvesting area, are identified from various design methods and their performances are figured out from this review. Therefore, this study provides a useful reference for future researchers to select the appropriate design topology for CP circuits under technological and operational constraints.

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