



Article 3.3-kV 4H-SiC Split-Gate DMOSFET with Floating p+ Polysilicon for High-Frequency Applications

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Abstract: A split-gate metal-oxide-semiconductor field-effect transistor (SG-DMOSFET) is a wellknown structure used for reducing the gate-drain capacitance (CGD) to improve switching characteristics. However, SG-DMOSFETs have problems such as the degradation of static characteristics and a high gate-oxide electric field. To solve these problems, we developed a SG-DMOSFET with floating p+ polysilicon (FPS-DMOSFET) and compared it with a conventional planar DMOSFET (C-DMOSFET) and a SG-DMOSFET through Technology Computer-Aided Design (TCAD) simulations. In the FPS-DMOSFET, floating p+ polysilicon (FPS) is inserted between the active gates to disperse the high drain voltage in the off state and form an accumulation layer over the entire junction field effect transistor (JFET) region, similar to a C-DMOSFET, in the on state. Therefore, the FPS-DMOSFET can minimize the degradation of static characteristics such as the breakdown voltage (BV) and specific on resistance (R_{ON,SP}) in the split-gate structure. Consequently, the FPS-DMOSFET can shorten the active gate length and achieve a gate-to-drain capacitance (C_{GD}) that is less than those of the C-DMOSFET and SG-DMOSFET by 48% and 41%, respectively. Moreover, the high-frequency figure of merit (HF-FOM = $R_{ON,SP} \times C_{GD}$) of the FPS-DMOSFET is lower than those of the C-DMOSFET and SG-DMOSFET by 61% and 49%, respectively. In addition, the FPS-DMOSFET shows an E_{MOX} of 2.1 MV/cm, which guarantees a gate oxide reliability limit of 3 MV/cm. Therefore, the proposed FPS-DMOSFET is the most appropriate device to be used in high-voltage and high-frequency electronic applications.

Keywords: 4H-SiC; DMOSFET; split-gate; switching; energy loss; high-frequency

1. Introduction

4H-SiC metal-oxide-semiconductor field-effect transistors (MOSFETs) are considered promising candidates for high-temperature and high-voltage applications [1,2]. Recently, several studies have been conducted on trench MOSFETs (UMOSFESTs) owing to their high channel mobility and small cell pitch [3–5]. However, a high gate-oxide electric field occurs at the trench gate corner, leading to reliability issues in the gate oxide. To achieve stable operation, the maximum electric field in the gate oxide (E_{MOX}) must be lower than 3 MV/cm [6]. In addition, the gate-drain capacitance (C_{GD}) and gate-drain charge (Q_{GD}) of trench MOSFETs are higher than those of planar MOSFETs (DMOSFESTs) due to the large cell density. Furthermore, in high-voltage applications (>3.3 kV), the channel resistance of trench MOSFETs does not have a significant effect on the overall resistance owing to the thick drift region [7]. Therefore, planar MOSFETs are more suitable for high-voltage and high-frequency applications.

The high-frequency performance of SiC MOSFETs is generally evaluated using the high-frequency figure of merit (HF-FOM), which is calculated as $R_{ON,SP} \times Q_{GD}$ or $R_{ON,SP} \times C_{GD}$, where $R_{ON,SP}$ is the specific on resistance. A well-known method for reducing C_{GD} is the use of the split-gate MOSFET (SG-MOSFET) structure [8,9], which is shown in Figure 1b. This structure improves HF-FOM through reduction of C_{GD} by decreasing the active gate



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Copyright: © 2021 by the authors. Licensee MDPI, Basel, Switzerland. This article is an open access article distributed under the terms and conditions of the Creative Commons Attribution (CC BY) license (https:// creativecommons.org/licenses/by/ 4.0/). length protruding into the n-drift region (L_{SG}). However, this structure substantially decreases Baliga's figure of merit (BFOM), which is calculated as $BV^2/R_{ON,SP}$ [10]. In particular, SG-DMOSFETs have a serious problem of a high E_{MOX} at the gate-oxide corner, which leads to issues with the reliability of the gate oxide. Previously, we showed that, for high-voltage (>3.3 kV) SG-DMOSFETs, the BFOM reduction is intensified as the L_{SG} decreases compared to the HF-FOM improvement [11]. The decrease in BFOM and gate-oxide reliability issues limits the ability of SG-DMOSFETs to improve HF-FOM at high voltages.



Figure 1. Schematic cross-sectional views of the MOSFETs. (a) C-DMOSFET (conventional planar DMOSFET); (b) SG-DMOSFET (split-gate DMOSFET); (c) FPS-DMOSFET (floating p+ polysilicon DMOSFET).

The present study proposes and analyzes a new SG-DMOSFET with floating p+ polysilicon (FPS-DMOSFET) in comparison with a conventional planar MOSFET (C-DMOSFET) and conventional SG-DMOSFET through technology computer-aided design Technology Computer-Aided Design (TCAD) simulations. The floating p+ polysilicon (FPS) of the FPS-DMOSFET forms an accumulation layer in the on state and disperses the high drain voltage due to the relatively low potential in the off state. Consequently, the FPS-DMOSFET can have a shorter L_{SG} with significantly less BFOM degradation than the SG-DMOSFET. In addition, it can overcome the problem of electric-field crowding at the active gate oxide, enabling stable operation. The simulation results show that the FPS-DMOSFET achieves not only the best HF-FOM among the studied structures but also an E_{MOX} lower than 3 MV/cm.

2. Device Structures and Fabrication Process

The simulations in this study were conducted using Sentaurus TCAD simulation from Synopsys, Inc. [12]. The models used in the simulation include the doping-dependent carrier mobility model; Shockley–Read–Hall (SRH) recombination, Auger recombination, and inversion and accumulation layer mobility models, and de Man models for impact ionization. Incomplete ionization, high-field velocity saturation, and band-narrowing models are also used [13–15].

2.1. Device Concept and Key Parameters

Figure 1 shows schematic cross-sectional views of (a) a C-DMOSFET, (b) a SG-DMOSFET, and (c) the proposed FPS-DMOSFET. The doping concentration and device dimensions of the C-DMOSFET and SG-DMOSFET are described in our previous work [10]. All structures had a drift-layer thickness of 30 μ m and an n-drift doping concentration of 1.5×10^{15} cm⁻³. The channel length was 0.5 μ m, the doping concentration of the channel region was 1×10^{17} cm⁻³, and a fixed charge concentration of 3×10^{12} cm⁻² was included at the interface between 4H-SiC and SiO2 to set an adequate threshold voltage. In addition, the L_{SG} of the SG-DMOSFET was 0.7 μ m. The detailed device parameters are listed in Table 1. In the FPS-DMOSFET, FPS is inserted between the active gates. It plays a role in preventing the deterioration of the static characteristics because FPS disperses the high

Parameter	Value	Unit
W _{CELL}	5	μm
W _{DRIFT}	30	μm
L _{CH}	0.5	μm
W _{JFET}	1.25	μm
p+ base depth	1	μm
Gate oxide thickness	50	nm
n+ source doping concentration	$1 imes 10^{19}$	cm^{-3}
Channel doping concentration	$1 imes 10^{17}$	cm^{-3}
p+ base doping concentration	$5 imes 10^{19}$	cm^{-3}
n-drift doping concentration	$1.5 imes10^{15}$	cm^{-3}
L _{SG} of SG-DMOSFET	0.7	μm
L _{SG} of FPS-DMOSFET	0	μm

drain voltage in the off state and forms an accumulation layer in the on state, resulting in superior BFOM compared to the SG-DMOSFET.

Table 1. Device parameters of the three devices.

2.2. Proposed Fabrication Process

Figure 2 shows the proposed fabrication procedure of the FPS-DMOSFET. First, the p+ base and n+ source regions are formed by ion implantation. Next, thermal oxidation and n+ polysilicon deposition are performed, as shown in Figure 2b. Then, n+ polysilicon is etched using reactive-ion etching (RIE) to form a split active gate. Subsequently, an interlayer dielectric oxide (ILD) is deposited through low-pressure chemical vapor deposition (LPCVD), which forms a relatively low defect density [16,17]. Next, the ILD is etched to form space for FPS. The thickness of the side oxide between the active gate and FPS (T_{S,OX}) is one of the most important parameters in FPS-DMOSFETs, which affects both static and dynamic characteristics. Therefore, in this ILD etching process, T_{S,OX} is determined by the alignment of the ILD etching process. Accordingly, the oxide between the FPS and n-drift is formed with a thickness of 50 nm through thermal oxidation. Next, p+ polysilicon is deposited by LPCVD and etch-back [18,19]. ILD is deposited through LPCVD again. Finally, the source and drain electrodes are formed.



Figure 2. Proposed fabrication procedure of FPS-DMOSFET (floating p+ polysilicon DMOSFET). (**a**) form the p+ base and n+ source region; (**b**) thermal oxidation and n+ polysilicon deposition; (**c**) n+ polysilicon etching; (**d**) ILD (interlayer dielectric oxide) oxide deposition; (**e**) oxide etching and oxidation; (**f**) p+ polysilicon deposition and etch back; (**g**) ILD oxide deposition and etching; (**h**) form the source and drain electrode.

3. Results and Discussion

3.1. FPS-DMOSFET Optimization

In the FPS-DMOSFET optimization process, L_{SG} is one of the most important parameters that determine the performance. A decrease in L_{SG} leads to a decrease in C_{GD} , which improves the HF-FOM; however, it causes deterioration of static characteristics such as BV and $R_{ON,SP}$. Therefore, L_{SG} should be optimized to enhance the performance of the proposed FPS-DMOSFET, considering both BFOM and HF-FOM.

Figure 3 shows the change rate of $R_{ON,SP}$, BV, and C_{GD} according to L_{SG} . To simultaneously analyze the effect of L_{SG} on device characteristics, the $R_{ON,SP}$, BV, and C_{GD} of the FPS-DMOSFET were compared by dividing them by the corresponding values for the C-DMOSFET. First, as shown in Figure 3, the FPS-DMOSFET does not increase $R_{ON,SP}$ even if L_{SG} decreases, unlike the SG-DMOSFET, because the FPS forms an accumulation layer in the on state. This allows the FPS-MOSFET to significantly improve the trade-off relationship between BFOM and HF-FOM. On the other hand, a decrease in L_{SG} affects BV and C_{GD} . Figure 3 shows that a reduction of L_{SG} slightly decreases BV while causing a significant improvement in C_{GD} . Therefore, considering both BFOM and HF-FOM, the best performance of the FPS-DMOSFET can be obtained when L_{SG} is set to 0 μ m. Although it is difficult to achieve precise alignment in the fabrication process, we assumed it to be the ideal case in the simulation. In addition, as the FPS-DMOSFET is proposed for high-frequency applications, optimization has been performed with a focus on reducing C_{GD} .



Figure 3. Change rate of C_{GD} , $R_{ON,SP}$ and BV (gate-to-drain capacitance, specific on resistance and breakdown voltage) compared to C-DMOSFET (conventional planar DMOSFET) when $T_{S,OX}$ (thickness of the side oxide) is 250 nm.

However, the FPS-DMOSFET has a higher C_{GD} than the SG-DMOSFET when they have the same L_{SG} . Figure 4 shows the C_{GD} change of the SG-DMOSFET and FPS-DMOSFET according to the change in L_{SG} . In Figure 4, the C_{GD} of the FPS-DMOSFET is larger than that of the SG-DMOSFET when both have the same L_{SG} because of the FPS between the active gates in the FPS-DMOSFET. Figure 5 shows the capacitance analysis of the two structures and a capacitance model that schematically shows these capacitances. The C_{GD} of the SG-DMOSFET consists of a series connection of (1) Cox, the capacitance formed by the overlapping region between the active gate and n-drift and (2) C_{DEP} , the capacitance formed by the depletion region in the junction field effect transistor (JFET) region [9]. Therefore, the C_{GD} of the SG-DMOSFET can be expressed as follows:

$$C_{GD} = \frac{C_{OX} \times C_{Dep}}{C_{OX} + C_{Dep}} \tag{1}$$

$$C_{GD} = \frac{(C_F + C_{OX}) \times C_{DEP}}{(C_F + C_{OX}) + C_{DEP}}$$
(2)

$$C_F = \frac{C_{F1} \times C_{F2}}{C_{F1} + C_{F2}}$$
(3)

where C_F is the total capacitance of the additional factors due to the FPS of the FPS-DMOSFET. In Equation (3), C_{F1} is the capacitance formed by the overlapping region between the active gate and FPS, and C_{F2} is the capacitance formed by the overlapping region between the n-drift and FPS. In other words, C_{F1} is determined by the side-oxide thickness between the active gate and FPS ($T_{S,OX}$), and C_{F2} is determined by the gate-oxide thickness (T_{OX}). Based on Equation (2), C_F must be minimized to reduce the C_{GD} of the FPS-DMOSFET. However, there is a limit to the increase in T_{OX} because it has a significant influence on the static characteristics. Therefore, the FPS-DMOSFET was optimized by increasing $T_{S,OX}$ to reduce C_F .







Figure 5. Depletion lines and C_{GD} (gate-to-drain capacitance) factors distribution of (a) SG-DMOSFET (split-gate DMSOFET); (b) FPS-DMOSFET (floating p+ polysilicon split-gate DMOSFET); and (c) models schematically showing the capacitance of the two structures.

Figure 6 shows the C_{GD} change of the FPS-DMOSFET according to variations in L_{SG} and $T_{S,OX}$. The straight lines of each color show the C_{GD} of the SG-DMOSFET, which has a different L_{SG} . The total C_{GD} of the FPS-DMOSFET decreases with increasing $T_{S,OX}$ and then gradually saturates to a similar level to that of SG-DMOSFET. This result is consistent with the capacitance model of FPS-DMOSFET established in Figure 5. Therefore, $T_{S,OX}$ must be increased to minimize C_F . However, increasing $T_{S,OX}$ decreases BV because the drain-voltage dispersion effect of the FPS is reduced in the off state. Therefore, $T_{S,OX}$ should be

optimized to enhance the performance of the FPS-DMOSFET. In Figure 6, C_{GD} begins to gradually saturate to a level similar to that of SG-DMOSFET for all L_{SG} values from the point where $T_{S,OX}$ is 250 nm. Therefore, the optimized $T_{S,OX}$ of the FPS-DMOSFET is set to 250 nm.



Figure 6. Comparison of C_{GD} (gate-to-drain capacitance) values of SG-DMOSFET (split-gate DMOS-FET) and FPS-DMOSFET (floating p+ polysilicon split-gate DMOSFET) according to L_{SG} (active gate length) change.

3.2. Static Characterisitics

Figure 7 shows the static characteristics, such as BV, $R_{ON,SP}$ of the three structures. These results are summarized in Table 2. The on-state characteristics were obtained with V_{GS} and V_{DS} set to 20 V. The C-DMOSFET and FPS-DMOSFET have the same $R_{ON,SP}$ of 15.66 m $\Omega \cdot cm^2$, but the SG-DMOSFET has a higher $R_{ON,SP}$ of 17.88 m $\Omega \cdot cm^2$. All three structures have the same structure, except for the gate structure. This implies that only the gate structure affects $R_{ON,SP}$. This can be explained through the following equations representing the accumulation-layer resistance ($R_{A,SP}$) and JFET resistance ($R_{JFET,SP}$), respectively [21]:

$$R_{A,SP} = K_A \frac{L_{SG} W_{Cell}}{4\mu_{nA} C_{OX} (V_G - V_{TH})}$$
(4)

$$R_{JFET,SP} = \frac{\rho_{JFET} x_{JP} W_{Cell}}{L_{SG} - 2W_0}$$
(5)

where K_A is a coefficient accounting for the current spreading from the accumulation layer to the JFET region, W_{CELL} is the cell pitch, μ_{nA} is the electron mobility of the accumulation layer, V_{GS} is the biased gate voltage, and V_{TH} is the threshold voltage. In Equation (5), ρ_{JFET} is the conductivity of the JFET region, and W_0 is the zero-bias depletion width formed by the junction between the p-base and n-drift under the gate. According to the above equations, a shorter L_{SG} results in a shorter accumulation-layer length, implying a decrease in $R_{A,SP}$. However, this causes a larger increase in $R_{JFET,SP}$ and a resultant increase in $R_{ON,SP}$. In addition, in the off state (Figure 7b), the leakage current of the FPS-DMOSFET is the largest and the C-DMOSFET is the smallest. This is because the voltage applied to the body diode composed of p+ base and n-drift increases as the active gate length decreases. However, since the leakage currents of the three structures are almost the same, the overall characteristics are not significantly affected.



Figure 7. Static characteristics of the three structures. (a) output curve in the on state and (b) off state leakage current.

Parameter	C-DMOSFET	SG-DMOSFET	FPS-DMOSFET	Unit
R _{ON,SP}	15.66	17.85	15.66	$m\Omega\times cm^2$
BV	3421	3284	3266	V
BFOM	747.3	604.2	681.2	MW/cm ²
E _{MOX}	2.1	3.4	2.1	MV/cm

Table 2. Static characteristics of three structures.

 $R_{ON,SP}$: specific on resistance; BV: breakdown voltage; BFOM: Baliga's figure of merit calculated as $BV^2/R_{ON,SP}$; E_{MOX} : maximum gate oxide electricfield.

Figure 8 shows the electron current densities of the three structures with V_{GS} and V_{DS} set to 20 V. In Figure 8a, the accumulation layer is formed on the entire JFET region owing to the active gate of the C-DMOSFET. On the other hand, in Figure 8b, the accumulation layer breaks in the middle of the JFET because no active gate exists in the middle of the JFET region. As previously mentioned, it leads to an increase in R_{ON,SP} due to the increase in R_{IFET.SP}. Therefore, the SG-DMOSFET, which has a shorter L_{SG}, has a 14% larger R_{ON.SP} compared with the C-DMOSFET. However, as shown in Figure 8c, the FPS-DMOSFET shows the same transformation of the accumulation layer as the C-DMOSFET, despite having a smaller L_{SG} than those of the C-DMOSFET and SG-DMOSFET. This is because FPS, which has a high electrostatic potential, forms an accumulation layer over the entire JFET region. In addition, Figure 9 shows the electrostatic potential of the three structures with V_{CS} and V_{DS} set to 20 V. Figure 9b shows that the SG-DMOSFET has a remarkably low electrostatic potential in the region where the active gate does not exist. However, as shown in Figure 9c, the electrostatic potential of the FPS is very close to that of the active gate; therefore, the FPS-DMOSFET shows a similar performance as the C-DMOSFET in the on state. In the off state, the p+ base junction is the main region that sustains the high drain voltage before avalanche breakdown. Furthermore, this cause of breakdown is strengthened as L_{SG} decreases, leading to premature p+ base junction breakdown [22]. This is the main cause of the BFOM deterioration in the SG-DMOSFET. Figure 10 shows the electrostatic potential in the off state ($V_{DS} = 3000 \text{ V}$, $V_{GS} = 0 \text{ V}$). Unlike the SG-DMOSFET (Figure 10b), the FPS-DMOSFET in Figure 10c maintains a relatively low electrostatic potential at the center of the gate structure owing to the FPS. In other words, in the FPS-DMOSFET, the FPS mitigates this effect. Consequently, the concentrated drain voltage across the p + base junction is distributed. Therefore, the optimized FPS-DMOSFET has a BV very close to that of the SG-DMOSFET, although the L_{SG} (=0 μ m) is significantly lower than that of the SG-DMOSFET (0.7 µm).



Figure 8. Electron current density of (a) C-DMOSFET (conventional planar DMOSFET); (b) SG-DMOSFET (split-gate DMOSFET); and (c) FPS-DMOSFET (floating p+ polysilicon DMOSFET) in the on state ($V_{GS} = 20 \text{ V}$, $V_{DS} = 20 \text{ V}$).



Figure 9. Electron current density of (a) C-DMOSFET (conventional planar DMOSFET); (b) SG-DMOSFET (split-gate DMOSFET); and (c) FPS-DMOSFET (floating p+ polysilicon DMOSFET) in the on state ($V_{GS} = 20 \text{ V}$, $V_{DS} = 20 \text{ V}$).



Figure 10. Electrostatic potential of (**a**) C-DMOSFET (conventional DMOSFET); (**b**) SG-DMOSFET (split-gate DMOSFET); and (**c**) FPS-DMOSFET (floating p+ polysilicon DMOSFET) in the off state (V_{DS} = 3000 V, V_{GS} = 0 V).

Moreover, owing to the relatively low electrostatic potential of the FPS, the FPS-DMOSFET has a smaller E_{MOX} than the SG-DMOSFET. Figure 11 shows the electric-field distribution of the three structures with V_{DS} and V_{GS} set to 3000 V and 0 V, respectively. The SG-DMOSFET shows an E_{MOX} of 3.4 MV/cm owing to the electric-field crowding effect at the active gate corner. Consequently, the SG-DMOSFET does not guarantee the reliability of the gate oxide. On the other hand, the E_{MOX} of C-DMOSFET and FPS-DMOSFET is equal to 2.1 MV/cm. Therefore, the FPS-DMOSFET can guarantee gate-oxide reliability with the split-gate structure applied through FPS.



Figure 11. Electric field distribution of (**a**) C-DMOSFET (conventional planar DMOSFET); (**b**) SG-DMOSFET (split-gate DMOSFET); and (**c**) FPS-DMOSFET (floating p+ polysilicon DMOSFET) in the off state (V_{DS} = 3000 V, V_{GS} = 0 V).

3.3. Dynamic Characteristics

In the simulation of dynamic characteristics, the active area of the device under test (DUT) was set to 1 cm². Figure 12a,b show the capacitance graphs of the three structures. The capacitance simulation conditions were as follows: the AC small signal was set to 1 MHz, V_{GS} was fixed at 0 V, and V_{DS} was swept from 0 V to 1500 V. Figure 12a indicates that the FPS-DMOSFET exhibits the smallest C_{GD}. As mentioned earlier for the capacitance modeling, the FPS-DMOSFET has additional C_{GD} factors due to the FPS. However, the optimized FPS-DMOSFET has a smaller L_{SG} than the SG-DMOSFET, resulting in a smaller C_{GD}. In addition, because T_{S,OX} is sufficiently thick (=250 nm), additional C_{GD} factors due to the FPS are significantly eliminated. Similar to C_{GD}, the input capacitance (C_{ISS}) is a very important parameter because it affects the delay time in the switching cycle [23]. As shown in Figure 12b, the C_{ISS} values of the FPS-DMOSFET, SG-DMOSFET, and C-DMOSFET are 10.13, 11.82, and 12.37 nF/cm², respectively. This is because the gate–source capacitance (C_{GS}) decreases as L_{SG} decreases. Moreover, in Figure 12b, all three structures have almost the same output capacitance (C_{OSS}).



Figure 12. Capacitance curves of three structures extracted through simulation. (**a**) C_{GD} curve; (**b**) C_{ISS} and C_{OSS} curves.

Figure 13a shows the gate charges of the three structures. The test circuit is shown in Figure 13b, and a constant current of 100 mA was used to charge the gate. In addition, a supply voltage of 1700 V and a load current of 100 A were used to charge the gate of the test circuit. The total gate charge (Q_G) affects the delay time, and it is dependent on C_{ISS}. Moreover, Q_{GD} determines the switching power loss and it is dependent on C_{GD}. The extracted Q_{GD} values for the C-DMOSFET, SG-DMOSFET, and FPS-DMOSFET are 240.2, 131.1, and 102.8 nC/cm², respectively, while the extracted Q_G values are 894.1, 545.0, and 419.3 nC/cm², respectively.



Figure 13. (a) Gate Charge curves of three structures and (b) the test circuit for gate charge simulation.

Finally, switching parameters such as the turn-on time (T_{ON}), turn-off time (T_{OFF}), turnon energy loss (E_{ON}), and turn-off energy loss (E_{OFF}) are extracted through a double-pulse test simulation, and the results are summarized in Table 3. Figure 14a,b show the turn-off and turn-on transients of the double-pulse test simulation. In addition, the test circuit for the double-pulse test simulation is shown in Figure 14c. In this circuit, the external gate resistance and stray inductance were set to 10 Ω and 10 nH, respectively. The gate voltage was swept from -5 V to 20 V to switch between the off and on states. The supply voltage and load inductance were set to 1700 V and 170 μ H, respectively, and the first gate pulse was biased for 10 μ s; therefore, the load current was set to 100 A/cm². The body diode of the DUT was used as a freewheeling diode.

Parameter	C-DMOSFET	SG-DMOSFET	FPS-DMOSFET	Unit
C _{GD}	48.19	32.14	18.88	pF/cm ²
C _{ISS}	12.37	11.82	10.13	nF/cm ²
C _{OSS}	29.25	29.19	29.20.	nF/cm ²
QG	984.1	545.0	419.3	nC/cm ²
Q_{GD}	240.2	131.1	102.8	nC/cm ²
HF-FOM	754.7	574.7	295.7	$m\Omega imes pF$
T _{D,OFF}	608.7	359.5	236.6	ns
T _F	119.3	90.0	67.0	ns
T _{OFF}	728.0	449.5	303.6	ns
T _{D,ON}	35.1	31.7	28.3	ns
T _R	71.8	58.2	30.6	ns
T _{ON}	106.9	89.9	58.9	ns
Turn off dV _{DS} /dt	2.1	3.4	5.0	V/ns
Turn on dV _{DS} /dt	14.3	17.0	26.0	V/ns
E _{OFF}	9.53	6.65	5.20	mJ/cm ²
E _{ON}	5.44	4.11	3.31	mJ/cm ²

Table 3. Dynamic characteristics of three structures.



Figure 14. The switching waveforms of three structures extracted by double pulse test simulation. (a) drain voltage and gate voltage waveforms; (b) drain voltage and drain current waveforms; and (c) the test circuit for double pulse test simulation.

In this paper, T_{ON} and T_{OFF} are defined as follows [24]:

$$T_{ON} = T_{D,ON} + T_R \tag{6}$$

$$T_{OFF} = T_{D,OFF} + T_F \tag{7}$$

where $T_{D,ON}$ is the turn-on delay (from 10% of V_{GS} to 90% of V_{DS} at the rising edge of the second pulse), T_R is the rise time in the turn-on transient (from 90% to 10% of V_{DS} at the rising edge of the second pulse), $T_{D,OFF}$ is the turn-off delay (from 90% of V_{GS} to 10% of V_{DS} at the falling edge of the first pulse), and T_F is the fall time in the turn-off transient (from 10% to 90% of V_{DS}). As a result, FPS-DMOSFET with C_{ISS} has the fastest T_{ON} and T_{OFF} as 71.1 ns and 310.9 ns, respectively.

In addition, Figure 15 shows the extracted total switching energy loss ($E_{TOTAL} = E_{ON} + E_{OFF}$) of the three structures. Due to the smallest C_{GD} , FPS-DMOSFET has the E_{ON} of 3.31 mJ/cm² and E_{OFF} of 5.20 mJ/cm², so that E_{TOTAL} is 8.51 mJ/cm², which decrease by 43% and 21%, respectively, compared to C-DMOSFET and SG-DMOSFET.



Figure 15. The switching power loss of three structures extracted by double pulse test. (a) turn off transient and (b) turn on transient.

4. Conclusions

In this paper, an SG-DMOSFET with floating p+ polysilicon (FPS-DMOSFET) was proposed and analyzed in comparison with a C-DMOSFET and a SG-DMOSFET through TCAD simulations. The FPS-DMOSFET shows a shorter L_{SG} with significantly less BFOM degradation than the SG-DMOSFET because the proposed structure has FPS between the active gates, forming an accumulation layer in the on state and dispersing the high drain voltage due to the relatively low potential in the off state. As a result, the HF-FOM of the FPS-DMOSFET is improved by 61% and 49%, respectively, compared to the C-DMOSFET and SG-DMOSFET. Therefore, the FPS-DMOSFET not only has the fastest T_{ON} and T_{OFF} , but also the smallest E_{ON} and E_{OFF} during the switching operation. Moreover, the FPS-DMOSFET has an E_{MOX} of 2.1 MV/cm, which is lower than that of the SG-DMOSFET (3.4 MV/cm) and the same as that of C-DMOSFET. This implies that the FPS-DMOSFET can guarantee reliable operation. Therefore, FPS-DMOSFETs can significantly improve HF-FOM while solving serious problems in SG-DMOSFETs, such as BFOM degradation and a high E_{MOX} at high voltages.

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