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Reconfiguration Strategy for Fault Tolerance in a Cascaded Multilevel Inverter Using a Z-Source Converter

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Abstract: The cascade multilevel inverters are widely used in industrial manufacturing processes for DC-AC conversion. Therefore, the reliability and efficiency improvement, optimized control, and fault-tolerant strategies are areas of interest for researchers. The fault tolerance strategies applied to cascade multilevel inverters are classified as material redundancy and analytical redundancy. This paper presents the use of the Z-source converter as a fault reconfiguration method applied to a cascade multilevel inverter. On the one hand, the proposed approach has the characteristic of combining the use of material redundancy (modifying the output voltage by changing the Z-source operation), and on the other hand, it has the use of analytical redundancy (modifying the switching sequence of the multilevel inverter, changing from symmetrical to asymmetrical operation mode). This approach has been validated by experimental results of the system under fault-free conditions and employing the Z-source converter as the main fault reconfiguration element. The proposed fault reconfiguration strategy allows the cascaded multilevel inverter to continue to operate even in the presence of a fault by having continuous operation.

Keywords: fault tolerance; inverter; power system fault; Z-source converter; multilevel inverter

1. Introduction

The cascade multilevel inverters (CMLI) are widely used in industrial manufacturing processes for DC-AC conversion for several advantages compared to a two-level inverter, such as including the ability to higher voltage stress due to their cascaded structure, lower common-mode voltage, and lower Total Harmonic Distortion (THD) [1]. Among the disadvantages of the CMLI are complex control strategies and a larger number of semiconductor devices. The increased number of power semiconductor devices in CMLI increases the risk of failures, since the failure of a single device could cause the whole inverter to fail.

The most usual faults that may occur in the CMLI are open- and short-circuit faults in power semiconductor devices as well as the loss of gate pulse signals (control failure) such as those shown in Figure 1 [2]. The control failure could be considered as an open-circuit fault in the power semiconductor devices and thus, the main faults are open- and short-circuit faults.

If an open-circuit fault occurs in the CMLI, the loss of one or several voltage levels could occur. If a short-circuit fault happens, the short circuit circulation path could cause

extra electrical stress on the power semiconductor devices (thermal fatigue) or a short-circuit condition on the source side, which results in further damage [3,4].

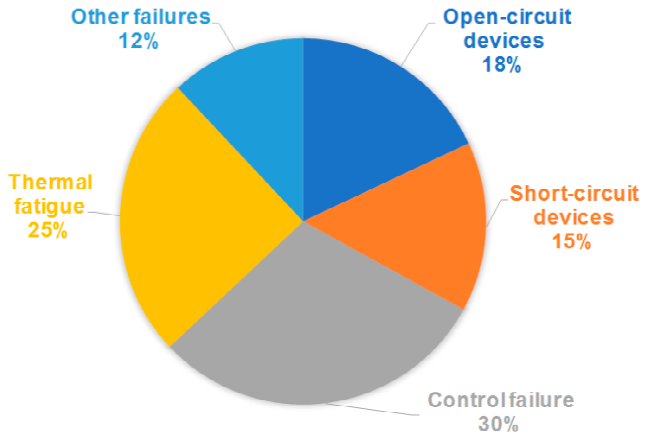

Figure 1. Pie diagram of failure distribution in power semiconductor devices.

When a fault occurs in the CMLI, the failed component should be diagnosed and located for possible recovery. However, the large variety of power converter topologies and structures, as well as a large number of power semiconductor devices in the CMLI, could cause ambiguous conditions that impede the fault diagnosis. This issue has attracted significant research interest to yield effective fault-tolerant strategies. To detect the faults in the CMLI, various fault diagnostic methods have been developed [5,6].

The fault tolerance strategies applied to CMLI are classified as material redundancy and analytical redundancy, and they are briefly described below.

1.1. Material Redundancy

This type of redundancy involves having extra elements to replace the damaged elements. Making use of this redundancy allows systems to isolate the fault and continue to operate in degraded conditions. In references [7–9], material redundancy is used by connecting an auxiliary branch in parallel to the converter; when a short-circuit fault occurs in any of the circuit breakers, this auxiliary branch is activated, replacing the damaged branch. Similarly, in reference [10], bidirectional switches are used on each cell of the CMLI, which are directly connected to transformers with a different ratio in each of their windings.

For material redundancy, it is necessary to use high-speed electronic devices to detect and replace the damaged branch. Therefore, it is necessary to have efficient sensing systems, since an unbalance in the sensed voltages can cause the disconnection of one or more elements in a fault-free condition.

1.2. Analytical Redundancy

Analytical redundancy is also referred to as software redundancy. It consists of the incorporation of an additional block in the control system capable of reconfiguring the output signals of the system using feedback of these signals [11]. Employing this type of redundancy allows the system to continue to operate even after a fault has occurred, operating with degradation in its output signals without adding extra devices to the system circuitry, reflecting a decrease in its implementation costs [12].

In reference [13], the PWM signal re-assignment technique is used in the CMLI; this strategy bases its operating principle on the comparison of high-frequency carrier signals with a low-frequency modulating signal generating switching pulses that control the full-bridge switches of the CMLI. The modularity characteristic of these systems is used to perform a re-accommodation of their control signals even after a failure of one of the cells of the complete bridge.

This paper presents the use of the Z-source converter as a fault reconfiguration method applied to a CMLI. The proposed approach combines the modification of the output voltage due to a change in the Z-source converter operation, and it modifies the switching sequence of the multilevel inverter, allowing the change from symmetrical to an asymmetrical operation mode. The proposed fault reconfiguration strategy in this paper allows the CMLI to remain in operation even in the presence of a fault in any cell of the CMLI (only one fault at a time). In addition, the THD value obtained is within the values established in the IEEE 519 standard.

The rest of the paper is organized as follows: Section 2 presents the description of the cascaded multilevel inverter. Section 3 describes the design equations of the Z-source converter, as well as the two operating states. Subsequently, Section 4 presents the description of the proposed reconfiguration technique. Section 5 shows the experimental results obtained from the behavior of the cascaded multilevel inverter without faults and with faults by applying the proposed method. Finally, the conclusions of this document are found in Section 6.

2. Multilevel Inverter

The main function of the CMLI is to synthesize the output AC voltage from a DC voltage level at the input, which can be connected in series or cascade, summing the voltages. CMLI includes an array of power semiconductor devices and capacitor or DC voltage sources that generate step-waveform output voltages. Multilevel technology started with the three-level converter; then, it was followed by numerous multilevel inverter topologies. By increasing the number of levels in the inverter, the output voltage has more steps generating a staircase waveform, which has a reduced THD value. However, a high number of levels increases the control complexity and introduces voltage unbalance problems [14].

The CMLI depending on the power supply can be symmetrical or asymmetrical.

2.1. Symmetrical Cascaded Multilevel Inverter (S-CMLI)

The symmetrical CMLI (S-CMLI) consists of "S" cells connected in series, which are powered by isolated DC sources. Their number of levels is defined by the following equation:

$$L = 2S + 1 \tag{1}$$

where L is the number of output voltage levels and S is the number of H-bridge cells with their respective DC source.

Figure 2 shows the CMLI for three H-bridge cells and seven-level output voltage.

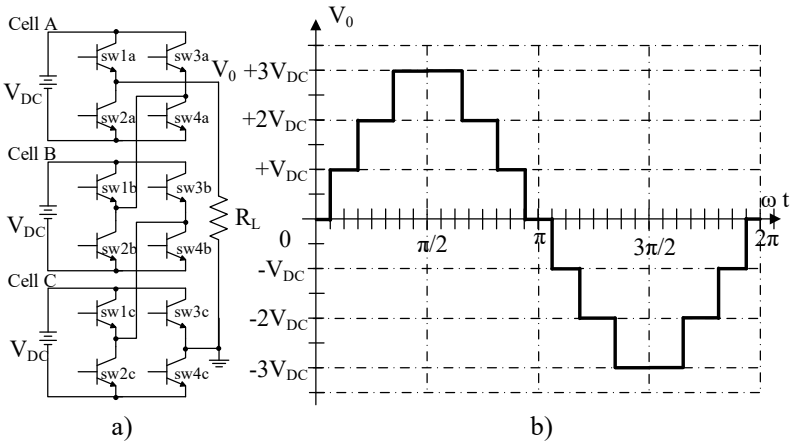

Figure 2. (**a**) Diagram of symmetrical cascaded multilevel inverter with a seven-level, single-phase structure. (**b**) Output voltage waveform.

2.2. Asymmetrical Cascaded Multilevel Inverter (A-CMLI)

The asymmetrical CMLI (A-CMLI) is a modification of the conventional topology of the multilevel inverter (S-CMLI), being differentiated only by the voltage ratio applied to the power supplies of each of the cells. A-CMLI generates more levels in the output waveform with fewer cells compared to other multilevel topologies [15]. There are two A-CMLI structures: (a) Binary (power of 2) in which the supply voltage of each cell is doubled consecutively, and (b) Trinary (power of 3) in which the supply voltage of each cell is tripled consecutively [16] and [17].

$$L = 2^{s+1} - 1 \tag{2}$$

where L is the number of output voltage levels and S is the number of H-bridge cells with their respective DC source.

Figure 3 shows the A-CMLI for two H-bridge cells and a seven-level output voltage. Comparing Figures 2b and 3b, seven levels of the output voltage waveform are observed for both cases: three cells (symmetrical) and two cells (asymmetrical). This is possible only by making modifications to the switching sequence of the cells and duplicating the supply voltage of one of the cells. The above describes the main idea of the reconfiguration technique when a fault occurs in one of the cells that compose the CMLI.

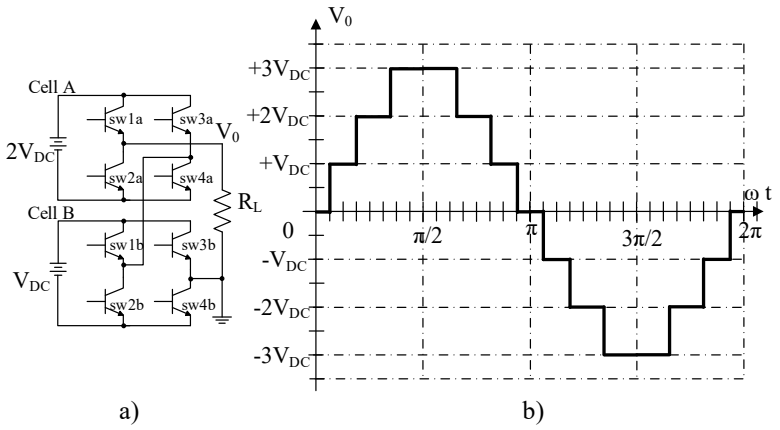

Figure 3. (**a**) Diagram of asymmetrical cascaded multilevel inverter with a seven-level, single-phase structure. (**b**) Output voltage waveform.

3. Z-source Inverter

The Z-source inverter (ZSI) also known as the Z-impedance network, emerged as a DC-AC power converter in 2002 introduced by Peng [18]. The ZSI in conjunction with the three-phase bridge configuration type [19] allows the inverter to increase the output voltage using only one conversion stage, as shown in Figure 4.

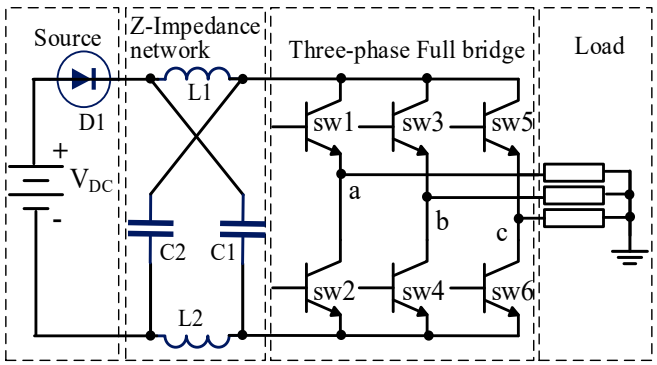

Figure 4. Electrical diagram of a three-phase full-bridge Z-source inverter.

The ZSI uses an impedance network at the input consisting of the inductors (*L*1 and *L*2) and the capacitors (*C*1 and *C*2), as shown in Figure 4. The capacitors are connected diagonally, and in conjunction with the inductors, they form a second-order filter that operates as energy storage. This allows increasing the voltage with an optimal design using components with low capacitance and inductance values, reducing the implementation cost [20].

The operating principle of ZSI depends on the switching states of the inverter connected to it.

3.1. Z-Source Converter

We replace the three-phase full-bridge of the Z-source inverter (shown in Figure 4) with a switch named Q1, which is controlled by the trigger signal "D" generated by the "Simple Boost" method. Therefore, the Z source is used as a DC-DC converter switched to high frequency and with increased dynamic speed. Figure 5 shows the simplified diagram of the Z-source converter.

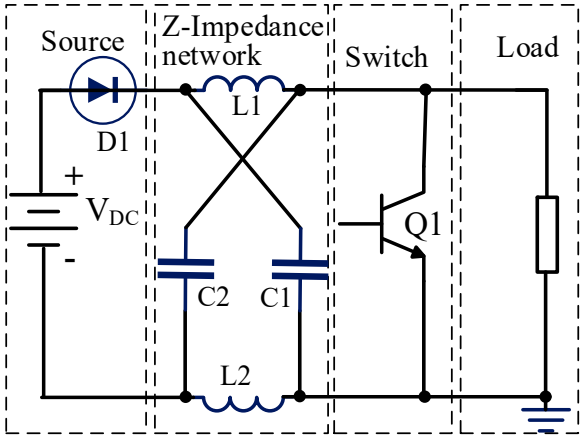

Figure 5. Electrical diagram of Z-source converter.

The Z-source converter, similar to the ZSI, operates on the same principles as the NST (Non-Shoot-Through) and ST (Shoot-Through) switching states.

3.2. NST State in Z-Source Converter

During the NST status, switch Q1 is turned off by connecting to the impedance network with the load, as shown in Figure 6.

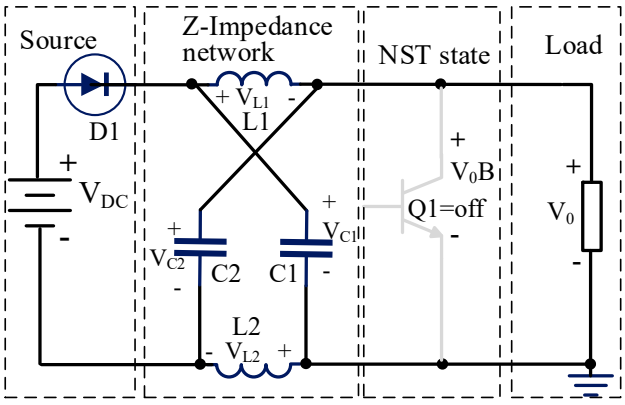

Figure 6. Electrical diagram of Z-source converter in the Non-Shoot-Through (NST) state.

The D1 diode is directly polarized, so the $L1$ and $L2$ inductors together with the V_{DC} power supply charge the $C1$ and $C2$ capacitors:

$$V_{DC} = V_{C1} + V_{L2} \tag{3}$$

Where V_{C1} is the voltage of the capacitor $C1$, and V_{L2} is the voltage of the inductor $L2$. Where V_0B is the short-circuit output voltage:

$$V_{L2} = V_{C2} - V_0B \tag{4}$$

Substituting Equation (4) in (3):

$$V_0B = -V_{DC} + V_{C1} + V_{C2} \tag{5}$$

Since the voltages $V_{C1} = V_{C2} = V_C$ are equal, the following expression is given:

$$V_0B = 2V_C - V_{DC} \tag{6}$$

3.3. ST State in Z-Source Converter

During the ST state shown in Figure 7, switch Q1 is activated (turn-on), short-circuiting the output. Capacitors $C1$ and $C2$ are connected in parallel with the inductors and in series with the diode and power supply V_{DC}, polarizing the D1 diode in reverse, so the capacitors charge to the inductors.

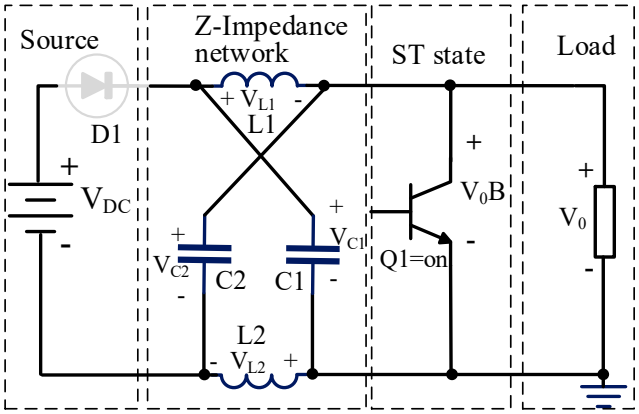

Figure 7. Electrical diagram of Z-source converter in the Shoot-Through (ST) state.

In Figure 7, the expressions can be deduced:

$$V_{L1} = V_{C1} \tag{7}$$

$$V_{L2} = V_{C2} \tag{8}$$

$$V_0 = V_0B = 0. \tag{9}$$

When performing an energy balance on the inductor, in a steady state, the average voltage of the inductors during a complete period is zero. Here, we are using the expression $T_S = t_{ST} + t_{NST}$, where t_{ST} is the time in ST state and t_{NST} is the time in NST state.

$$V_L(t)_{ST} = \frac{1}{T_S}[t_{NST}(V_{DC} - V_C) + t_{ST}V_C] \tag{10}$$

where

$$D = \frac{t_{ST}}{T_S};\ (1 - D) = \frac{t_{NST}}{T_S}. \tag{11}$$

Substituting Equation (11) in (10) gives the following expression:

$$V_L(t)_{ST} = \frac{1}{T_S}[T_S(1-D)(V_{DC}-V_C) + T_S D V_C] = 0 \tag{12}$$

$$\frac{V_C}{V_{DC}} = \frac{1-D}{1-2D}. \tag{13}$$

Since $V_C = V_O$, the input–output ratio of the Z source converter is determined by:

$$G = \frac{V_C}{V_{DC}} = \frac{1-D}{1-2D} \tag{14}$$

where G is the Z-source converter gain as a function of the duty cycle D. Since $L1 = L2$, the average currents and voltages are identical in both elements. The value of the inductors is linked to the permitted current ripple level Δ_{iL}, and this influences the peak stresses of the power semiconductor devices.

From the following equation:

$$v(t) = L\frac{di}{dt}, \tag{15}$$

the following is deduced:

$$L = \frac{v(t)}{dt}dt \tag{16}$$

For the times of the ST and NST states, fs must be the frequency of operation of the converter, $di = \Delta_{iL}$, and $v(t)$ is the voltage applied to the inductor to be analyzed. The value of the inductor is calculated with the following expressions:

$$L_{ST} = \frac{V_0 D}{f_s \Delta i_L} \tag{17}$$

$$L_{NST} = \frac{(V_0 - V_{DC})(1-D)}{f_s \Delta i_L} \tag{18}$$

To determine the value of the capacitor, the following equation is used:

$$i(t) = C\frac{dv}{dt} \tag{19}$$

where $dv = \Delta_{VC}$ and $i(t)$ is the current applied to the capacitor. The capacitor values for the times of the ST and NST states can be calculated with:

$$C_{ST} = \frac{I_{in} D}{f_s \Delta v_C} \tag{20}$$

$$C_{NST} = \frac{(I_{in})(1-D)}{f_s \Delta v_C}. \tag{21}$$

4. Fault Reconfiguration Technique

The reconfiguration technique is based on changing the operating mode of the CMLI from symmetrical to asymmetrical mode. For this purpose, it is necessary to identify the faulted cell to deactivate it and assign the modulation sequence to the remaining fault-free cells.

It is important to emphasize that for the technique proposed here, the nature of the fault does not matter (open circuit or short circuit), because the fundamental principle of the technique is the deactivation of the entire cell. However, it is necessary to point out that this proposal is limited to the fault in a single cell; if there are faults in two or more different cells, this reconfiguration technique cannot be applied.

Figure 8 shows the Z-source converter in conjunction with the single-phase seven-level CMLI. This converter is designed to perform a reconfiguration (S-CMLI to A-CMLI) by changing operation in the presence of a fault (fault condition) in one of the three full-bridge cells that conform to the system, changing its output voltage from V_{DC} to double value ($2V_{DC}$).

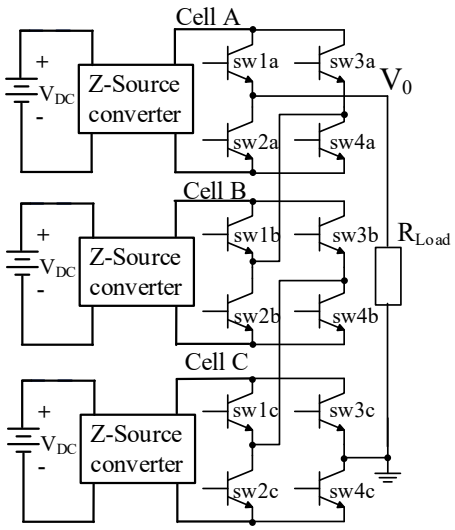

Figure 8. Combination of cascade multilevel inverters (CMLI) with the Z-source converter, used for reconfiguration purposes.

Figure 9 shows the flow chart of the methodology used; it is worth mentioning on the one hand that the modifications of the inverter operation from symmetrical to asymmetrical form are made by the cells that compose the multilevel inverter (analytical redundancy), and on the other hand, the variation of the output voltage of the Z source is carried out through the variation of the duty cycle of the gate signal of the semiconductor device that composes the Z source (material redundancy).

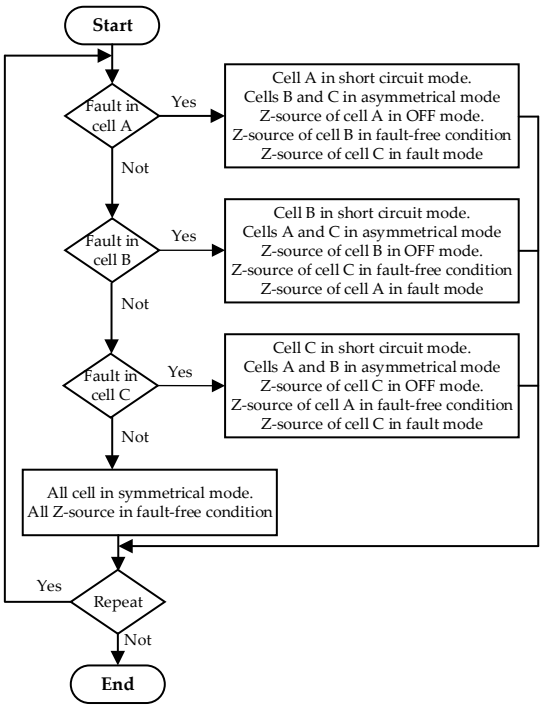

Figure 9. Flowchart of the methodology used.

Table 1 presents the possible cases of faults analyzed in this paper and the sequence to follow when a fault occurs in a single cell of the CMLI. The goal is to maintain an energy balance; therefore, the duty cycle of the fault-free cells is modified.

Table 1. Possible cases of CMLI with fault tolerance.

Condition	Cell A	Cell B	Cell C
Fault-free	CMLI in symmetric mode. Z-Source in fault-free condition.	CMLI in symmetric mode. Z-Source in fault-free condition.	CMLI in symmetric mode. Z-Source in fault-free condition.
Fault in Cell A	CMLI in short-circuit mode. Z-Source in OFF mode.	CMLI in asymmetric mode. Z-Source in fault-free condition.	CMLI in asymmetric mode. Z-Source in fault mode.
Fault in Cell B	CMLI in asymmetric mode. Z-Source in fault mode.	CMLI in short-circuit mode. Z-Source in OFF mode.	CMLI in asymmetric mode. Z-Source in fault-free condition.
Fault in Cell C	CMLI in asymmetric mode. Z-Source in fault-free condition.	CMLI in asymmetric mode. Z-Source in fault mode.	CMLI in short-circuit mode. Z-Source in OFF mode.

5. Experimental Results

Table 2 shows the values of the design parameters of the Z-source inverter, which are divided into fixed and variable values. Variable values change according to the operating condition that can be fault-free condition or fault condition. When a fault occurs in any cell (open circuit fault) in the multilevel converter, the Z source provides twice the output voltage for the multilevel converter modulation to be modified, changing from symmetrical to asymmetrical operating mode.

Table 2. Z-source converter design parameters.

Figure Parameter	Value	
V_{DC}	38 V	
$C1$ & $C2$	2.2 µF	
$L1$ & $L2$	1 mH	
R_{LOAD}	64 Ω	
L_X	1 mH	
C_X	1 µF	
f_s	100 kHz	
Variable Parameter	**Fault-Free Condition (Nominal)**	**Fault Condition**
V_0	40 V	80 V
P_0	25 W	100 W
D	0.048	0.344
Δi_L	0.02 A	0.25 A
ΔV_C	0.15 V	4 V

5.1. Experimental Prototype of the Z-Source Converter

The converter design was implemented in the laboratory to verify its performance. Table 2 lists the electrical parameters of the components used in the implementation. The details are as follows:

- Diode D1: HFA15TB60 (Ultrafast Diode), rated at 15 A, 600 V (International Rectifier, El Segundo, CA, USA)
- MOSFET Q1: IRFP350, rated at 10 A, 400 V (Vishay Siliconix, Santa Clara, CA, USA)
- Inductors $L1$ and $L2$: model 1140-102K-RC, 1 mH/5.5 A (Bourns, Jalisco, Mexico)

Figure 10 shows the experimental implementation of the Z-source converter, which was designed from the values in Table 2.

Figure 10. Electrical components of the experimental implementation of the Z-source converter.

5.2. Z-source Converter Behavior in Transient Mode

The results obtained experimentally are shown in Figure 11, showing the transition from fault-free condition to fault condition. A transient with a duration of 1.624 ms is presented, with a positive peak voltage of 90 V and a minimum voltage of 28.50 V.

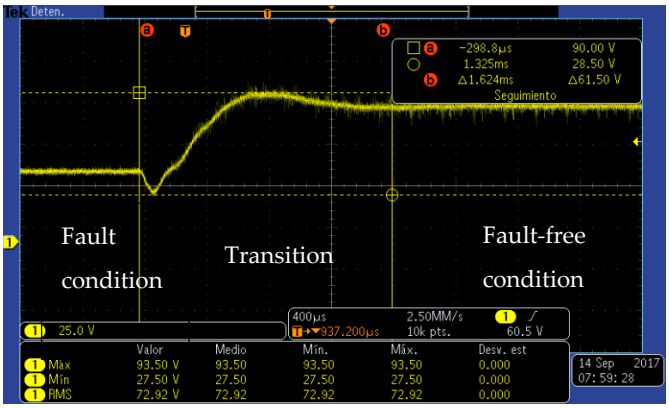

Figure 11. Oscillogram of the transient state of Z-source converter, during its operation change.

5.3. Multilevel Inverter Behavior in the Fault-Free Condition

The CMLI design was implemented in the laboratory to verify its performance. The electrical parameters of the components used in the implementation are briefly described below:

- Cells A, B, and C: Experimentally built with power modules IRAMS10UP60 (International Rectifier, El Segundo, CA, USA) (These power modules produce a short circuit in the output terminals when any fault occurs in the semiconductor power switches that compose it [21]), rated at 10 A, 600 V (Integrated gate drivers and bootstrap diodes).
- Optocouplers circuit: A2611 (Fairchild Semiconductor, CA, USA) (The internal shield provides a guaranteed common mode transient immunity specification up to 15,000 V/µs at 1000V).

Figure 12 shows the experimental implementation of a CMLI cell with its drive circuit.

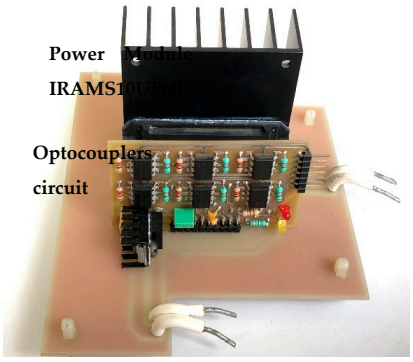

Figure 12. Electrical components of the experimental implementation of a CMLI cell with its drive circuit.

Three 40 V full-bridge cells with three isolated DC power supplies and the Z-source converter were used in the experimental testing stage of the single-phase seven-level CMLI. Figure 13 shows the CMLI operating in fault-free condition, displaying a symmetrical seven-level stepped response.

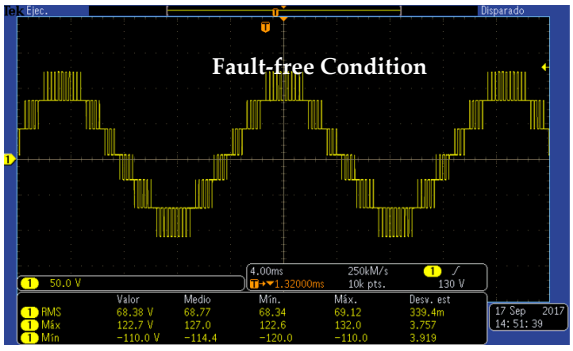

Figure 13. Oscillogram of the seven-level cascade multilevel inverter output voltage waveform in fault-free condition.

Figure 14 shows the screenshot of the power quality analyzer, showing the harmonic content of the seven-level symmetrical CMLI output voltage in a fault-free condition. The total harmonic content for the fault-free condition is THD = 5.36% at a frequency of 59.868 Hz, complying with the IEEE 519 standard, which specifies that the maximum total harmonic content permissible is THD = 8%.

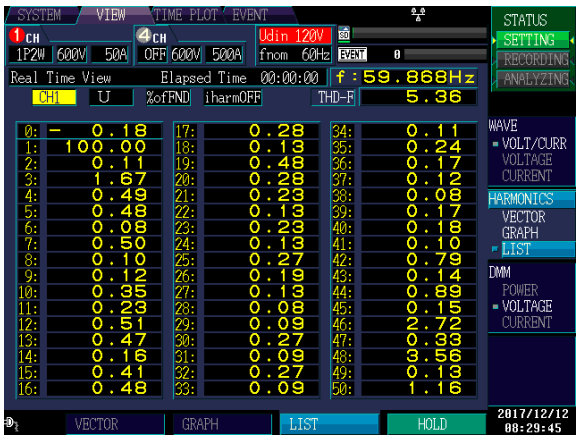

Figure 14. List of Total Harmonic Distortion (THD) value of the CMLI in the ideal case (power supplies of equal value).

5.4. Multilevel Inverter Behavior from the Fault-Free Condition to the Fault Condition (Degraded Response)

A fault is introduced into the CMLI (in cell "A"), producing a change from a fault-free condition to a fault condition. Therefore, cell "A" is disconnected from the system, resulting in the loss of two voltage levels (one at the top and one at the bottom), presenting a five-level output voltage waveform with a degraded response. Figure 15 shows the five-level voltage waveform obtained.

5.5. Multilevel Inverter Behavior during Fault Condition: Degraded Response Change to Reconfiguration

The Z-source converter (Figure 8) into the CMLI "cell C" produces a change of operation in CMLI from symmetrical to asymmetrical. Therefore, at a time t = 0, the Z-source converter provides a seven-level voltage waveform (as presented in the fault-free condition) of the inverter, as shown in Figure 16.

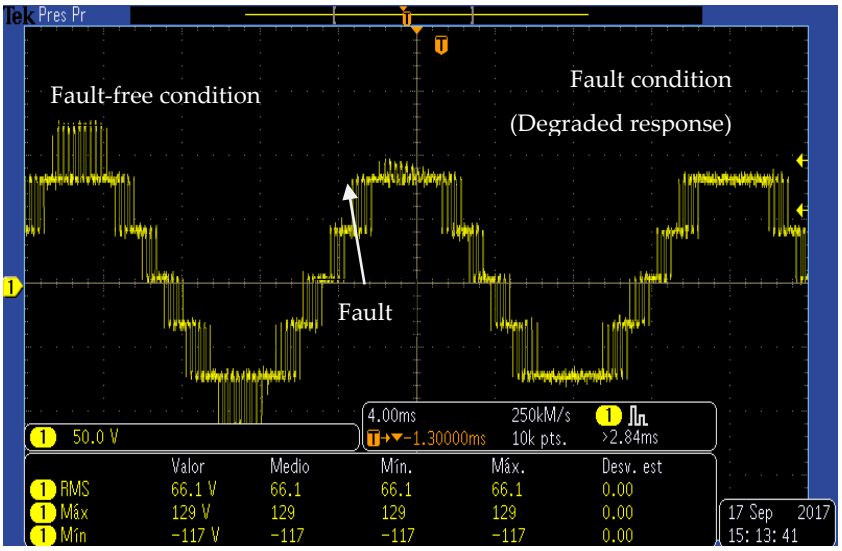

Figure 15. Oscillogram of the output voltage waveform behavior during the change from the fault-free condition to the fault condition (degraded response).

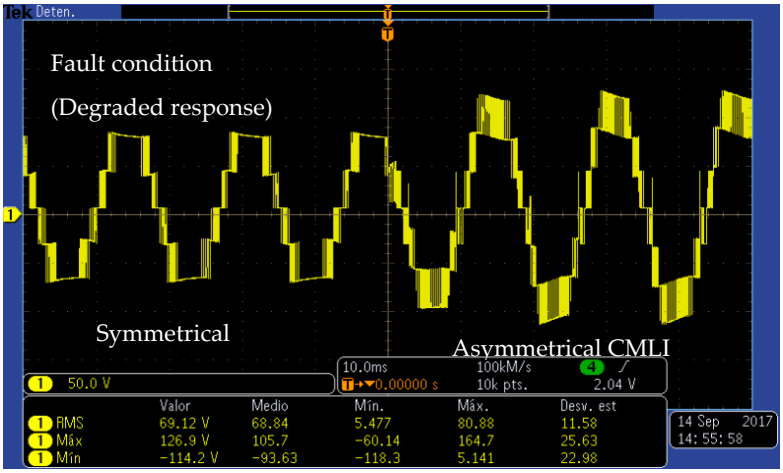

Figure 16. Oscillogram of the output voltage waveform behavior during fault condition: degraded response change to reconfiguration.

5.6. Multilevel Inverter Behavior from the Fault-Free Condition to the Fault Condition (Reconfiguration)

Figure 17 shows the output voltage waveform of the inverter operating in fault-free condition; at instant t = 0, the reconfiguration of the inverter operation is performed, changing from symmetrical to asymmetrical mode. Therefore, a transient state is observed during the change from the fault-free condition to the fault condition.

During the fault condition, the damaged cell of the inverter is automatically short-circuited, and the CMLI is reconfigured (in less than 60 Hz, cycle time = 16.66 ms). The CMLI operated in a degraded regime for a period t < 2 ms.

Figure 18 shows the screenshot of the power quality analyzer, showing the harmonic content of the seven-level asymmetrical CMLI output voltage in a reconfigured fault condition, using the Z-source converter, presenting a THD value = 8.23% at a frequency of 59.868 Hz. Therefore, it can be concluded that by reconfiguring the fault-free condition to fault condition, the output voltage signal increases from a THD value of 5.36% to 8.23%.

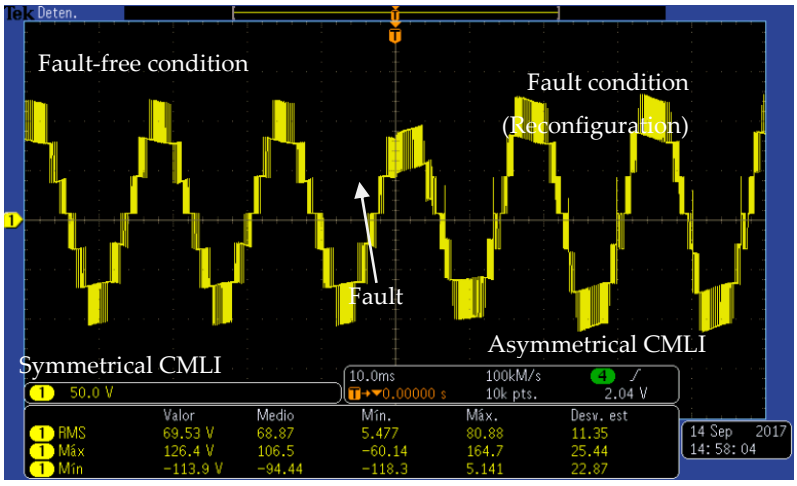

Figure 17. Oscillogram of the output voltage waveform behavior during the change from the fault-free condition to the fault condition (Reconfiguration).

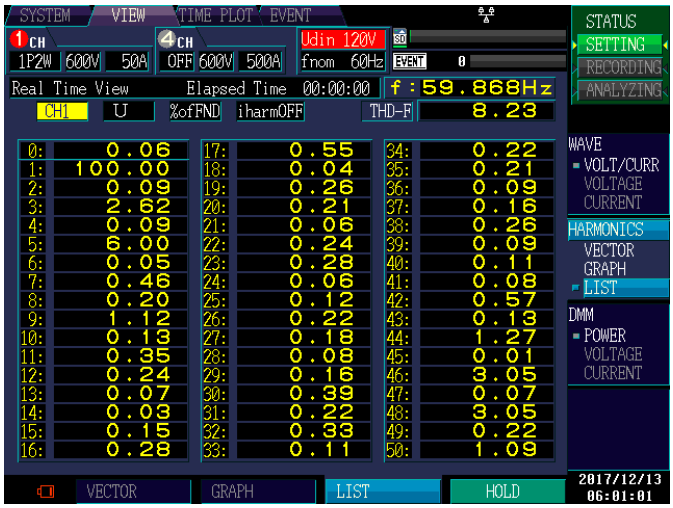

Figure 18. List of THD value of the seven-level asymmetrical CMLI in a reconfigured fault condition.

The speed of response of the Z-source converter allows a reconfiguration in the CMLI in a t < 2 ms. Therefore, if a random failure occurs during the sine wave period, the Z-source converter is capable of restoring the signal, without having phase shift problems, and without negative effects on the output signal cycles.

6. Conclusions

This paper presented the use of the Z-source converter as the main element of fault reconfiguration applied to a seven-level CMLI. The proposed approach combines the modification of the output voltage of the Z-source converter (mathematical redundancy) and the switching sequence of the multilevel inverter (analytical redundancy). Therefore, this combination allows the system to operate symmetrically when the system is in a fault-free condition and asymmetrically when only one fault condition occurs in any of the inverter cells.

The proposed fault tolerance strategy allows the system to operate continuously even when a fault occurs in one of the full-bridge power cells. The strategy allows the CMLI to provide a balanced voltage waveform, even though only two of the three initial power cells operate. This was achieved by performing an operation change on the Z-source converter and using a hybrid modulation technique.

By separating the Z source from the full-bridge inverter stage (single-phase or three-phase) and using it as a DC-DC converter, the Z-source converter can be operated at high frequency (100 kHz). Therefore, the switching frequency is no longer limited by the IGBTs used in the CMLI, and the dynamic response of the inverter is around 2 ms. This allows the output voltage value to be doubled when a change in operation occurs in the presence of a fault (fault condition). In contrast, the applications where the Z source is connected directly to the inverter exhibit a dynamic response with a duration of about 250 ms.

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