

Review

Trends and Challenges in Multi-Level Inverter with Reduced Switches

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Abstract: Multilevel inverter had been paid a lot of attention from the academia and research community in recent times due to its role in high and medium power applications. In this paper, a detailed survey is made on the recently designed multilevel inverter to find the suitability of the inverters for particular applications. Research is performed on various types of multilevel inverters such as: Symmetric, asymmetric, hybrid and modularized multilevel inverter in order to identify the issues in generating more levels at the output. A summary of various issues in multilevel inverter with reduced switch count is provided, so that a novel topology of multilevel inverter can be designed in future. Further, an 81-level switched ladder multilevel inverter using unidirectional and bidirectional switches is designed. Simulation work is carried out using Matlab/Simulink in order to validate the performance of the inverter with change in resistive load and impedance load. The output of the 81-level inverter is fed to a 110 V, 186.5 W single phase induction motor in order to study the characteristics, further speed control of motor is performed by varying the input voltage of the motor and the results are presented.

Keywords: cascaded unit; 81-level; induction motor; ladder circuit; multilevel inverter; pulse generation



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1. Introduction

Nowadays, multilevel inverters (MLI) play a major role in various power applications such as Electric Vehicle [1], Photovoltaic systems [2], Low-Power Loads [3], Grid integration system [4]. It is more attractive because of very low harmonic distortion, low number of drivers, absence of filters, low installation area, reduction in voltage stress and switching losses.

A generalized cascaded multilevel inverter is presented with nearest level modulation technique. The proposed converter is discussed with and without half bridge circuits [2]. A new multilevel inverter with one DC source is presented for low power applications. The proposed inverter generates the output voltage eight times higher than the input voltage [3]. In [4], various configurations of MLI's were analyzed in terms of number of switching devices and modulation techniques. MLI are broadly classified into cascaded H Bridge, neutral clamped and flying capacitor topologies [5].

Recently, for hybrid systems cascade multilevel inverters are applied. Many topologies are there to create the staircase voltages with higher levels with low devices count [6]. A new MLI is designed to generate generate 27-level and fifty one level output voltages using constant voltage sources for resistive-inductive load [7]. An inverter is designed using trinary DC sources and thirteen switches to generate 53 output levels with minimum THD of 1.15% [8]. A new switched source MLI is proposed which operates under both symmetric

and asymmetric mode. The proposed inverter is designed with six power switches and two voltage sources [9]. A new 81-level MLI is presented using two stage ladder circuits and the values of the dc sources are fixed by two different algorithms. The presented topology is tested with resistive and impedance load [10]. A cascaded MLI is presented to generate 9, 15, 27, 33 and 39 output voltage levels at the load. It is observed that increase in number of voltage levels reduces the presence of harmonic content in load voltage and current waveforms. The proposed inverter is simulated in Matlab/Simulink and analyzed the total harmonic distortion for resistive and resistive-inductive load [11]. Various configurations of symmetrical, asymmetrical and hybrid MLI's were synthesized in terms of number of switches, capacitors, diodes utilized in the inverter circuit. As well, an analyzes is made in terms of THD generation and total standing voltages of all the configurations [12]. Few drawbacks such as: switch count, voltage imbalance and number of DC sources are there in all the topologies [13].

Multilevel inverter with minimum switch count is focused nowadays with higher voltage levels [14]. Higher voltage levels are attained using cascaded H bridge MLI with isolated DC voltage sources. The switch count reduction is based on the design of basic unit. MLI with three phase is proposed with reduced power switches and has attained nine output voltage levels. The proposed structure is analyzed for various pulse width modulation (PWM) techniques. Total harmonic distortion is examined for all the PWM techniques [15].

A new optimized structure of MLI is designed to create a rectangular type and circular type with a smaller number of switching components. A new switching technique is adopted and it is validated through simulation and experimental studies [16]. A three phase cascade H bridge (CHB) inverter is proposed with discontinuous pulse width modulation which reduces switching losses and thus increases the lifetime of the switches. MLI also adopted with rotation scheme for even distribution of power in the switches [17]. A trinary CHB MLI is proposed for solar power system with equal number of voltage levels.

For the control of active power and grid interaction, a modified second order integral control is applied [18]. The space vector pulse width modulation scheme is being applied to the MLI for common mode voltage reduction [19]. Two new MLI structures are designed and interfaced with PV system. Both the MLI structures consists of equal number of power switches and generates 9-level output [20].

This paper consists of six sections including introduction. Section 2 discussed about the survey on multilevel inverter with reduced switch (MLIRS) designs, Section 3 discussed the issues related with the construction of MLIRS, Section 4 discussed proposed MLI topology, design parameters of switched ladder inverter and generation of 81-levels and Section 5 presented pulse generation logic and analysis of results.

2. Survey on MLIRS Designs

For a medium voltage high power single phase application, a fifteen level inverter is designed using three DC sources and ten switches. Further, the design topology is modified to generate 25-levels at the output using four DC sources and twelve switches. By comparing the two inverter design, the extended topology utilized fewer switches to generate more output levels. Nearest level control method is applied to generate pulse for the switches and this inverter works with symmetrical and asymmetrical configurations [21].

To attain the speed torque characteristics of AC motor under loaded conditions, a seven level inverter is designed using seven power switches and three voltage sources. The advantages of using this inverter in medium voltage drives are reduction in the size of filter and low voltage stress [22].

A 17-level inverter is designed using unidirectional and bidirectional switches with four asymmetric sources which varies in trinary fashion. The designed topology is tested with impedance load and found to be usage of minimum number of switches to generate more output levels [23].

A 17-level inverter with reduced power switches for open end induction motor drives is proposed. A level shifted carrier scheme is applied for v/f and d/q control for induction motor drives. The circulating power is analyzed and eliminated by space vector analysis. The proposed topology is suitable for traction and induction motor drive application [24].

A multilevel inverter is proposed with fuel cell and attains high output levels. Using MATLAB simulation is completed with less power electronic switches to obtain output voltage levels such as: 5, 7 and 15-levels. Through mathematical calculation efficiency and power loss is analyzed. Switching loss, device stress and driver circuits are compared with other multilevel inverter topologies [25].

A 9-level and 49-level multilevel inverter is proposed and simulated [26]. The basic structure consists of two voltage sources and five switches. The harmonic distortion achieved for a 9-level inverter is 9.85% and for a 49-level inverter is 2.01%, it is found that increase in output voltage levels leads to reduction in harmonic content at the load [26]. A 'T' type multilevel inverter is proposed for transformer less DVR with reduced switches. The basic structure consists of eight switches which generates five level output voltage using two DC sources. This designed inverter regulates the load voltage under sag condition, but this topology requires high power rated switches [27].

With no additional components such as inductor and capacitor, a new multilevel inverter is proposed. The proposed structure operates on symmetric and asymmetric mode. MATLAB simulation is done for constructing 79-levels and 321-levels. The proposed multilevel inverter is operated for grid utility from renewable energy sources [28].

Cascaded H bridge multilevel inverter contains a greater number of switching devices and sources. A new 9-level multilevel inverter in cascaded transformer is proposed with minimum number of switching devices and DC supply. Conventional cascaded transformer based 9-level MLI is compared with proposed 9-level MLI. The performance is analyzed and tested for multi carrier PWM technique [29].

A new MLI with hybrid structure is proposed. Selective harmonic elimination technique is applied to obtain the quality in the output voltage with reduction in lower order harmonics. The proposed topology is analyzed for R and RL loads [30]. High voltage stress occurs in two stage switched capacitor multilevel inverter. To overcome this problem single stage switched capacitor multilevel inverter is proposed. The basic unit consists of twelve switches with only one DC source. The proposed topology is tested experimentally [31]. Low total standing voltage is achieved by multi-unit MLI with single phase supply using minimum number of switching components. The proposed structure is compared with existing MLI units under varying loaded conditions [32]. Various configurations of cascaded half bridge inverter applied for grid tied PV system is discussed in terms of control methodologies. The performance of CHB inverter is validated in all the aspects [33]. The various applications of MLI are shown in Table 1.

Table 1. Applications of MLI with reduced switches.

Type of Applications
Renewable energy systems
Fuel cells
Low Voltage and High Voltage
Grid connections
Drives
High frequency AC distribution systems
Electric Vehicle

Output voltage level generated with respect to the number of switches used for various topologies is tabulated in Table 2.

Table 2. Number of switches versus Number of Levels.

Reference Paper Number	Name of MLI	Number of Switches	Number of Levels
21	Three Source MLI	8	15
22	Bidirectional stepped MLI	7	7
23	Switched Voltage Cascaded MLI	12	17
24	Flying Capacitor MLI	12	17
		9	5
25	MLI using Proton-exchange membrane fuel cell	10	7
		15	15
		9	9
26	Modified Half bridge MLI	14	49
27	T-type MLI	5	5
		13	79
28	Trinary MLI	20	321
29	Switched-dc-source sub module MLI	6	9
30	Bi-direction MLI	10	13
31	Single-Stage Switched-Capacitor MLI	12	9

3. Issues in MLI with Low Device Count

In MLI, there are issues such as: Voltage unbalancing, gate pulse generation and circuit complexity. The major issues in various MLI topologies are discussed in Table 3. Some of the challenges are discussed below. In [20] additional power stage is used, a transformer along with the inverter which increases the cost. Reactive power capability is absent in the structure proposed in [20]. The design structure presented in [21,22] requires a greater number of components for constructing higher number of levels. The design topology in [23] uses bidirectional switches which increases the cost and size of the inverter. The inverter topology in [24,25] utilizes more circuit components to generate higher output voltage levels. The reduction of harmonic content in the output load waveform is challenging and it is presented in [26]. Inverter proposed in [27] has higher total standing voltages. The presented topology in [28,29] requires more circuits to achieve more output levels. A complex control is necessary in-order to design a bi-direction MLI [30]. Voltage balance in the capacitor is challenging in the switched capacitor MLI with reduced switch count [31]. Balancing the voltage in DC link needs high attention [32]. The configuration presented in [33] utilizes more switches to generate higher number of voltage levels. In [34], the basic structure of proposed system requires two bidirectional switches and it is used to generate 17-levels in the output via asymmetrical configuration. In order to increase the output levels by cascading the SMLMI unit or increasing the ladder structure that is 'm', the total voltage appeared across the switches S_x and S_y is becoming high and it increases the rating of the devices. Furthermore, the switching frequency is high to generate desired output levels which increases switching losses.

In [35], various topologies of MLI were designed using higher number of voltage sources with less number of switches to achieve more output voltage levels and the issues found in the configurations are listed in Table 2. In [36,37], a symmetric multilevel inverter is designed and found failure in the implementation of medium and high voltage applications. In [38,39], a multilevel inverter is designed using asymmetrical voltage sources to generate more output voltages levels with increase in the number of switches. A hybrid MLI designed with complex control technique and it is presented in [40].

In [41], the proposed system is used to generate 9-levels in the output with four dc sources, eight switches and four diodes. While extending the output voltage levels, more units are added and thus conduction and switching losses are more. In addition to increase in switching loss, stress across the switch is increasing.

Table 3. Issues in MLIRS.

Reference Paper Number	Type of MLI	Problems
35	Reduced switch MLI	Increase in input DC voltage sources.
36	Symmetric	Failure in finding out the PWM technique.
37	Symmetric	Failure in the implementation of medium and high voltage applications.
38	Asymmetric	Failure in designing the filter for harmonic reduction.
39	Asymmetric cascaded MLI	More number of switches are used.
40	Hybrid	Control technique is complex.
41	Symmetric and Asymmetric	<ul style="list-style-type: none"> • More blocking voltages due to bidirectional switches • More switching losses • Not applied for High voltage applications • Cost Increases due to Bidirectional switches
42	Symmetric	More peak inverse voltage.
43	Cascaded switched diode MLI	Number of diodes is more.
44	Asymmetric	Requirement of more number of diodes due to high output voltage levels
45	Asymmetric	Switching scheme is more complex.
46	Asymmetric	Not possible for low frequency applications.
47	Reduced switch MLI	Low fault tolerant capacity.
48	Symmetric & Asymmetric	More number of diodes
49	Modularized MLI	Not suitable for high voltage applications.
50	Symmetric and Asymmetric	More switches to be turned on to generate a voltage level.

Circuit proposed in [42] consists of single source and double sources configuration to build multi levels in the output by connecting the sources in series and parallel. For this configuration there is a possibility of short circuit of DC sources while turning on the sources and voltage stresses between the switches is high. A Cascaded switched diode MLI is designed utilizing more number of diodes [43].

In [44], proposed cascaded switched diode structure consists of two stages. First stage contains dc sources, switch and diode. The second stage is an H-bridge inverter, in order to increase the multilevel in the output, number of units in the first stage is increased and thus large number of switches and diodes are required.

Conventional diode clamped and capacitor clamped multilevel inverters [45] are modified by adding single phase full bridge inverter. This proposed system reduces the number of switches but the requirement of diodes and capacitors are increased compared to the conventional inverters.

Significant factors of inverter design using Asymmetric voltage sources presented in [46] is identified and tabulated in Table 2. As well, few of the challenges in the reduced switch MLI [47], Asymmetric MLI [48] and modularized MLI [49] were identified and listed in Table 2.

In [50], 9-levels of output voltage are generated using 12 numbers of switches and 4 number of dc sources. In order to construct each level of output waveform, six switches are required to be turned on at an instant and thus switching losses are increasing. A 9-level symmetric and 31 level asymmetric inverter were simulated using a smaller number of voltage sources [51]. Using large number of switches, a symmetric MLI topology is designed and experimented in [52]. Also various topologies of MLI were designed using optimal number of switches [53–57].

4. Design of Proposed Cascaded SLMLI to Generate 81 Level

In the proposed work, switched ladder inverter is designed to generate 81 output voltage levels. Figure 1a is a generalized structure of SLMLI. Number of output levels can be increased by either increasing the magnitude of dc sources as shown in Figure 1b or by cascading a number of stages by fixing dc sources in each stage.

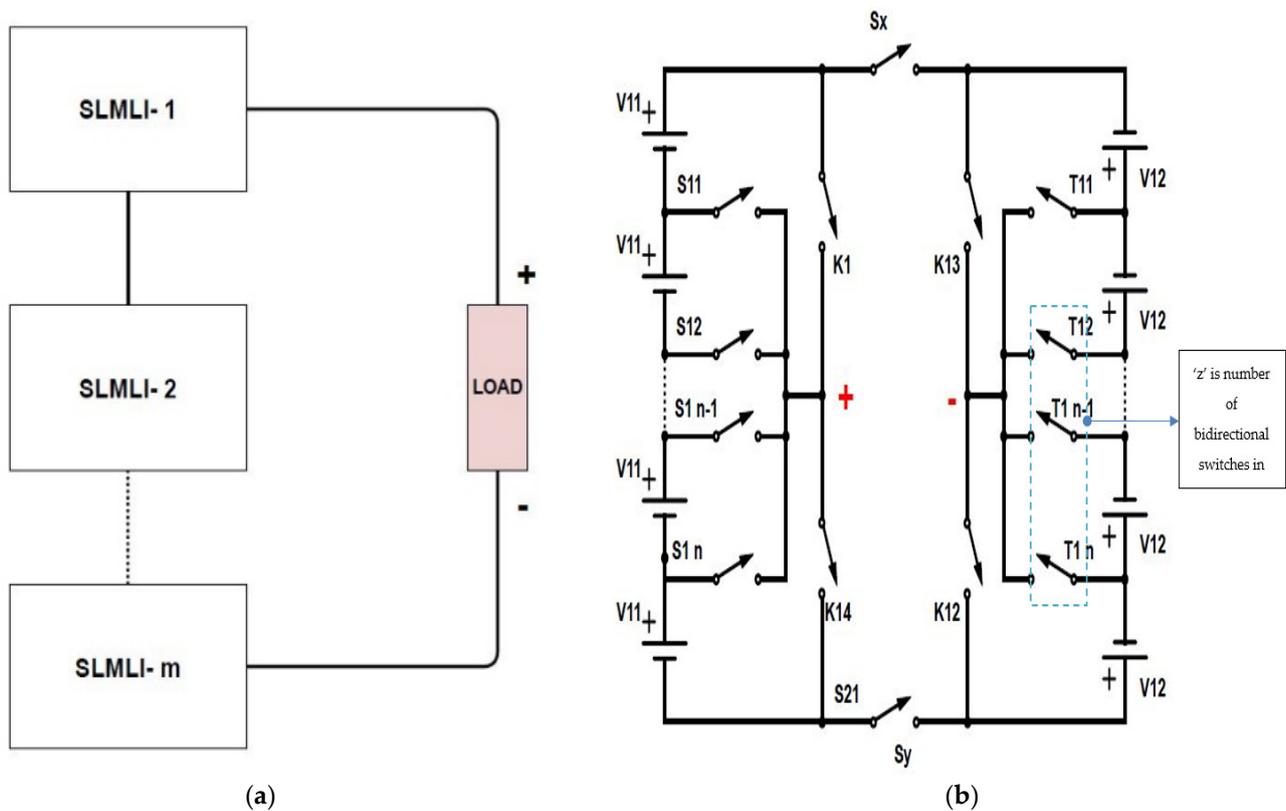


Figure 1. (a) Generalized structure of SLMLI [34]; (b) proposed SLMLI [34].

In order to increase the number of levels further, using proposed switched ladder inverter, it leads to increase the component count which makes the system bulky, costly, and complex. As well, the voltage rating on the switches of \$S_x\$ and \$S_y\$ is equal to the sum of all sources values. To reduce the number of used components and voltage on \$S_x\$ and \$S_y\$, cascade topology based on series connection of 'm' SLMLIs is recommended which is presented in Figure 1b. Proposed structure is named as cascaded switch-ladder inverter (CSLMLI). The output voltage of SLMLI (\$V_{out}\$) is equal to the sum of output voltages of all the SLMLIs and it is given in Equation (1).

$$V_{out} = V_{o1} + V_{o2} + \dots + V_{om} \tag{1}$$

where \$V_{o1}\$, \$V_{o2}\$ and \$V_{om}\$ are the output voltage produced by stage-1, stage-2 and stage-m respectively.

The voltage levels at the output are achieved by considering the quantity of bidirectional switches in each SLMLI and it is given by:

$$2z_1 = 2z_2 = \dots = 2z_b = 2z \tag{2}$$

The generalized structure shown in Figure 1 consists of unidirectional and bidirectional switches.

4.1. Design Parameters Cascaded SLMLI for Two Stages

The SLMLI design parameters are determined by using two methods and both methods are explained as follows.

Method 1: In this method, necessary expressions are given below:

$$V_1 = V_3 = V_{dc} \quad (3)$$

$$V_2 = V_4 = (z + 2) \times V_{dc} \quad (4)$$

The maximum output voltage, level generation, switches and sources required are calculated as follows:

$$V_{\text{cascaded,max}} = 2 \times [(z + 1) \times (V_1 + V_4)] \quad (5)$$

$$N_{\text{level}} = 2 \times [(V_{\text{cascaded,max}})/V_1] + 1 \quad (6)$$

$$N_{\text{switch}} = 4 \times (2z + 3) \quad (7)$$

$$N_{\text{source}} = 4 \times (z + 1) \quad (8)$$

where z is the number of bidirectional switches in each ladder structure.

Method 2: In this method, V_3 and V_4 values are computed and it is mentioned as follows:

$$V_1 = V_{dc} \quad (9)$$

$$V_2 = (z + 2) \times V_{dc} \quad (10)$$

$$V_3 = (4z) \times V_1 \quad (11)$$

$$V_4 = (z + 2) \times V_3 \quad (12)$$

The maximum output voltage, level generation, switches and sources required are represented as follows:

$$V_{\text{cascaded,max}} = (2) \times (V_1 + V_2 + V_3 + V_4) \quad (13)$$

$$N_{\text{level}} = 2 \times [(V_{\text{cascaded,max}})/V_1] + 1 \quad (14)$$

$$N_{\text{switch}} = 2 \times (4z + 6) \quad (15)$$

$$N_{\text{source}} = 4 \times (z + 1) \quad (16)$$

4.2. Cascaded SLMLI to Generate 81 Levels (2-Stages)

Inverter shown in Figure 1b is used to generate 'n' number of levels, but the rating of switches is increasing with the increase in magnitude of voltage. This problem is solved by cascading number of switch ladder multilevel inverters to generate 'n' number of output levels. Figure 2 shows the circuit diagram of cascaded SLMLI to generate 81 levels in the output voltage.

Stage-1 requires the same number of switches and sources that used in stage-2. In stage-1, unidirectional switches are represented as T11, T12, T13, T14, S_{X1} , S_{Y1} and the bidirectional switches are shown as S11, S12. In stage-2, unidirectional switches are mentioned as T21, T22, T23, T24, S_{X2} , S_{Y2} and the bidirectional switches are shown as S21, S22. By cascading two stages, the voltage stress between the switches and dv/dt are reduced and hence it reduces overall cost. Table 4 shows the switching sequence for the proposed SLMLI.

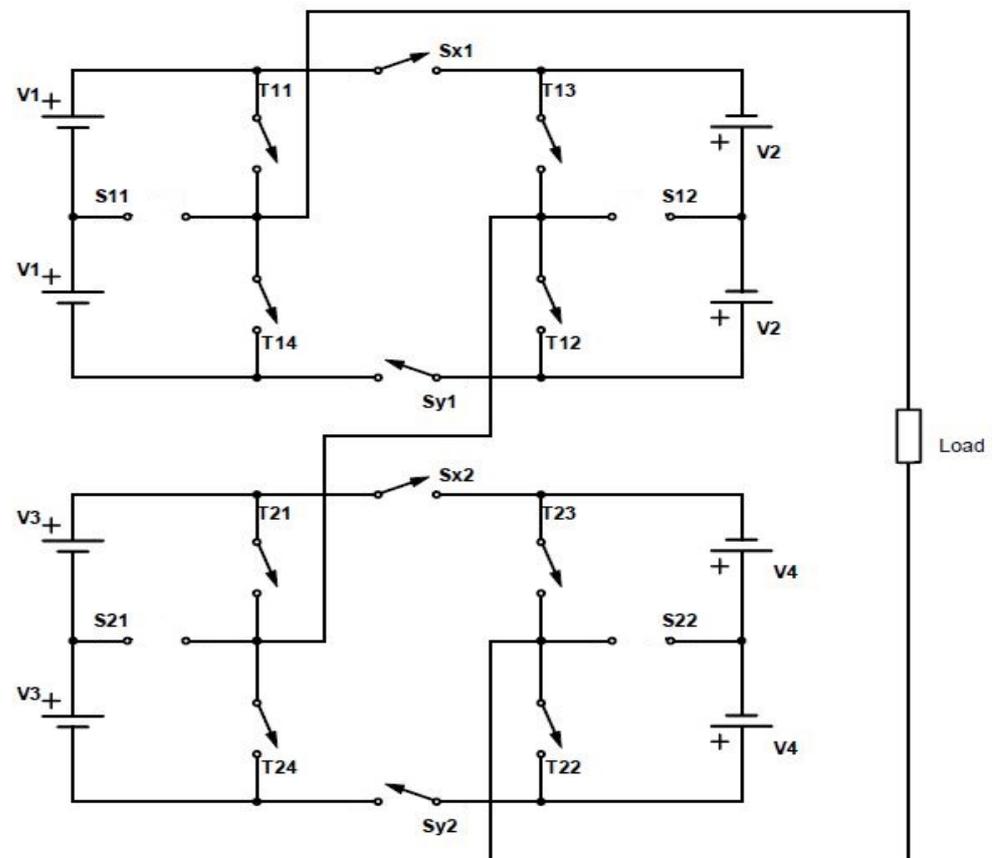


Figure 2. Cascaded two stages of SLMMLI.

Table 4. Switching sequence for the Proposed SLMMLI.

No. of Levels	Voltage Levels	T ₁₁	T ₁₂	T ₁₃	T ₁₄	S ₁₁	S ₁₂	S _{1X}	S _{1Y}	T ₂₁	T ₂₂	T ₂₃	T ₂₄	S ₂₁	S ₂₂	S _{2X}	S _{2Y}
1	0	δ	ø	δ	ø	ø	ø	δ	ø	δ	ø	δ	ø	δ	ø	δ	ø
2	V ₁	ø	δ	ø	ø	δ	ø	ø	ø	δ	ø	δ	ø	ø	ø	ø	δ
3	V ₁ + V ₁	δ	δ	ø	ø	ø	ø	ø	ø	δ	ø	δ	ø	ø	ø	ø	δ
4	V ₃	ø	ø	ø	δ	ø	δ	ø	ø	ø	ø	δ	ø	ø	ø	ø	δ
5	V ₄	ø	ø	ø	ø	δ	δ	ø	ø	ø	ø	δ	ø	ø	ø	ø	δ
37	V ₁ + V ₂ + V ₃ + V ₃ + V ₄ + V ₄	ø	ø	ø	ø	δ	δ	ø	ø	ø	ø	δ	ø	ø	ø	ø	δ
38	V ₁ + V ₁ + V ₂ + V ₃ + V ₃ + V ₄ + V ₄	δ	ø	ø	δ	ø	ø	ø	ø	ø	ø	δ	ø	ø	ø	ø	δ
39	V ₂ + V ₂ + V ₃ + V ₃ + V ₄ + V ₄	ø	ø	δ	ø	δ	ø	ø	ø	ø	ø	δ	ø	ø	ø	ø	δ
40	V ₁ + V ₂ + V ₂ + V ₃ + V ₃ + V ₄ + V ₄	ø	ø	ø	ø	ø	ø	ø	ø	ø	ø	δ	ø	ø	ø	ø	δ
41	V ₁ + V ₁ + V ₂ + V ₂ + V ₃ + V ₃ + V ₄ + V ₄	δ	ø	δ	ø	ø	ø	ø	ø	ø	ø	δ	ø	ø	ø	ø	δ

Where the ‘ON’ conditions of the switches are represented as ‘δ’ and the ‘OFF’ condition of the switches are represented as ‘ø’.

5. Pulse Generation and Simulation Results

In order to construct multiple voltage levels in the load side, proper generation of pulses is needed. Figure 3 explains the method to generate pulses for the inverter. Pulses are generated by comparing a sinusoidal wave with the constant voltage steps at regular intervals. Switching state will become one when sinusoidal is in between i^{th} level and $i + 1^{th}$ level. For 81 level generation, value of ‘i’ will be varying from 0 to 41 to construct positive 41 levels and same will be repeated for negative also. Adder will combine all the switching states created and it will act as an input to activate the corresponding switching pattern via a multiport switch. De-multiplexer is used for distributing the pulses for the inverter. Based on the switching sequence shown in Table 4 the pulses will be given to appropriate switches. In the Table 4, the ON condition and OFF condition of the switches are represented as δ and ø respectively.

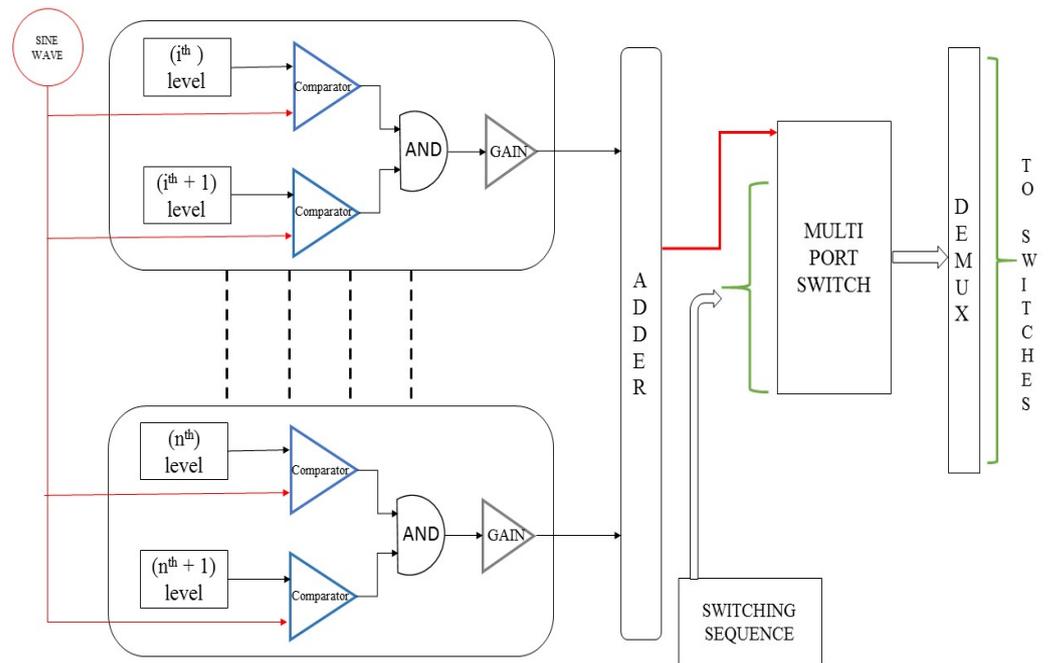


Figure 3. Block diagram for pulse generation.

Figure 4 shows the block diagram for generating 81 levels and Figure 2 represent the structure of SLMLI. Pulse generator (Figure 3) is used for creating pulses for all the switches located in the two stages.

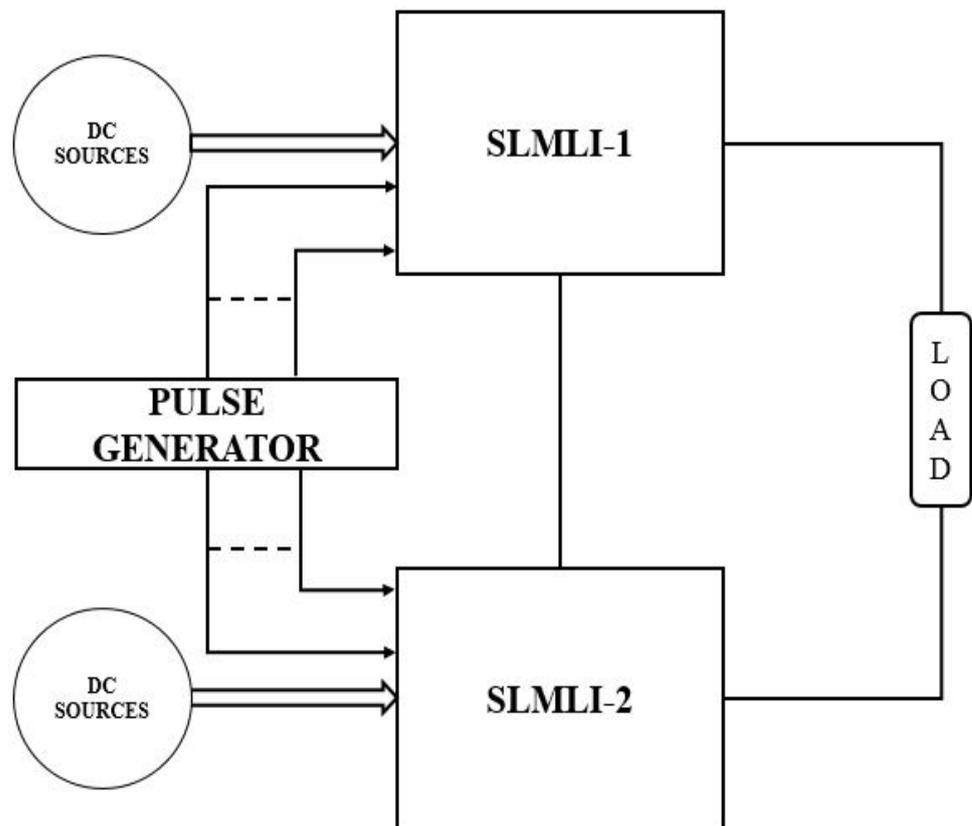
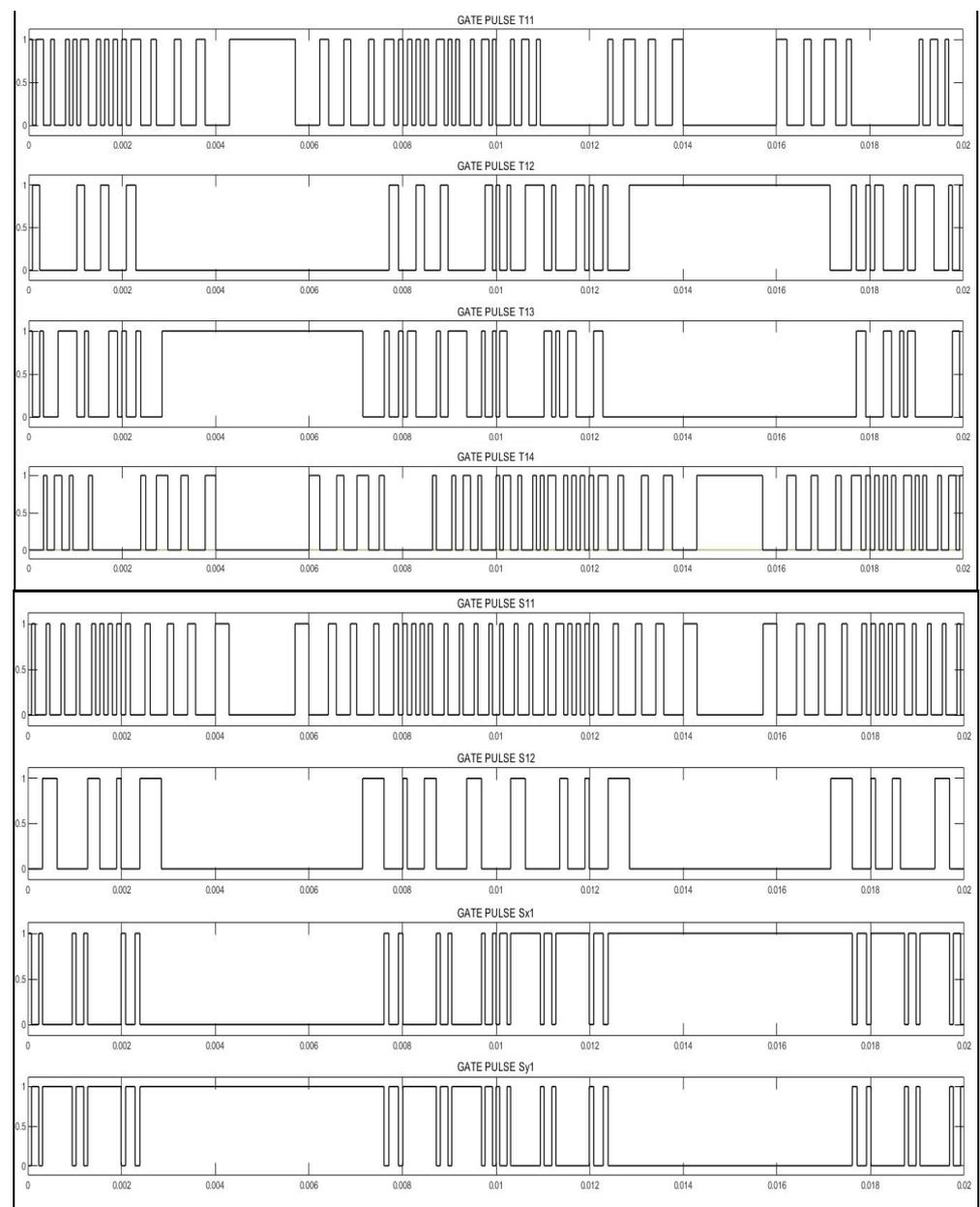


Figure 4. Block diagram of SLMLI.

Figure 5a,b shows the pulse waveforms for one cycle of switches in stage-1 and stage-2 respectively to generate 81 levels.

The magnitude of the direct current voltage sources in switched ladder multilevel inverter stage-1 are selected as $V_1 = 5$ V and $V_2 = 15$ V. For the stage-2 switched ladder multilevel inverter the amplitude of the voltage sources is selected as $V_3 = 20$ V and $V_4 = 60$ V. The proposed topology is simulated for grid frequency 50 Hz and the parameters of the sources voltages and load values are given in Table The magnitude of the direct current voltage sources in switched ladder multilevel inverter stage-1 are selected as $V_1 = 5$ V and $V_2 = 15$ V. For the stage-2 switched ladder multilevel inverter the amplitude of the voltage sources is selected as $V_3 = 20$ V and $V_4 = 60$ V. The proposed topology is simulated for grid frequency 50 Hz and the parameters of the sources voltages and load values are given in Table 5.



(a)

Figure 5. Cont.

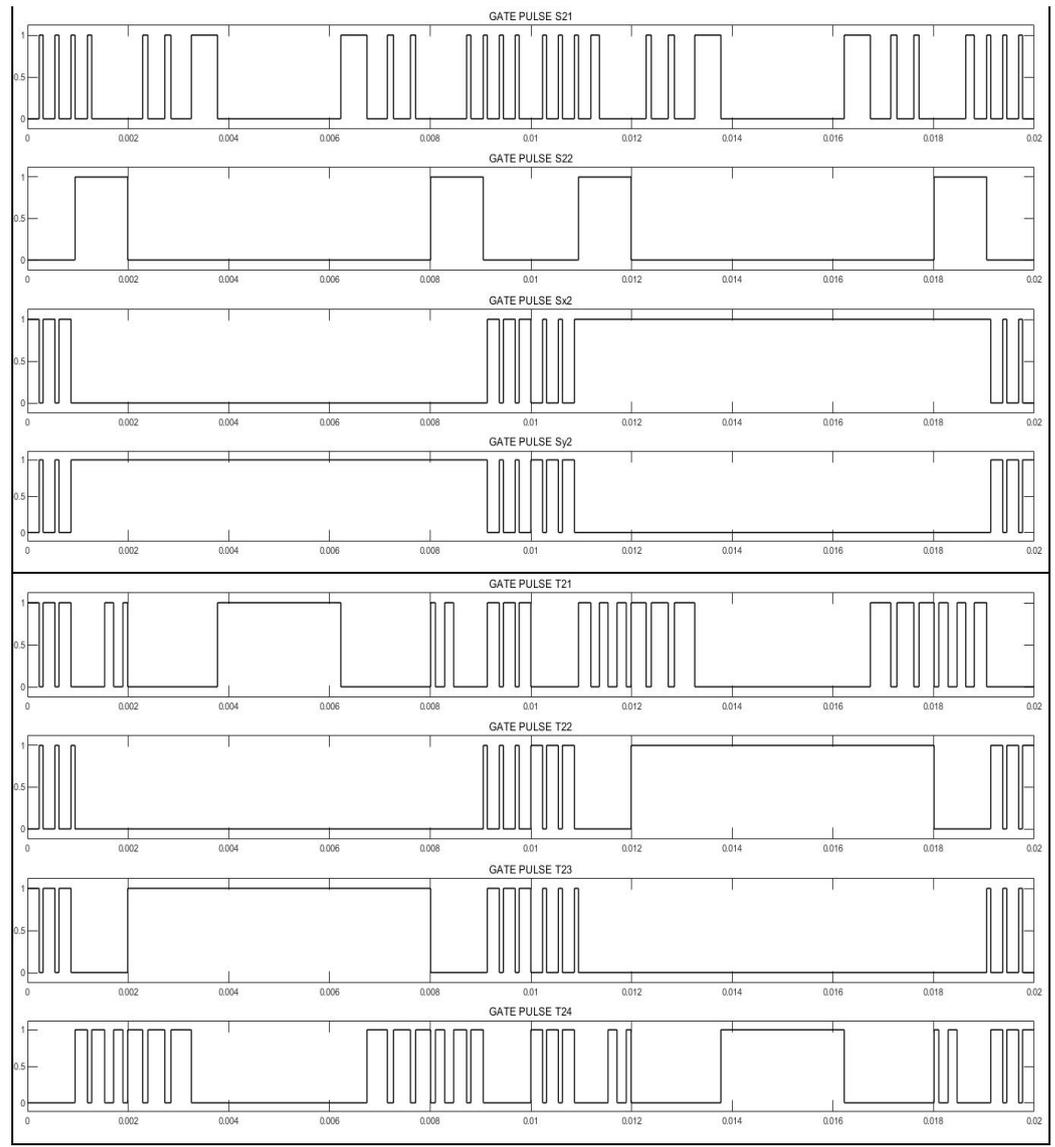


Figure 5. (a) Pulse waveforms for stage-1; (b) pulse waveforms for stage-2.

Table 5. Specification of two stage SLMLI.

S.No	Parameters		Values
INPUT VOLTAGES OF SLMLI-1			
1		V_1	5 V
2		V_2	15 V
INPUT VOLTAGES OF SLMLI-2			
3		V_3	20 V
4		V_4	60 V
OUTPUT FREQUENCY			
5		F	50 Hz
LOAD			
6	R	1st cycle	10 Ω
		2nd cycle	5 Ω
		3rd and 4th cycle	2.5 Ω
7	L	1st cycle	10 Ω , 5 mH
		2nd cycle	5 Ω , 2.5 mH
		3rd and 4th cycle	2.5 Ω , 1.25 mH

The 81 level inverter output voltage and output current waveform is shown in Figure 6. The resistive load is tested for four cycles (i.e., 0.08 s). The inverter is tested with resistive load of 10 Ω for the first cycle (i.e., 0.02 s), during this period the output load current is observed as 20 A. For the second cycle (i.e., from 0.02 s to 0.04 s) the inverter is connected with 5 Ω resistance and obtained the load current as 40 A. For the third and fourth cycle (i.e., from 0.04 s to 0.08 s), the inverter is connected with load resistance of 2.5 Ω to produce 80 A at the load. For these entire instances, the peak load output voltage is observed as ±200 V.

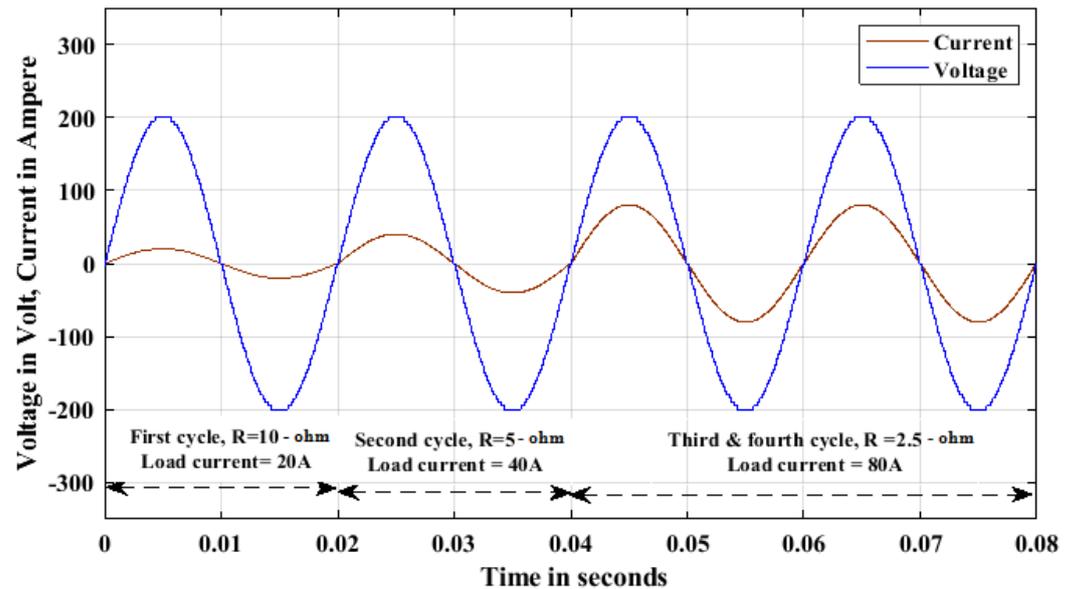
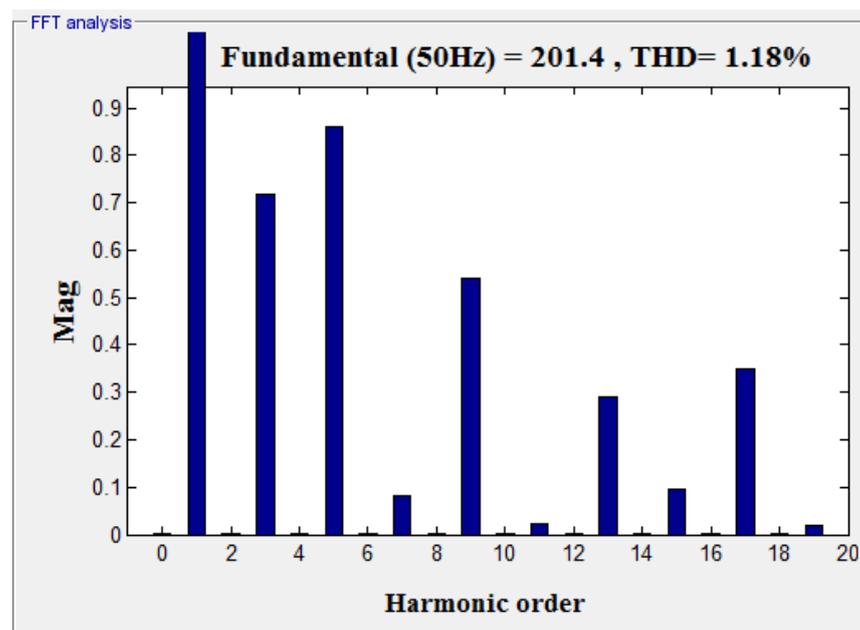


Figure 6. Output voltage and change in current waveforms for variable R load.

The harmonic content present in the output voltage and current waveforms are obtained from FFT (Fast Fourier transform) analysis are 1.18% and it is shown in Figure 7a,b.



(a)

Figure 7. Cont.

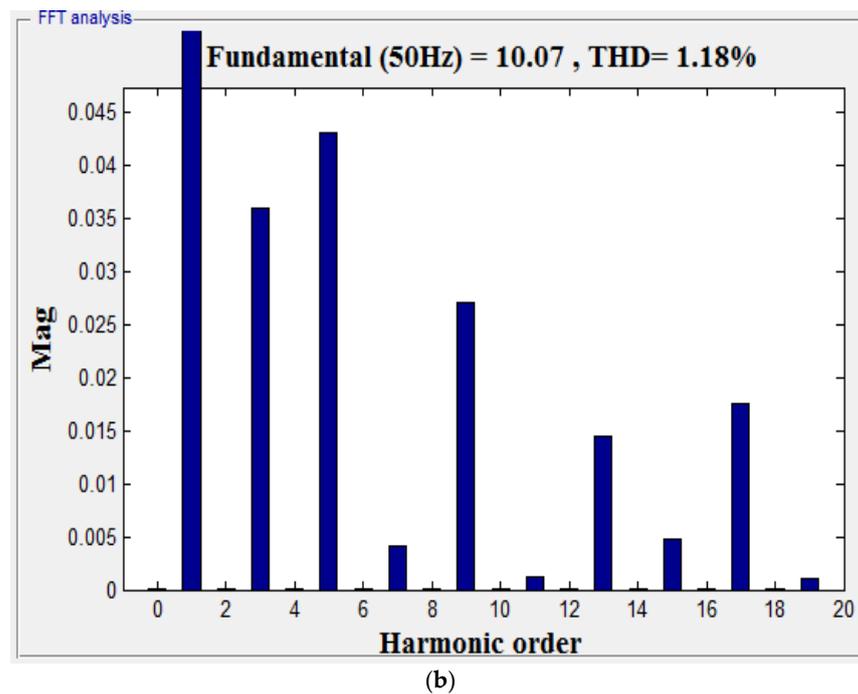


Figure 7. (a) FFT for output voltage fed with R load; (b) FFT for output current fed with R load.

Figure 8 shows the output voltage and variation in the current waveform for the change in impedance load at equal interval of time. For $Z = 10.12 \Omega$, 5.06Ω and 2.53Ω the output current is measured as 19.76 A, 39.52 A and 79.05 A respectively.

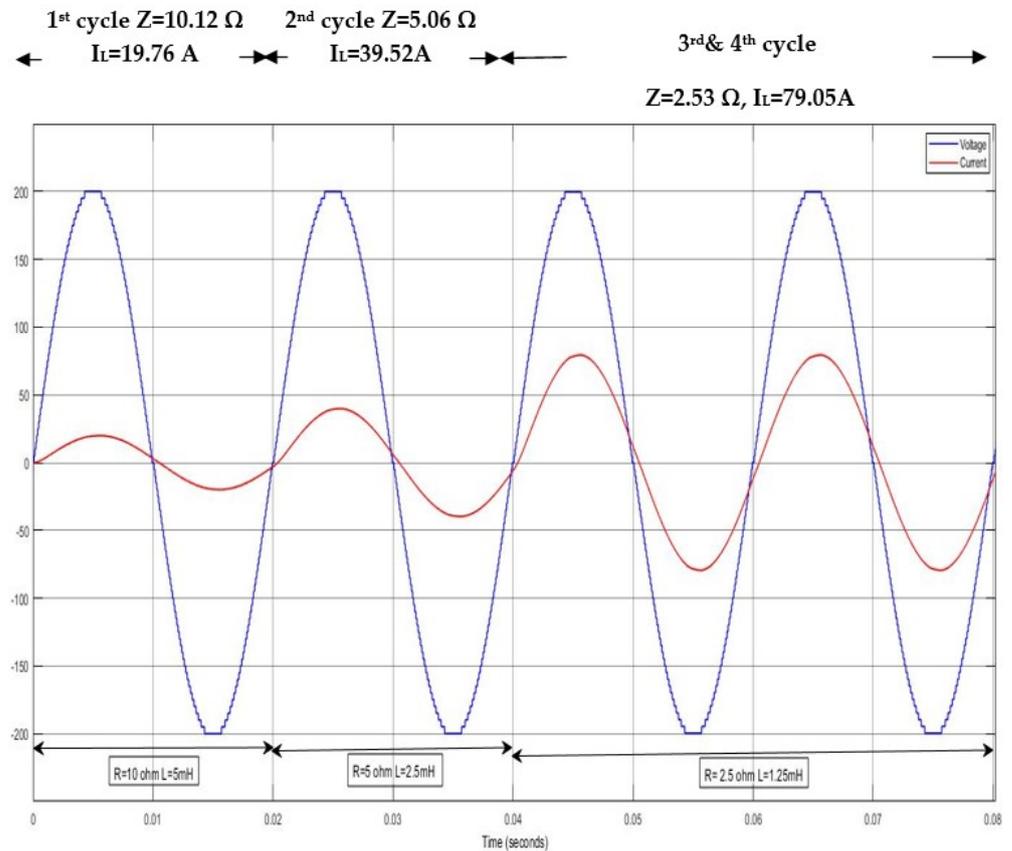
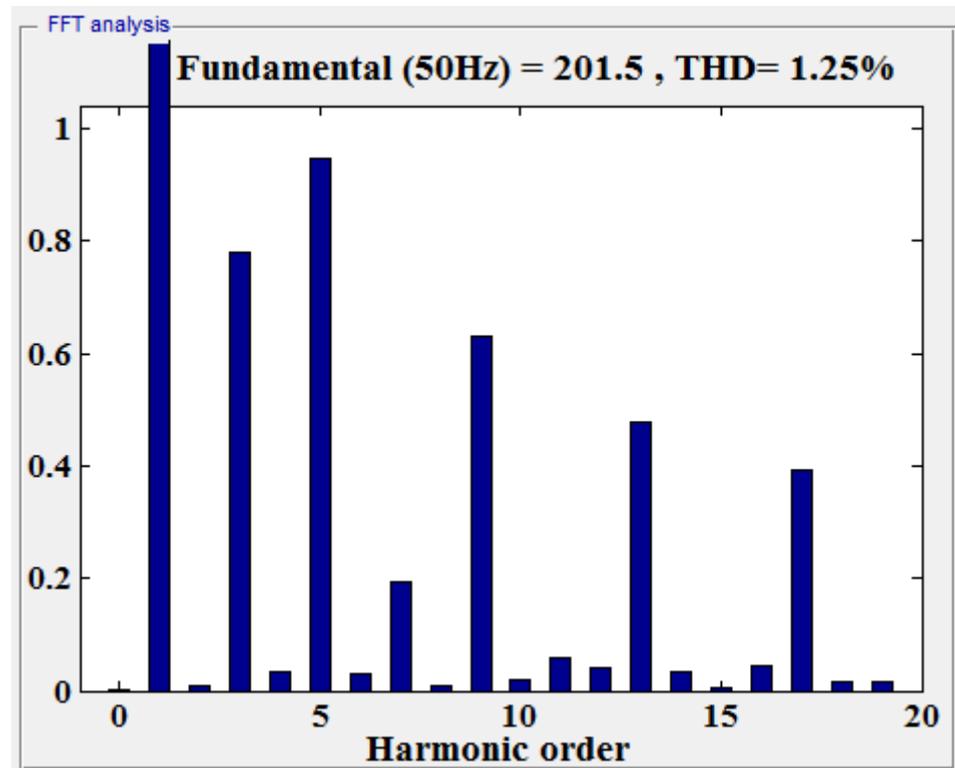
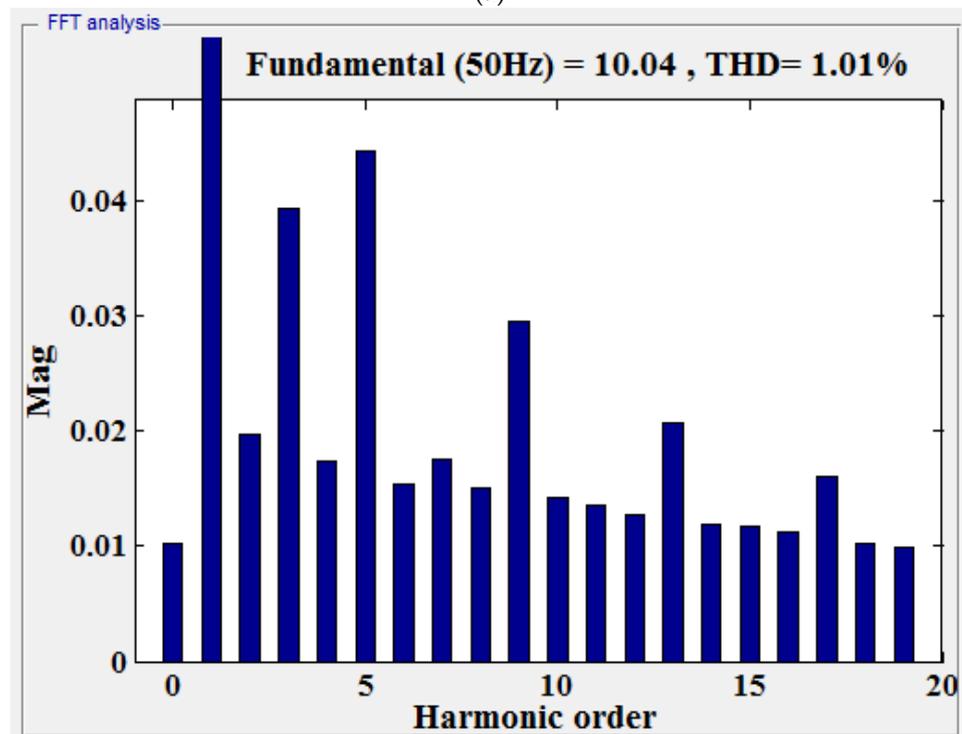


Figure 8. Output voltage and current waveforms for RL load.

The harmonic content present in the output voltage and current waveforms fed with impedance load obtained from FFT analysis are 1.25% and 1.01%, it is shown in Figure 9a,b. Current THD is reduced due to inductance load added in the circuit which smoothen the current waveform and small phase swift occurs due to inductance.



(a)



(b)

Figure 9. (a) FFT for output voltage fed with RL load; (b) FFT for output current fed with RL load.

When motor is supplied by a cascaded two stages of SMLMI of 81 levels in the output, the speed of the motor is shown in Figure 10 for the load torque of 1 Nm, due to load torque it settles at average speed of 1730 rpm.

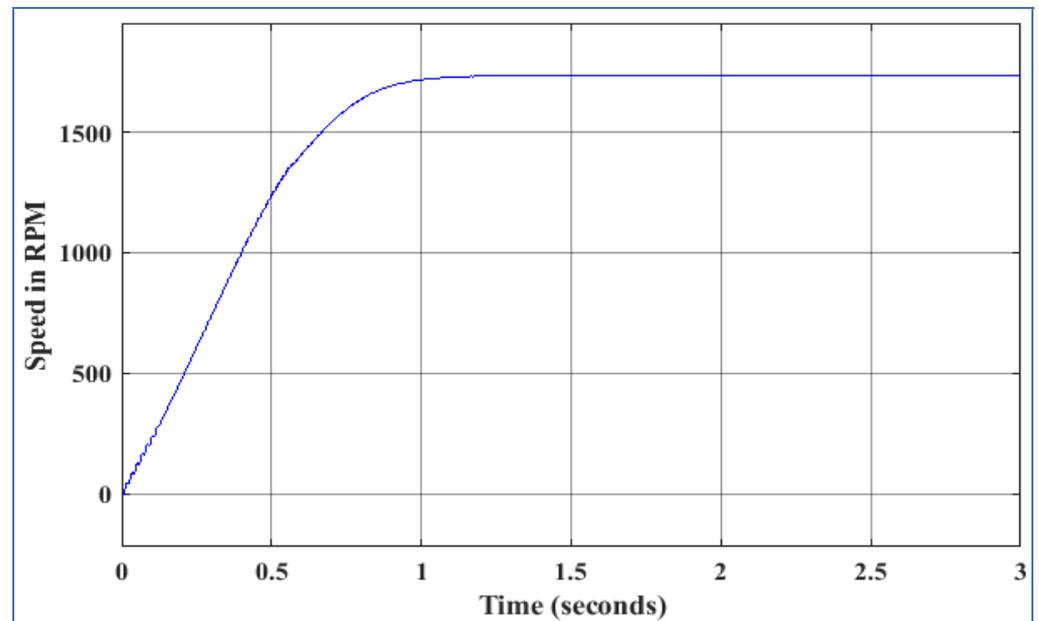


Figure 10. Speed of single stage SMLMI fed induction motor.

The electromagnetic torque produced by the given induction motor fed by the cascaded two stages of SMLMI is shown in Figure 11.

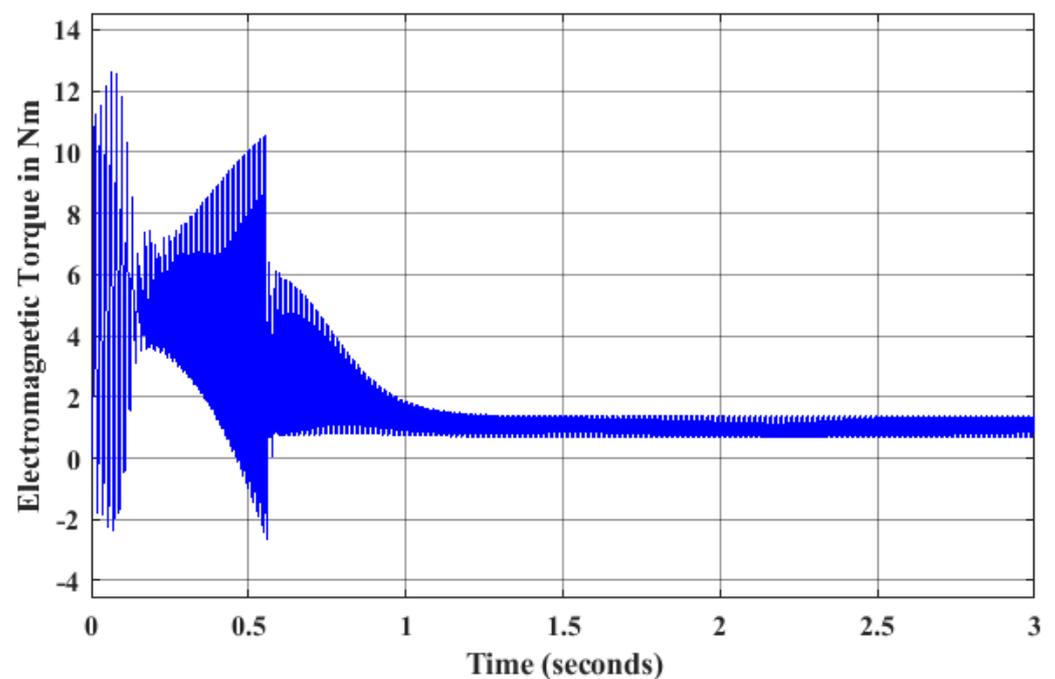


Figure 11. Electromagnetic torque of single stage SMLMI fed induction motor.

FFT analysis for the source voltage and current of induction motor is shown in Figure 12a which contains the fundamental frequency of 60 Hz and the peak magnitude is 156.7 V and the voltage THD is 1.24%. The input current drawn from the SMLMI fundamental peak is 3.434 A and the THD is 4.12% as shown in Figure 12b.

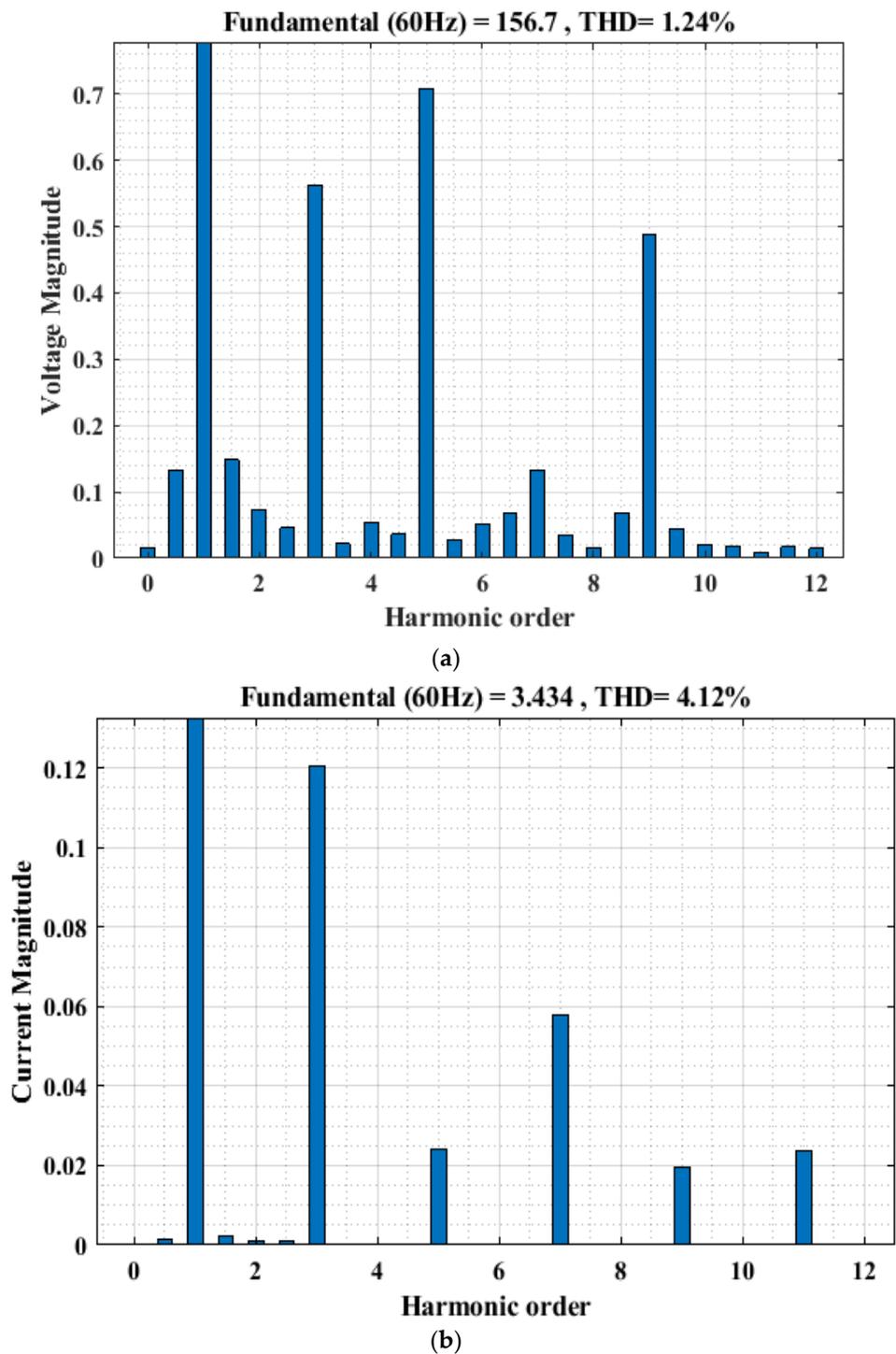


Figure 12. (a) FFT analysis for input voltage for induction motor load; (b) FFT analysis for current for induction motor load.

5.1. Speed Control Technique

In this speed control has been done by varying the supply voltage given to the induction motor. Specification of the inverter is shown in Table 6, as per proposed system the output voltage has 81-levels which gives to the rated voltage of 110 V (rms) due to that it will produce the rated speed of the induction motor which is 1800 RPM. The magnitude of the direct current voltage sources in switched ladder multilevel inverter stage-1 are selected as $V_1 = 4V$ and $V_2 = 12 V$. For the stage-2 switched ladder multilevel inverter the

amplitude of the voltage sources is selected as $V_3 = 16$ V and $V_4 = 48$ V, the specification of inverter and induction motor is given in Table 6.

Table 6. Specification of Inverter and Induction motor.

S.No	Parameters	Values
Input voltages of SLMLI-1		
1	V_1	4 V
2	V_2	12 V
Input voltages of SLMLI-2		
3	V_3	16 V
4	V_4	48 V
Output frequency		
5	f	60 Hz
Induction motor load		
6	Power	0.25 Hp
7	Supply voltage	110 V
8	Frequency	60 Hz
9	Speed	1800 RPM
10	Load torque	1 Nm

Figure 13 shows the various speed responses of the induction motor with respect to different input voltages. The blue colored line in the graph shows the speed response for the rated voltage given by the inverter which is nearly rotates at rated speed of 1736 RPM.

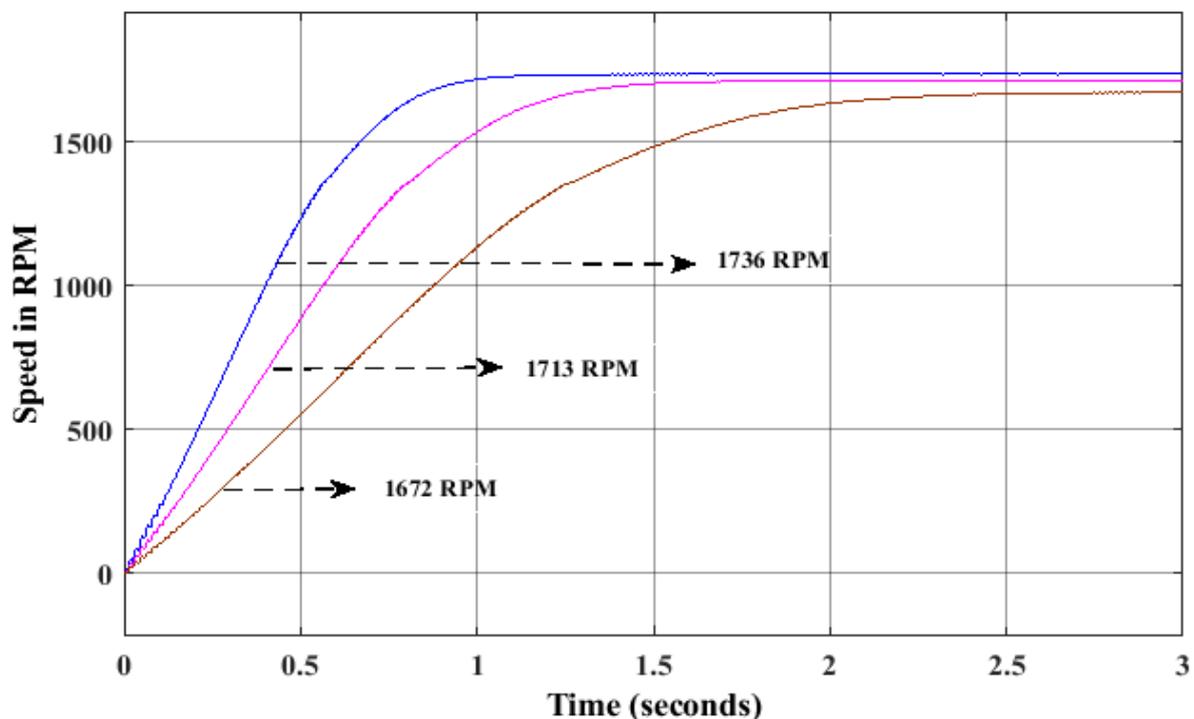


Figure 13. Various speed responses of the induction motor with respect to different input voltages.

Variation in the inverter output voltage can be achieved by changing the magnitude of sinusoidal reference control logic and it is shown in Figure 14. In order to vary the speed of the motor, change in magnitude of reference is done; the other two different speeds are shown in Figure 13 that is plotted with pink and brown lines. These speeds are less compared to the rated speed, less than rated speeds only achieved by this control technique.

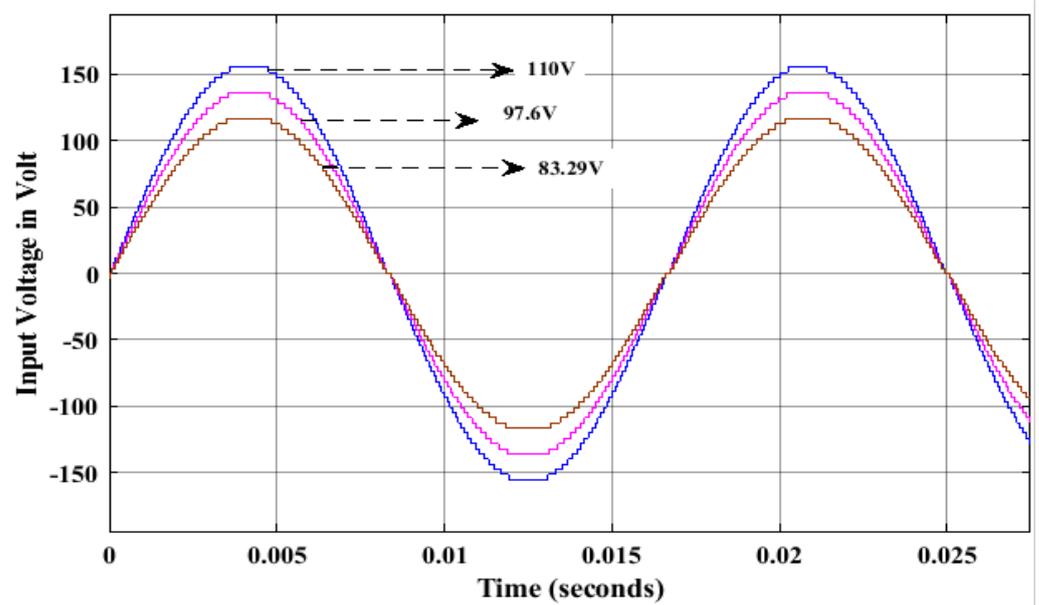


Figure 14. Different Output voltages of a SLMLI.

Figure 14 shows the inverter output voltages for different magnitudes, blue colored voltage in Figure has the magnitude of 110 V rms which gives to the induction motor as per motor rating. The other two colored voltages in the Figure 14 are reduced voltage and the magnitude is less compared to the rated voltage of the motor.

The load torque is applied as 1 Nm at 3 s and 1.25 Nm at 6 s. The variation in load torque, speed and current waveform are shown in Figures 15–17.

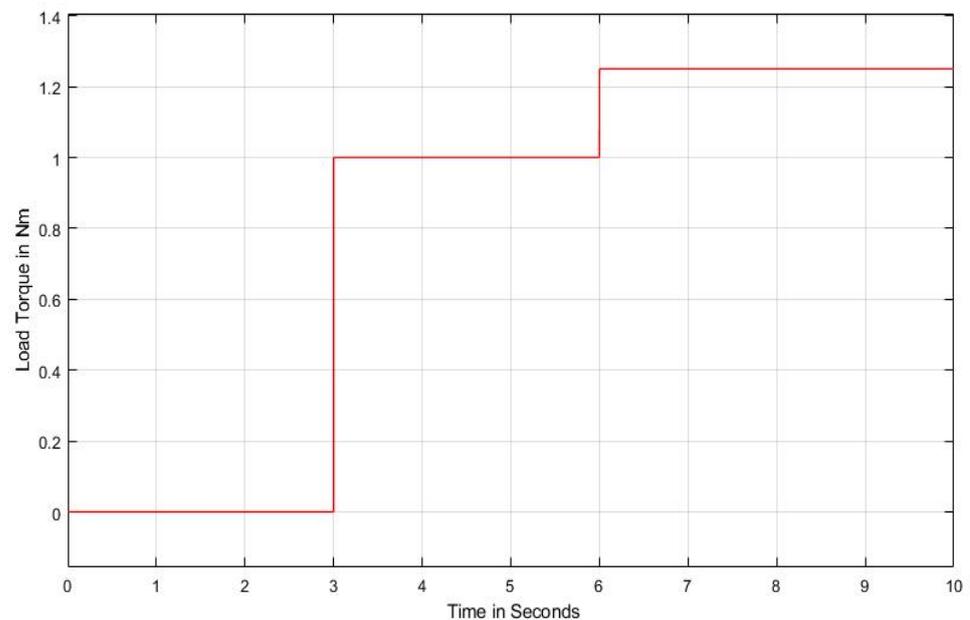


Figure 15. Load torque vs. time.

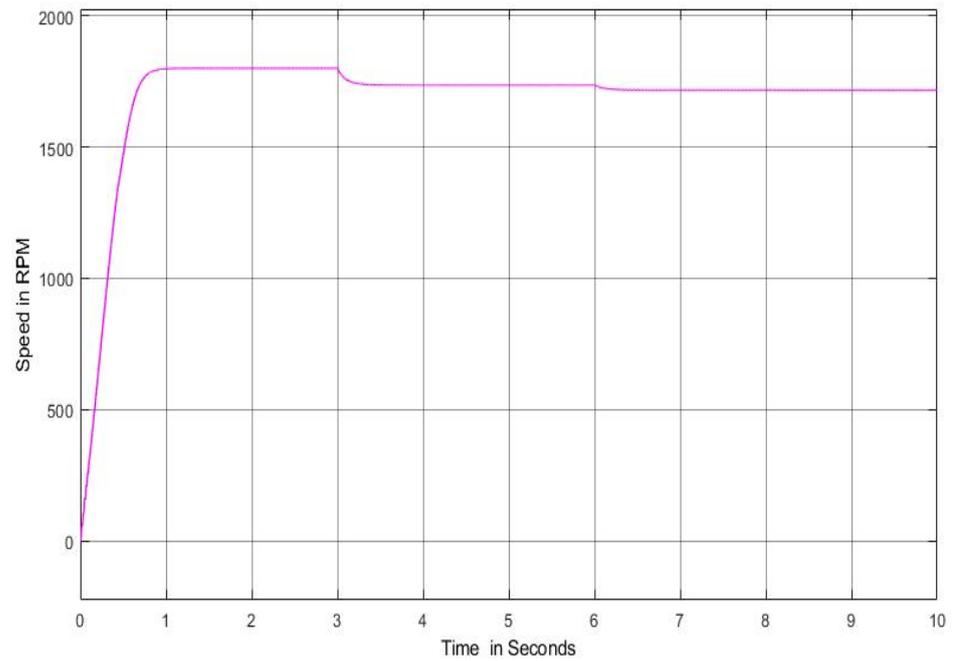


Figure 16. Speed variations for various load torque.

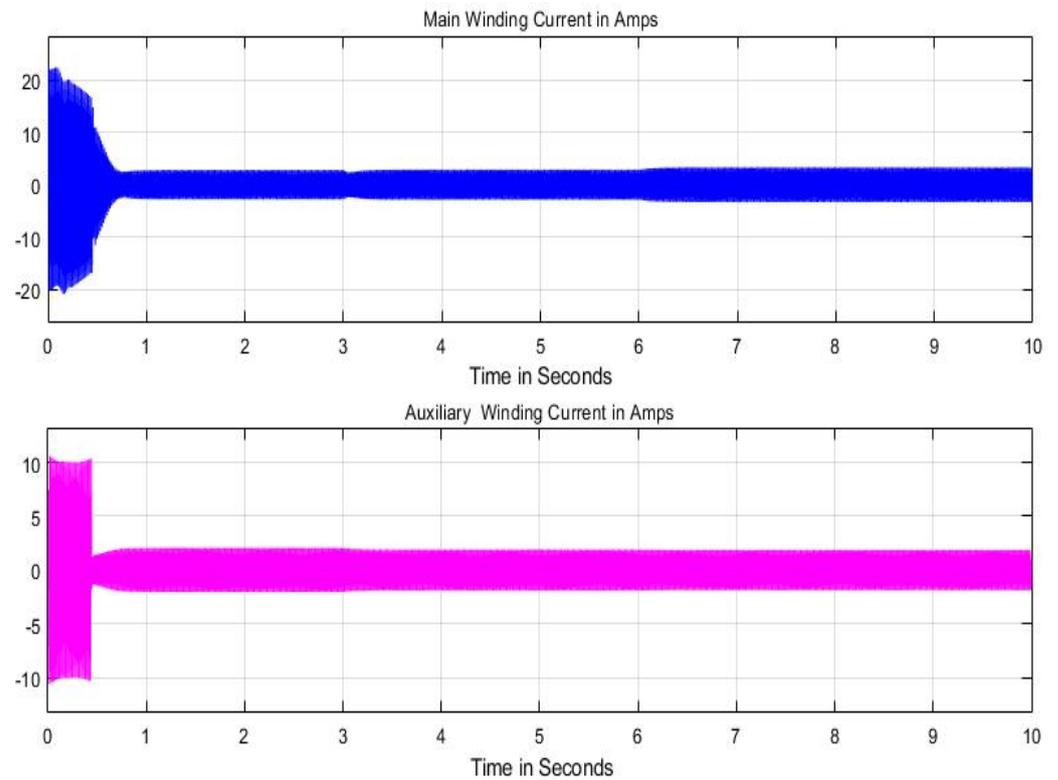


Figure 17. Current variations for various load torque.

The main winding current is zoomed and it is shown in Figure 18.

The proposed SLMLI is constructed with low number of power electronics devices for generating 81 levels in the output voltage. Design of DC sources is framed with two different algorithms. Furthermore, the SLMLI structure is tested with single phase induction motor and Speed control has been performed with satisfactory results.

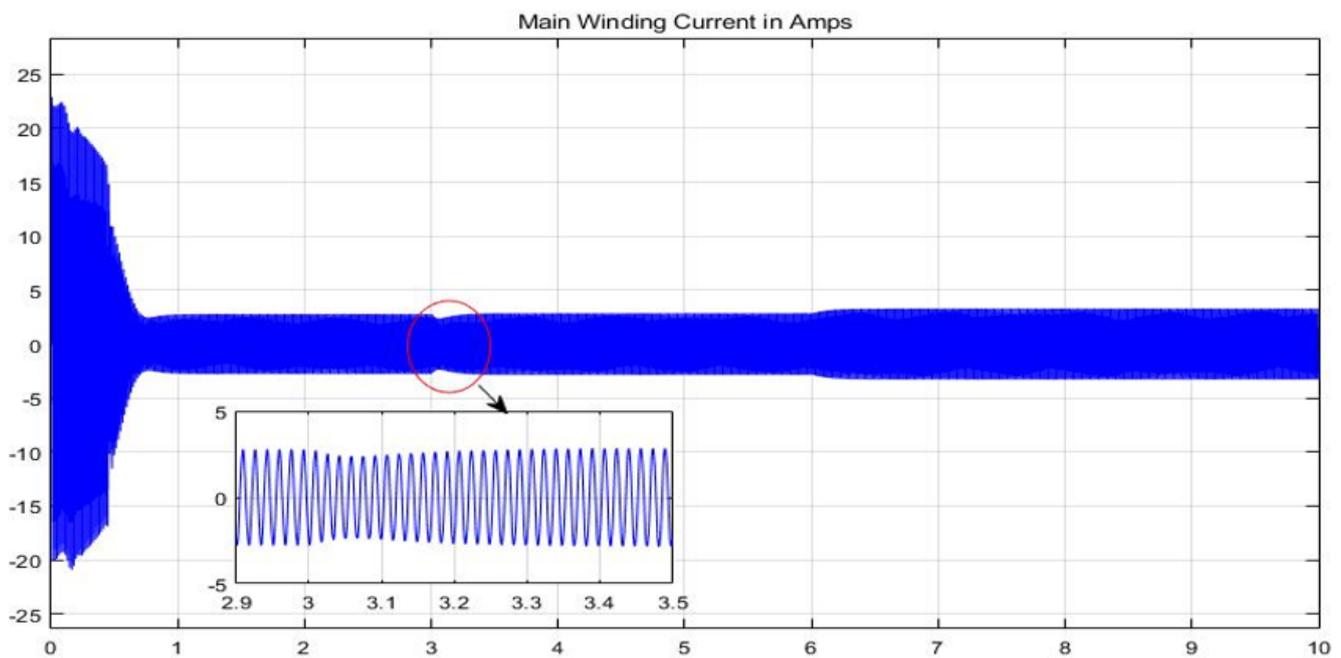


Figure 18. Main winding current for various load torque.

5.2. Cost-Benefit Analysis of 81-Level SLMLI with Conventional MLI's

The unit price of the component is given in Table 7. The cost-benefit analysis of proposed 81-level switched ladder in comparison with the conventional MLI is shown in Table 8. From the cost analysis it can be concluded that the proposed inverter can be designed with low cost compared to conventional MLI's.

Table 7. Unit price of the circuit components.

Name of the Component	Component Number	Voltage Rating	Unit Price in \$
IGBT (80 A)—Single Switch	IKW75N60TFKSA1	600 V	6.97
Diode (80 A)	VS-80EBU02	200 V	5.04
Capacitor (10 μF)	EEE-FK1K100XP	80 V	0.58

Table 8. Cost-benefit analysis of 81-level SLMLI with conventional MLI's.

To Generate 81 Level	Number of Switches	Number of Diodes	Number of Capacitors	Overall Cost of Switches in \$	Overall Cost of Diodes in \$	Overall Cost of Capacitors in \$	Total Cost in \$
Proposed MLI	20	Nil	Nil	139	Nil	Nil	139
CHBMLI	216	Nil	Nil	1505	Nil	Nil	1505
FCMLI	216	Nil	3240	1505	Nil	1879.2	3384
NPMLI	216	3160	78	1505	15926	45.24	17477

Sources from Infineon Technologies, www.digikey.in (accessed on 30 January 2021).

6. Conclusions

Much research had been undertaken to design multilevel inverters with reduced circuit components, minimum losses, low cost, and compact size with high efficiency. A survey is made in this paper to identify the type of multilevel inverter used in high and medium power applications such as Electric Vehicle, Power drives, Grid integration systems, etc. A detailed review is conducted on the recent multilevel inverter design with reduced switch count to find out the challenges and key issues. Significant issues of various multilevel inverter designs are provided in terms of number of diodes, switches, source

utilization and filter requirement. A new 81-level switched ladder inverter is configured using MATLAB/Simulink and tested with change in resistive and impedance load at equal period of time. The results were analyzed in terms of harmonic content. Further, the output of 81-level inverter is connected to 0.25 HP, 110 V single phase induction motor. The speed of the induction motor is observed for change in input voltages and the various speed curves were presented. Variation in the speed with respect to change in load torque is plotted in this paper, thus the performance of the single phase induction motor fed by 81-level switched ladder inverter is found satisfactory.

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Abbreviations

MLI	Multilevel Inverter
DC	Direct Current
THD	Total Harmonics Distortion
PWM	Pulse Width Modulation
CHB	Cascaded Half Bridge
MLIRS	Multilevel Inverter with Reduced Switch
DVR	Dynamic Voltage Restorer
SLMLI	Switched Ladder Multilevel Inverter
FFT	Fast Fourier Transform
Nm	Newton meter
RPM	Revolution Per Minute
RMS	Root Mean Square

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