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Light-Load Efficiency Improvement for Ultrahigh Step-Down Converter Based on Skip Mode

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Abstract: In this paper, two light-load efficiency improvement methods are presented and applied to the ultrahigh step-down converter. The two methods are both based on skip mode control. Skip Mode 1 only needs one half-bridge driver integrated circuit (IC) to drive three switches, so it has the advantages of easy signal control and lower cost, whereas Skip Mode 2 requires one half-bridge driver integrated circuit IC, one common ground driver IC, and three independent timing pulse-width-modulated (PWM) signals to control three switches, so the cost is higher and the control signals are more complicated, but Skip Mode 2 can obtain slightly higher light-load efficiency than Skip Mode 1. Although the switching frequency used in these methods are reduced, the transferred energy is unchanged, but the output voltage ripple is influenced to some extent.

Keywords: light-load efficiency; skip mode; ultrahigh step-down; PWM

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1. Introduction

1.1. Motivation and Incitement

Nowadays, the 48 V direct bus (DC) bus is very popular in the telecom system and networking communication equipment. The front-end AC-DC converter generates a stable 48 V DC bus from the alternating current (AC) grid. The traditional two-stage step-down converter architecture generates a low output voltage (usually under 3.3 V) from 48 V to feed the digital circuit. The 48 V DC bus is first stepped down by the first-stage converter to the 12 V DC bus to supply the power on load (POL) converter, and then the POL converter creates a low voltage to the load. Two-stage DC-DC converter requires a relatively large component count and provides relatively low efficiency.

1.2. Literature Review

The methods proposed in [1–4] use a two-stage buck converter to obtain a high step-down voltage gain, but the methods used in [1–4] require a lot of active switches, passive components, and driving circuits. The method mentioned in [5] is to use a first-order high-efficiency open-loop bus converter, which converts from a 48 V DC high voltage to a 12 V DC intermediate bus, and then generates low voltage from the POL to supply the load. In addition, the bus converter requires four active switches and two magnetic elements. If the second-stage buck converter is added, six switches and three magnetic elements are required, and a separate control integrated circuit (IC) is required. The methods proposed in [6–11] need to use multiple sets of switching regulators in parallel and to adopt interlaced pulse-width-modulated (PWM) signals to improve the conversion ratio of input and output. Compared with the traditional buck converter, under the same

input and output voltage conditions, these converters can operate in a larger duty cycle and the corresponding switching loss can be reduced. In addition, this kind of architectures requires interleaved operation with at least two phases, which is more suitable for high output current applications.

The methods proposed in [7,12–19] use coupled inductors to achieve high step-down ratio output. These circuits are relatively simple, but there will be leakage inductances to generate high voltage spikes on the switches. To reduce the breakdown risk from high voltage spikes, passive snubbers must be used to absorb and suppress the leakage energy of the winding, making the efficiency lower. Although the authors of [19] proposed that active snubbers can recover the leakage energy of the windings, these circuits are quite complicated. In the schemes in [6,13], there are many switching elements and magnetic elements, making the circuits too complicated and the corresponding cost high, and they are not suitable for low and medium power applications.

1.3. Contribution and Paper Organization

The above research results have many limitations and shortcomings in practical applications, so the authors of [20,21] proposed a new high step-down converter, which, compared with the traditional buck converter, has the following three advantages: (i) the use of a single coupled inductor only requires the addition of an active switch with common ground and a small-capacity capacitor, and this switch can be driven by an existing buck control IC; (ii) the voltage gain of this circuit does not contain nonlinear components, and hence the control is simple; and (iii) although the circuit shown in [20,21] has high efficiency at rated load, this circuit has the problem of lower efficiency at light load.

Therefore, based on the circuit structure in [20,21], this paper presents two skip mode control methods to improve the light-load efficiency. Although the switching frequency used in these methods are reduced, the transferred energy is unchanged, but the output ripple is affected to some extent. In addition, the mode exchange is very smooth. The rest of this paper is organized as follows. Section 2 briefly describes the used circuit. Section 3 elaborates on basic circuit operating principles, containing Normal Mode, Skip Mode 1, and Skip Mode 2. Section 4 gives some experimental results to verify that the light-load efficiency can be improved based on the proposed PWM control strategies. Section 5 gives some discussions. Some conclusions are drawn in Section 6.

2. Used Circuit

Figure 1 shows the circuit used herein, which contains three active switches Q_1, Q_2, and Q_3; capacitors C_B and C_o; one coupled inductor L with two windings N_1 and N_2; one magnetizing inductance L_m; and two leakage inductances L_{LK1} and L_{LK2}. In addition, Q_2 and Q_3, with both gates of Q_2 and Q_3 connected together, are driven synchronously. Accordingly, only one half-bridge driver is needed to drive three active switches. In addition, this circuit is always operated in the continuous current mode (CCM), and the illustrated waveforms shown in Figure 2a–c are for Normal Mode, Skip Mode 1, and Skip Mode 2, respectively.

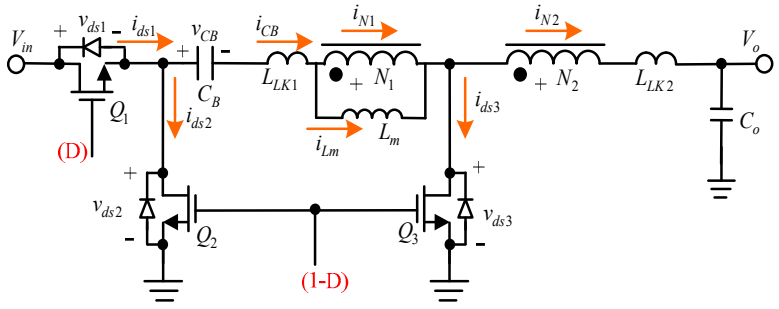
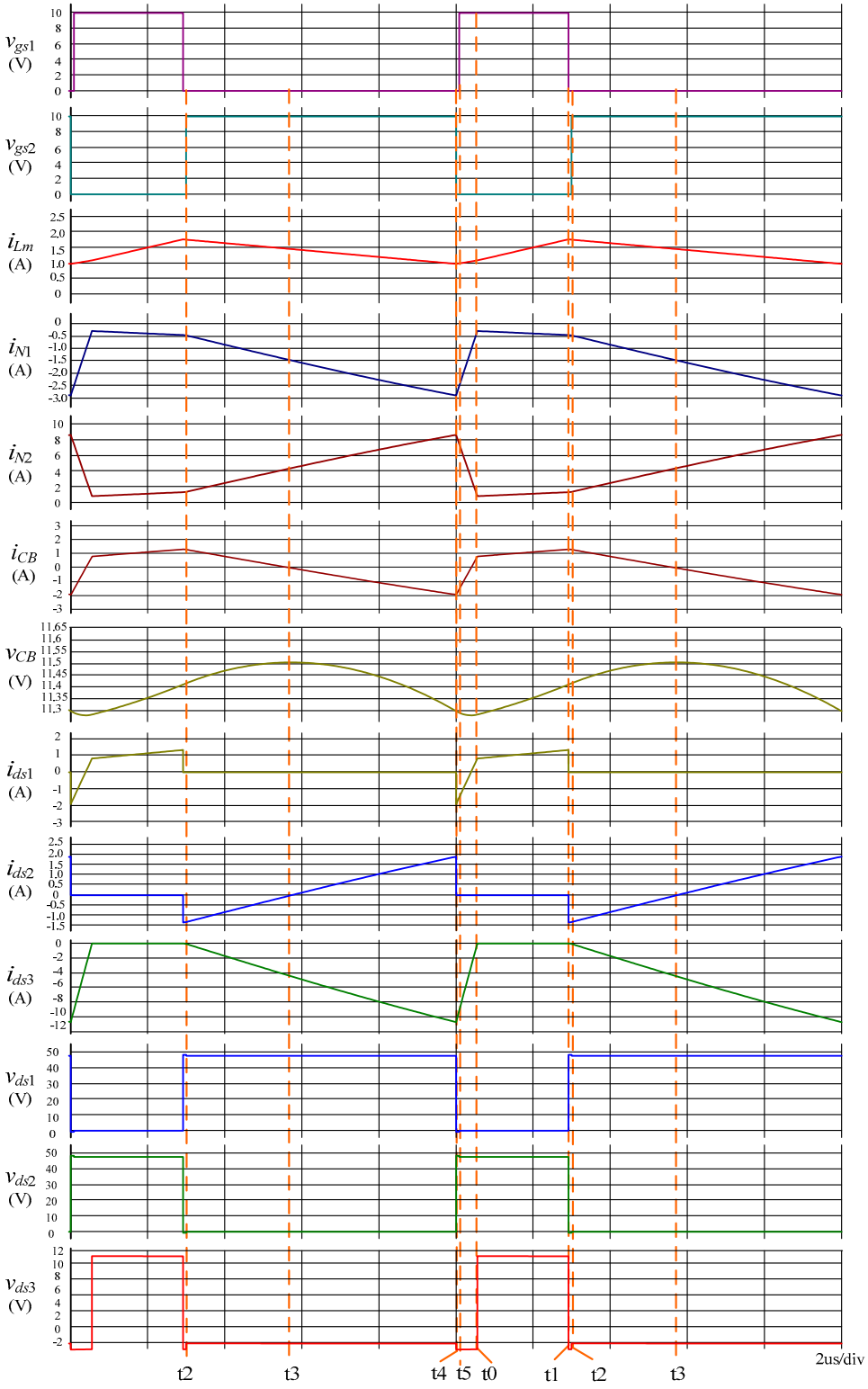
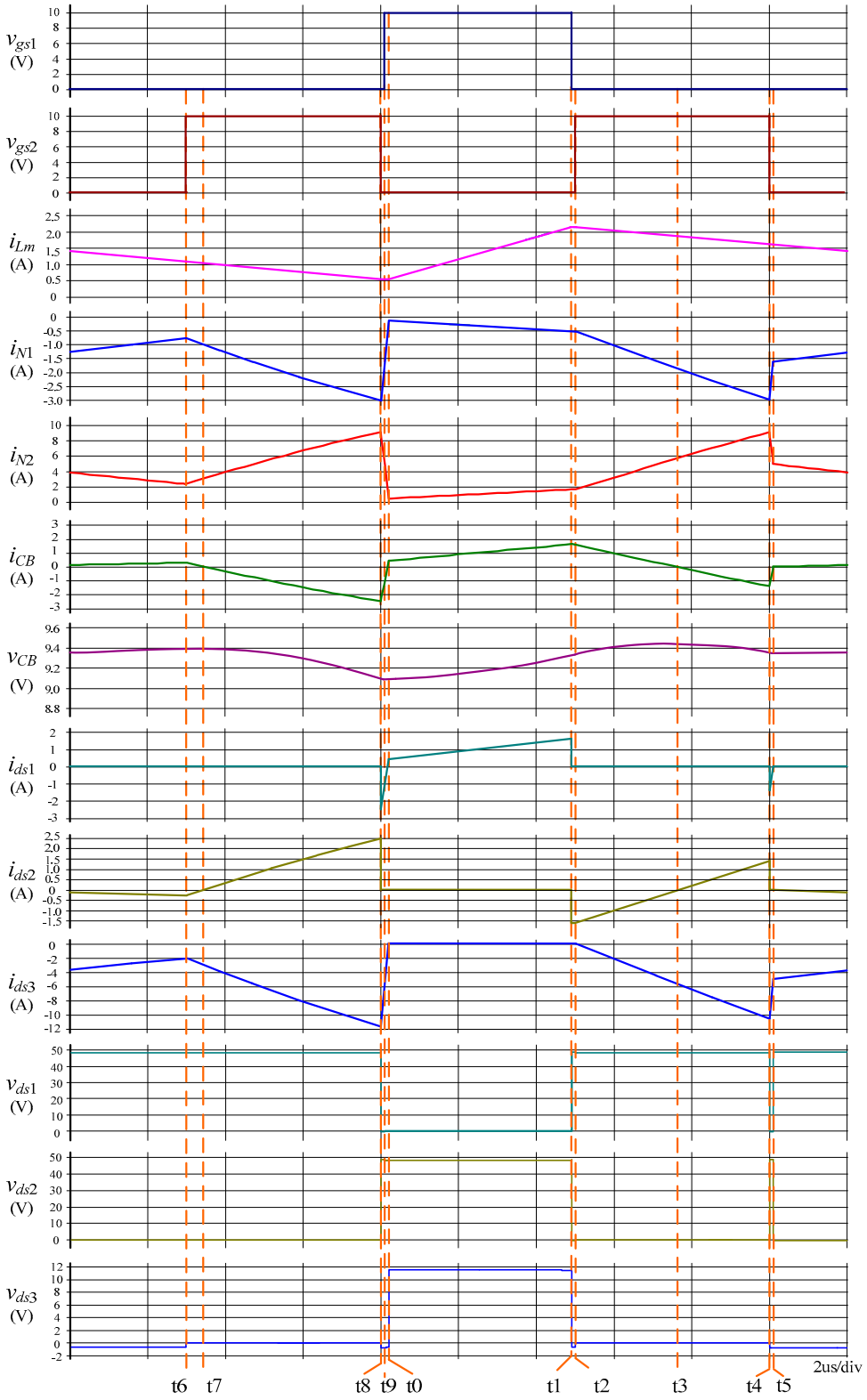


Figure 1. Circuit architecture in [20,21].



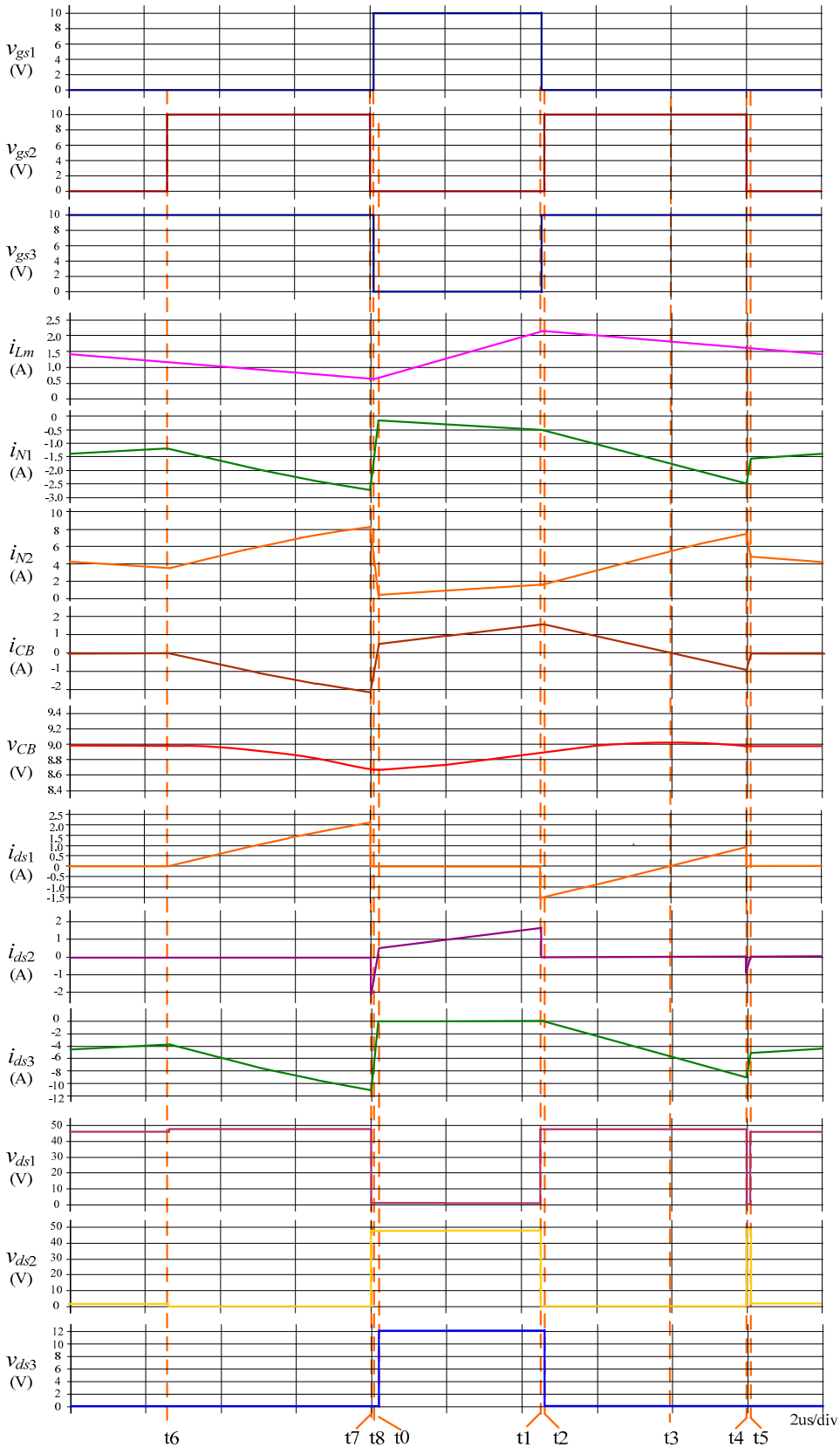
(**a**)

Figure 2. *Cont.*



(**b**)

Figure 2. *Cont.*



(**c**)

Figure 2. (**a**) Illustrated waveforms of Normal Mode; (**b**) Illustrated waveforms of Skip Mode 1; (**c**) Illustrated waveforms of Skip Mode 2.

3. Basic Circuit Operating Principles

There are six operating states in this circuit, which are described with reference to Figures 3–8. In all figures utilized to describe basic circuit operating behavior, orange is used to define the original current direction, whereas blue is used to indicate actual current direction.

3.1. Normal Mode

3.1.1. State 1

As shown in t0–t1 of Figure 3, Q_1 is turned on, but Q_2 and Q_3 are turned off. The input voltage V_{in} charges the capacitor C_B and magnetizes the magnetizing inductor L_m. Both the currents i_{N1} and i_{N2} are equal and increasing. During this stage, the input voltage V_{in} transmits energy to the output voltage V_o.

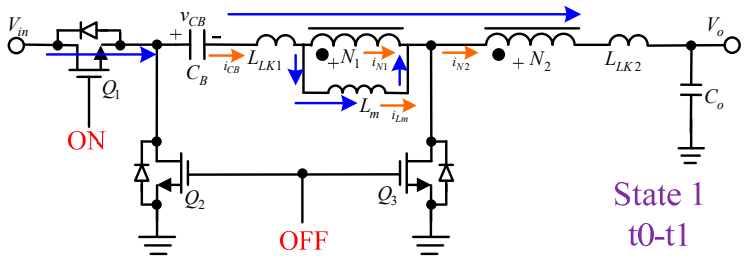


Figure 3. Current path in State 1 under Normal Mode.

3.1.2. State 2

As shown in t1–t2 of Figure 4, Q_1 is turned-off, and Q_2 and Q_3 remain off. This is the deadtime interval, and the currents i_{N1} and i_{N2} continue due to the leakage inductances L_{K1} and L_{K2}. The currents i_{N1} and i_{N2} flow through the body diodes of Q_2 and Q_3.

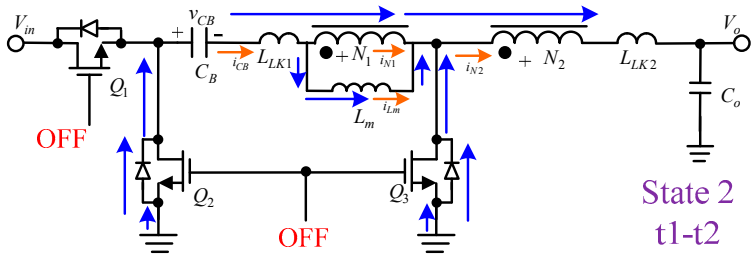


Figure 4. Current path in State 2 under Normal Mode.

3.1.3. State 3

As shown in t2–t3 of Figure 5, Q_1 remains off, but Q_2 and Q_3 are turned on. The currents i_{N1} and i_{N2} flow through body diodes of Q_2 and Q_3. At this instant, Q_2 and Q_3 are turned on with zero voltage switching (ZVS). As the current i_{N1} finally drops to zero, the circuit enters the next state.

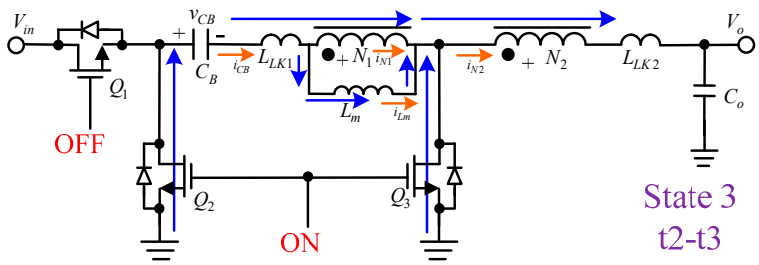


Figure 5. Current path in State 3 under Normal Mode.

3.1.4. State 4

As shown in t3–t4 of Figure 6, Q_1 remains off, and Q_2 and Q_3 remain on. During this stage, the energy stored in C_B will magnetize the winding N_1 in the opposite direction and transfer the energy to the winding N_2 and then to the output terminal in the transformer mode, so the currents i_{N1} and i_{N2} increase.

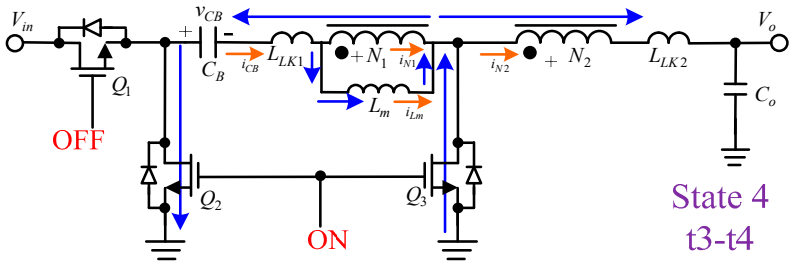


Figure 6. Current path in State 4 under Normal Mode.

3.1.5. State 5

As shown in t4–t5 of Figure 7, Q_1, Q_2, and Q_3 are turned off. During this stage, the free-wheeling current in the leakage inductance L_{LK1} of the winding N_1 will flow through the body diode of Q_1, so the voltage v_{ds1} reduces to zero. L_{LK1} is demagnetized continuously, and the energy stored in L_{LK1} is returned to the input voltage V_{in} and gradually decreases. During this interval, $i_{N1} < i_{N2}$. Since Q_3 is turned off, there is still excess current flowing through the body diode of Q_3. As i_{N1} rises to zero, it enters State 6.

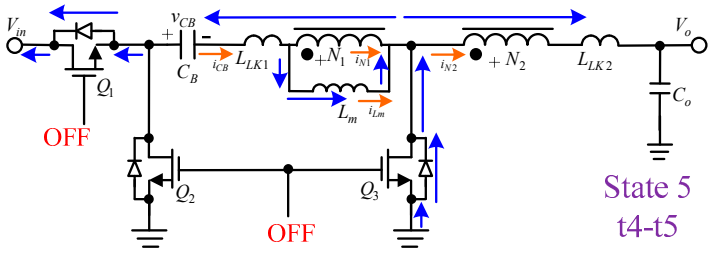


Figure 7. Current path in State 5 under Normal Mode.

3.1.6. State 6

As shown in t5–t0 of Figure 8, Q_1 is turned on, but Q_2 and Q_3 are still kept turned-off. Since the voltage v_{ds1} is zero in State 5, if Q_1 is turned on during this state, then Q_1 has ZVS turned on. In addition, due to the leakage inductance and i_{N1} being smaller than i_{N2}, there is still excess current flowing through Q_3, but Q_3 has been turned off, so the body diode of Q_3 is forced to conduct. As $i_{N1} = i_{N2}$, the current no longer flows through the body diode of Q_3 and it returns to State 1.

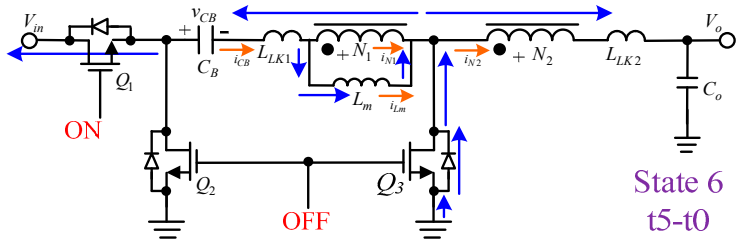


Figure 8. Current path in State 6 under Normal Mode.

3.2. Skip Mode 1

When this circuit is in Skip Mode 1 at light-load operation, there are nine operating states, which are described in Figure 9a–e. Among them, the behavior of t0–t5 is the same as Normal Mode, so only the actions of t5–t0 are described.

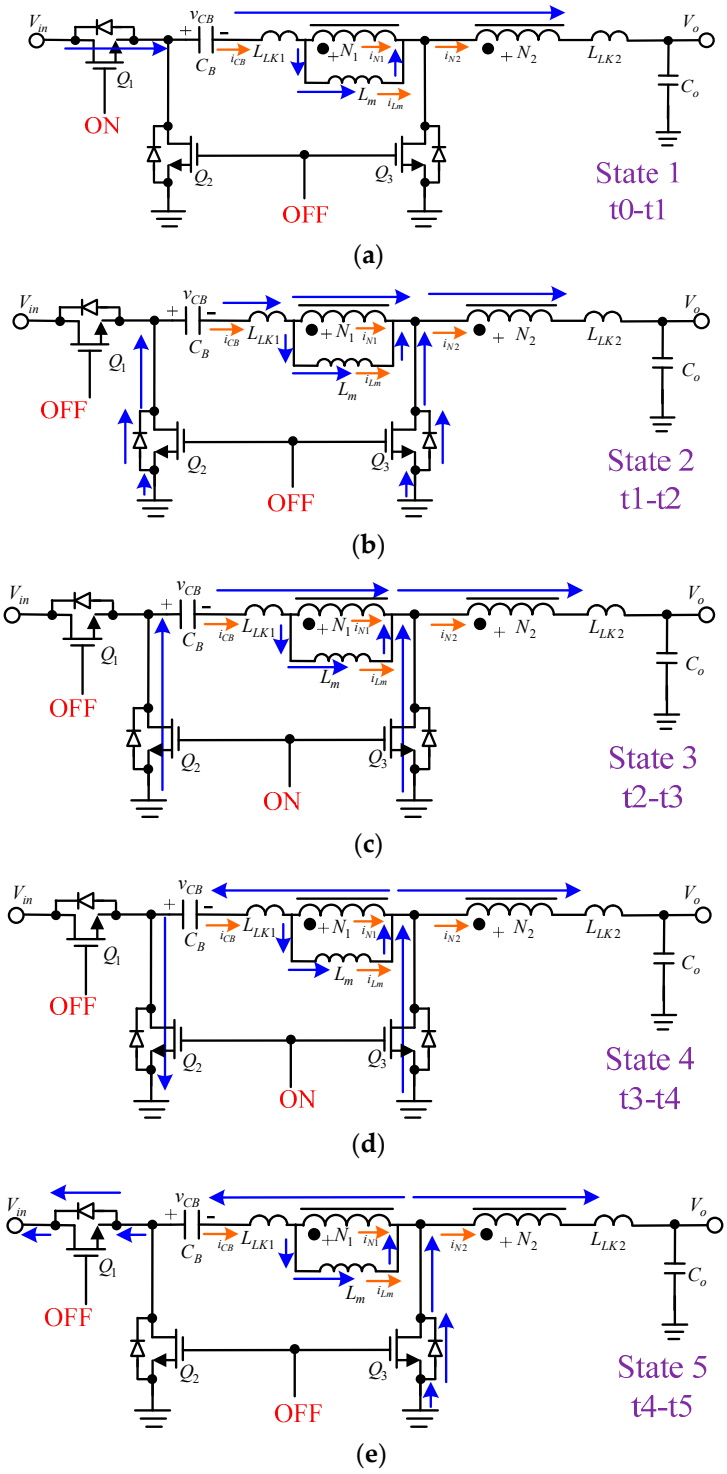


Figure 9. Current path in different state under Skip Mode 1: (**a**) State 1; (**b**) State 2; (**c**) State 3; (**d**) State 4; (**e**) State 5.

3.2.1. State 6

As shown in t5–t6 of Figure 10, after the demagnetizing of L_{LK1} in State 5 is completed, Q_1, Q_2, and Q_3 are all turned off at this time, but i_{Lk1} and i_{Lk2} continue to flow through the windings N_1 and N_2, so there is still current flowing through the body diode of Q_3.

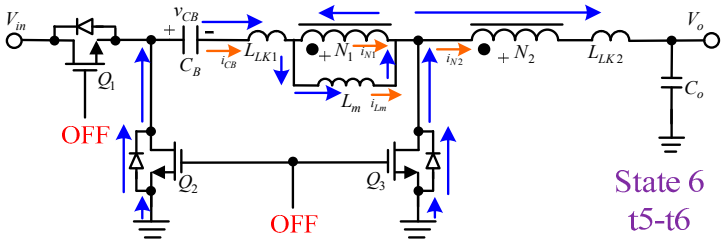


Figure 10. Current path in State 6 under Skip Mode 1.

3.2.2. State 7

As shown in t6–t7 of Figure 11, at this time Q_2 and Q_3 are turned on for the second time, the capacitor C_B magnetizes L_m, causing i_{Lm} to rise, and at the same time C_B is discharged to the output through the N_1 and N_2, which are under the transformer mode.

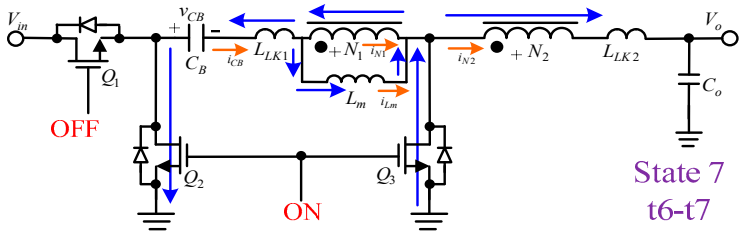


Figure 11. Current path in State 7 under Skip Mode 1.

3.2.3. State 8

As shown in t7–t8 of Figure 12, Q_2 and Q_3 are turned-off for the second time, so i_{LK1} flows through the body diode of Q_1, making v_{ds1} zero. Hence, Q_3 is turned on with ZVS.

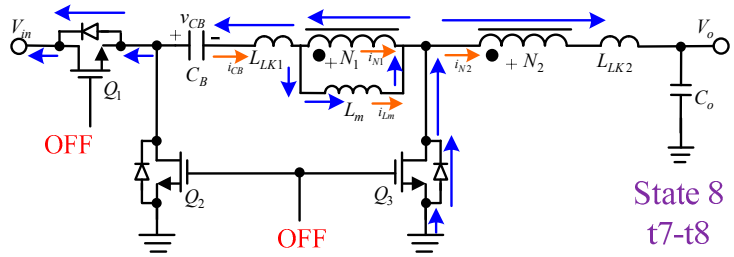


Figure 12. Current path in State 8 under Skip Mode 1.

3.2.4. State 9

As shown in t8–t0 of Figure 13, when v_{ds1} is zero, Q_1 is turned on, and Q_1 can be turned on with ZVS.

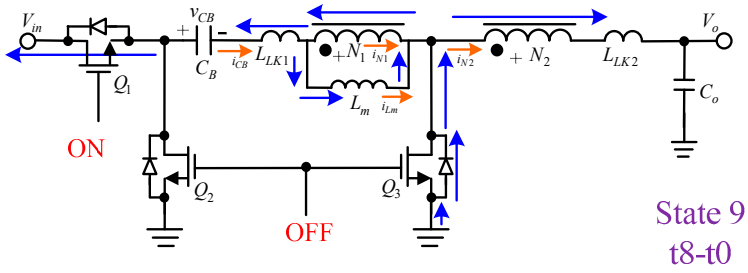
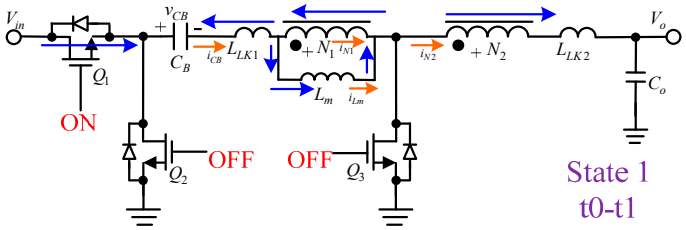


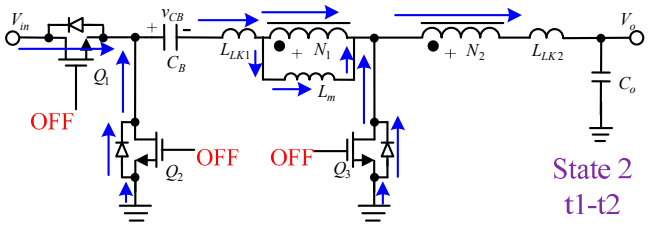
Figure 13. Current path in State 9 under Skip Mode 1.

3.3. Skip Mode 2

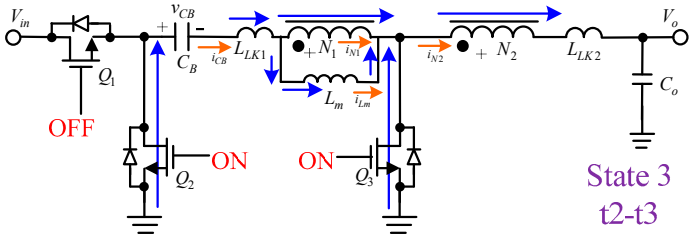
When this circuit is in Skip Mode 2 at light-load operation, there are nine operation states, which are described in Figure 14a–d. Among them, the behavior of t0–t4 is the same as Skip Mode 1, so only the actions of t4–t0 are described.



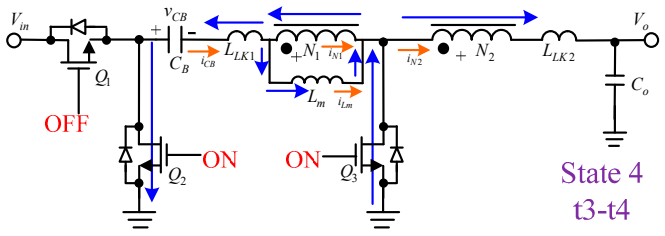
(**a**)



(**b**)



(**c**)



(**d**)

Figure 14. Current path in different state under Skip Mode 2: (**a**) State 1; (**b**) State 2; (**c**) State 3; (**d**) State 4.

3.3.1. State 5

As shown in t4–t5 of Figure 15, Q_1 and Q_2 are turned off. During this state, the free-wheeling current in leakage inductance L_{LK1} of the winding N_1 flows through the body diode of Q_1, so the voltage v_{ds1} reduces to zero. If Q_1 is turned on at this moment, ZVS is turned on. Although Q_1 is turned on, L_{LK1} is demagnetized continuously, and the energy stored in L_{LK1} is returned to V_{in} and gradually decreases. During this state, $i_{N1} < i_{N2}$. Since Q_3 is kept at the turned-on state, there is still excess current flowing through Q_3. As i_{N1} rises to zero, it enters State 6.

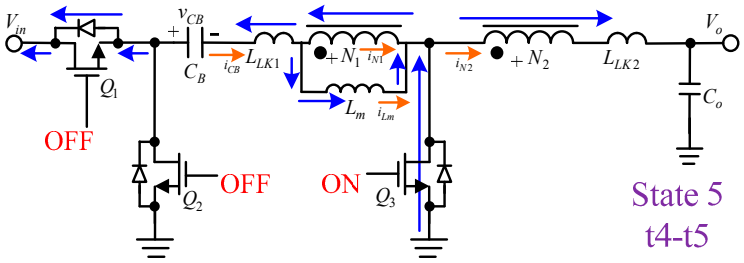


Figure 15. Current path in State 5 under Skip Mode 2.

3.3.2. State 6

As shown in t5–t6 of Figure 16, after the demagnetizing of L_{LK1} in State 5 is completed, Q_1, Q_2, and Q_3 are all turned off at this time, but i_{LK1} and i_{LK2} continue to flow through the windings N_1 and N_2, so there is still current flowing through the body diode of Q_3.

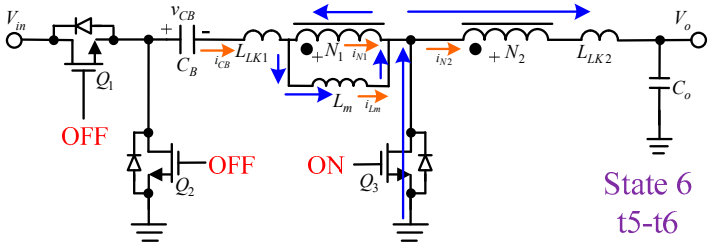


Figure 16. Current path in State 6 under Skip Mode 2.

3.3.3. State 7

As shown in t6–t7 of Figure 17, at this time, Q_2 is turned on for the second time, the capacitor C_B magnetizes L_m, causing i_{Lm} to rise, and at the same time C_B discharges the output through N_1 and N_2, which are under the transformer mode.

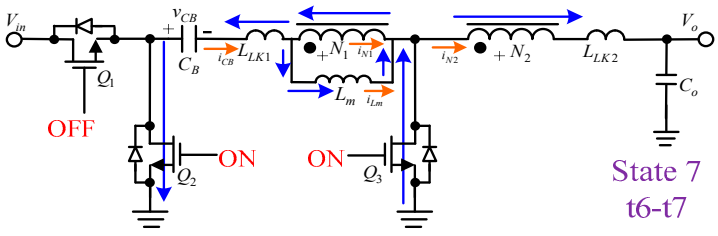


Figure 17. Current path in State 7 under Skip Mode 2.

3.3.4. State 8

As shown in t7–t8 of Figure 18, Q_2 and Q_3 are turned off for the second time, so i_{LK1} flows through the body diode of Q_1, making v_{ds1} zero. Hence, Q_3 is turned on with ZVS.

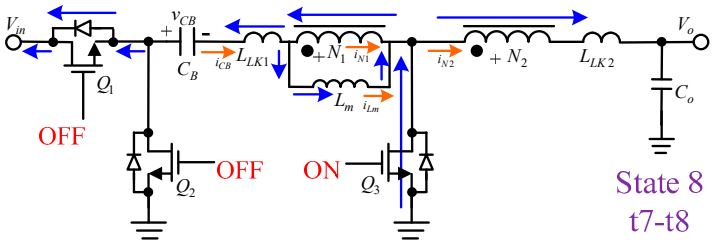


Figure 18. Current path in State 8 under Skip Mode 2.

3.3.5. State 9

As shown in t8–t0 of Figure 19, when v_{ds1} is zero, Q_1 is turned on at this time, and Q_1 can be turned on with ZVS.

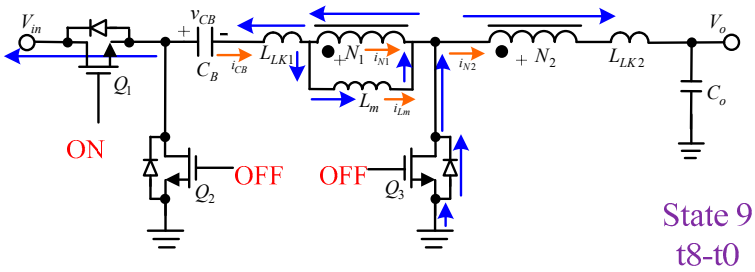


Figure 19. Current path in State 9 under Skip Mode 2.

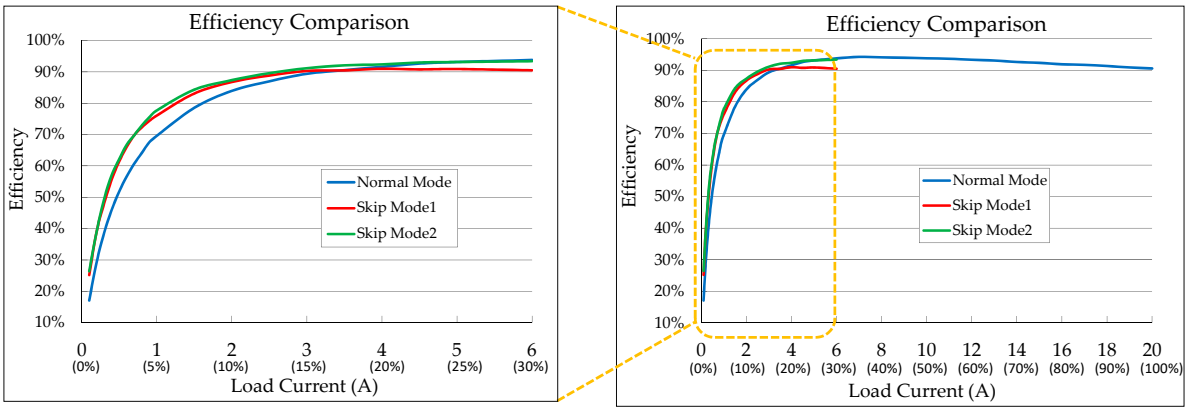
4. Experimental Results

The system parameters and components specifications are presented in Table 1.

Table 1. System requirements and component specifications.

Input voltage V_{in}	48 V
Output voltage V_o	2.5 V
Output rated current I_o	20 A
Switching frequency f_s	100 kHz
Capacitor C_B	20 uF/50 V TDK MLCC
Coupled inductor	N_1:N_2 = 24:8 with L_m = 87.1 uH, L_{LK1} = 3.94 uH, and L_{LK2} = 0.69 uH MPP core of Micrometals Co. (Colorado Springs, CO, USA), model T106-M125
Capacitor C_o	2 × 1000 uF solid electrolytic capacitor
Q_1, Q_2	AON6244, withstand voltage 60 V, 4.7 mΩ, Alpha and Omega Co. (Sunnyvale, CA, USA)
Q_3	AON6512, withstand voltage 30 V, 1.7 mΩ, Alpha and Omega Co.

First, the conversion efficiency in Normal Mode, Skip Mode 1, and Skip Mode 2 are measured. As shown in Figure 20, both Skip Mode 1 and Skip Mode 2 can provide better conversion efficiency than Normal Mode when the load is below 15% of rated load, so the controller can enter skip mode to improve conversion efficiency up to 5%.



(**a**) (**b**)

Figure 20. Efficiency comparison at light load among Normal Mode, Skip Mode 1, and Skip Mode 2: (**a**) from zero to 30% of rated load; and (**b**) from zero to rated load.

Figures 21–23 show the gate driving signals for Normal Mode, Skip Mode 1, and Skip Mode 2. Figure 24 shows the waveforms i_{N1} and i_{N2} in Normal Mode under different load levels. Figure 24 shows that, as the output current increases, the current ripples of i_{N1} and i_{N2} also increase. Figure 25 shows the waveforms i_{N1} and i_{N2} under different load levels in Skip Mode 1. After Q_1 is turned off, Q_2 is turned on twice in succession. When Q_2 is turned on for the first time, i_{N1} is higher and transmits more energy to the output terminal. At the second ON, i_{N2} is lower and transmits less energy to the output terminal. Figure 26 shows the waveforms i_{N1} and i_{N2} under different load levels in Skip Mode 2. After Q_1 is turned off, Q_2 is turned on twice in succession. When Q_2 is turned on for the first time, i_{N1} is higher and transmits more energy to the output terminal. At the second ON, i_{N2} is lower and transmits less energy to the output terminal. Figure 27 shows the waveforms v_{C1} and i_{C1} under different loads in Normal Mode. Figure 28 shows the waveforms v_{C1} and i_{C1} under different load levels in Skip Mode 1. Figure 29 shows that v_{C1} and i_{C1} under different loads in Skip Mode 2. In Figures 27–29, the voltages across C_B are almost the same.

Figures 30–32 show the output voltage ripples $v_{o\,(AC)}$ operating in Normal Mode, Skip Mode 1, and Skip Mode 2, respectively. In these three figures, the difference in output voltage ripple between Normal Mode and Skip Mode 1 below the output current of 2 A is slight, but Skip Mode 1 has a little higher output voltage ripple at 4 A than Normal Mode. Below the output current of 1 A, Skip Mode 2 has a slightly higher voltage ripple than Skip Mode 1, but both are similar above the output current of 2 A.

Figures 33 and 34 are the waveforms for the mode exchange between Normal Mode and Skip Mode 1 under different load levels. Under different output current levels, the mode exchange has a slight effect on v_o.

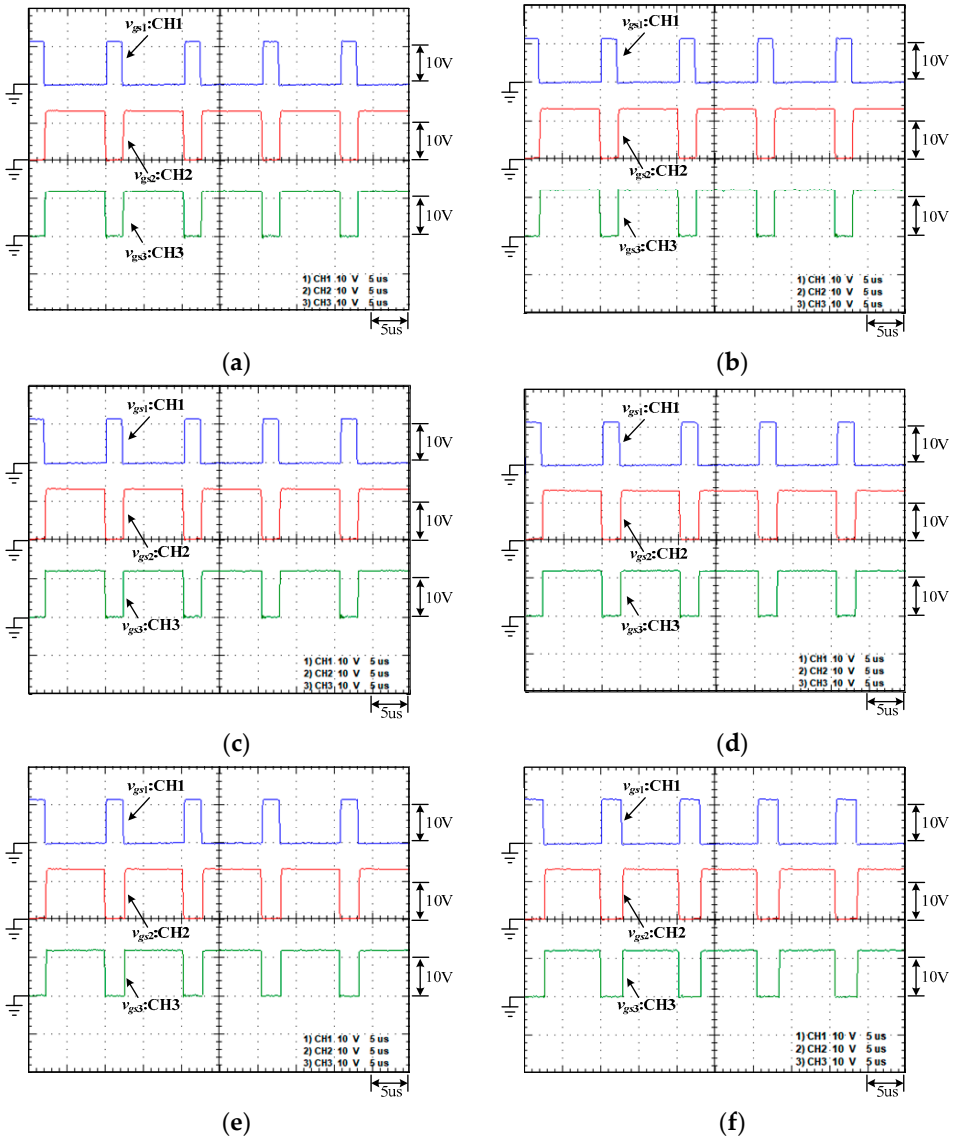


Figure 21. v_{gs1}, v_{gs2}, and v_{gs3} under Normal Mode: (**a**) 0.2 A; (**b**) 1 A; (**c**) 2 A; (**d**) 4 A; (**e**) 10 A; and (**f**) 20 A.

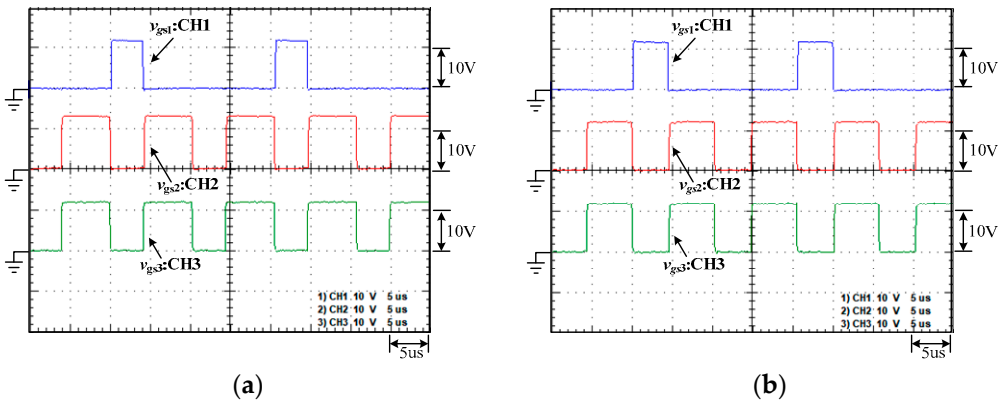


Figure 22. *Cont.*

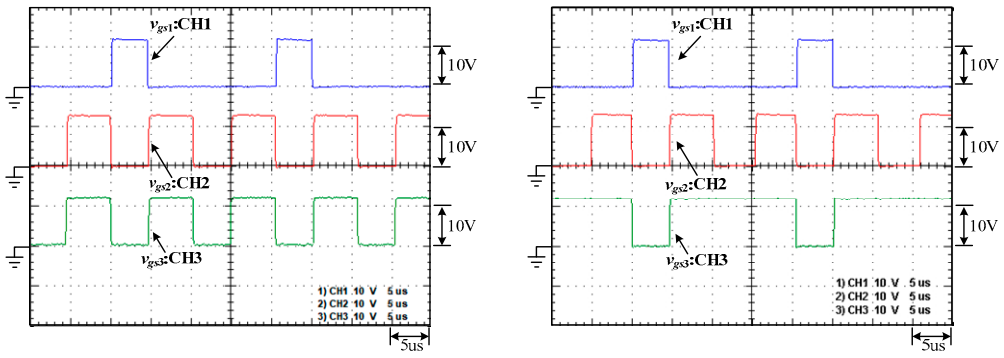


Figure 22. v_{gs1}, v_{gs2}, and v_{gs3} under Skip Mode 1: (**a**) 0.2 A; (**b**) 1 A; (**c**) 2 A; and (**d**) 4 A.

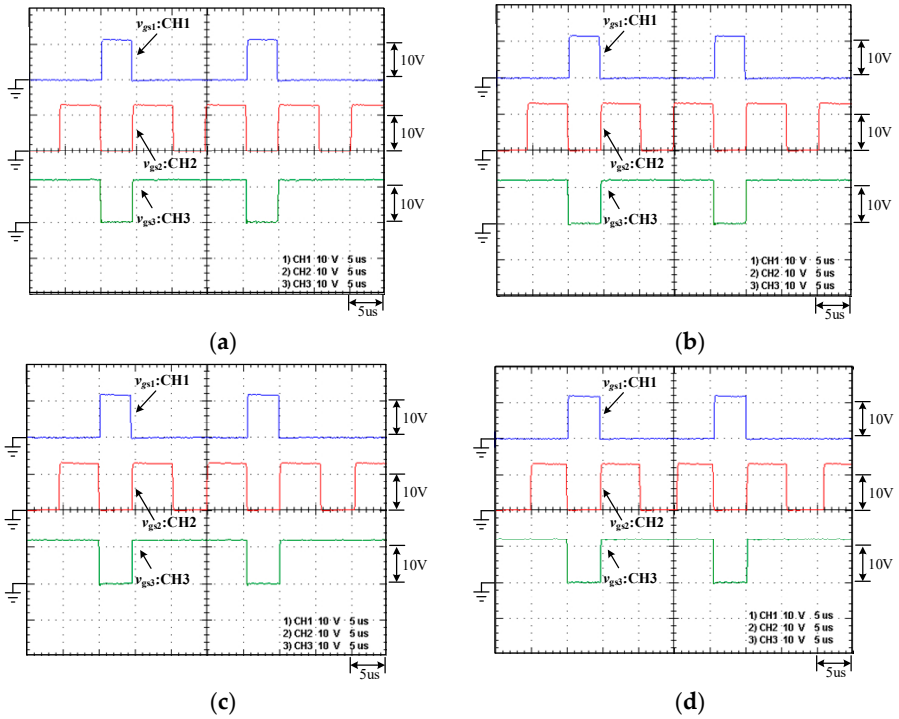


Figure 23. v_{gs1}, v_{gs2}, and v_{gs3} under Skip Mode 2: (**a**) 0.2 A; (**b**) 1 A; (**c**) 2 A; and (**d**) 4 A.

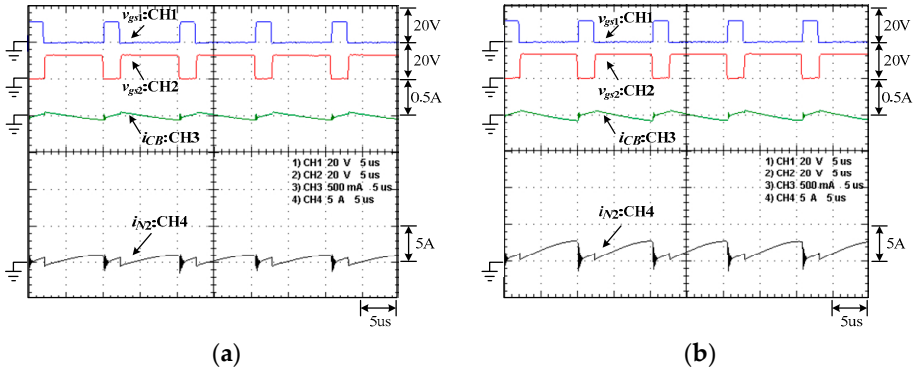


Figure 24. *Cont.*

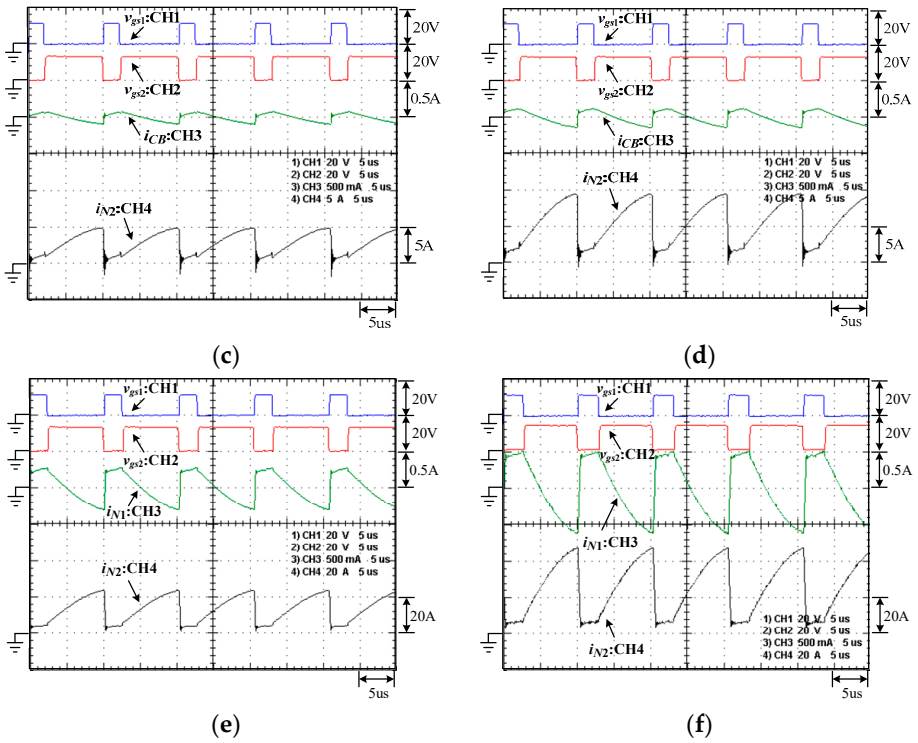


Figure 24. v_{gs1}, v_{gs2}, i_{CB}, and i_{N2} under Normal Mode: (**a**) 0.2 A; (**b**) 1 A; (**c**) 2 A; (**d**) 4 A; (**e**) 10 A; and (**f**) 20 A.

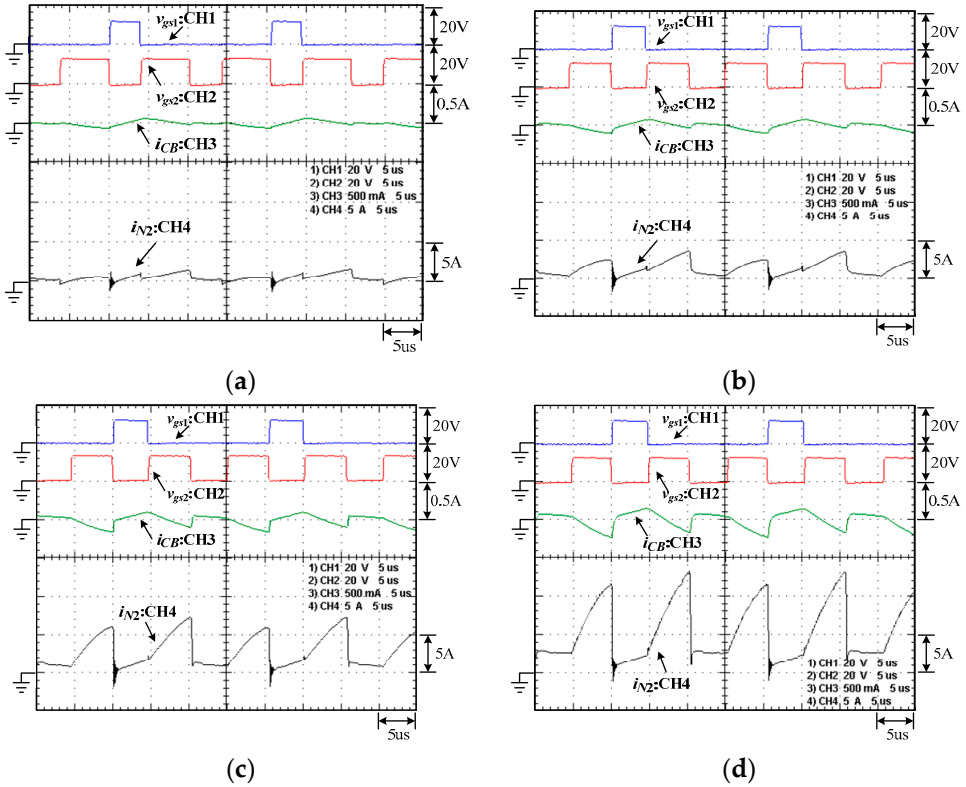


Figure 25. v_{gs1}, v_{gs2}, i_{CB}, and i_{N2} under Skip Mode 1: (**a**) 0.2A; (**b**) 1A; (**c**) 2A; and (**d**) 4A.

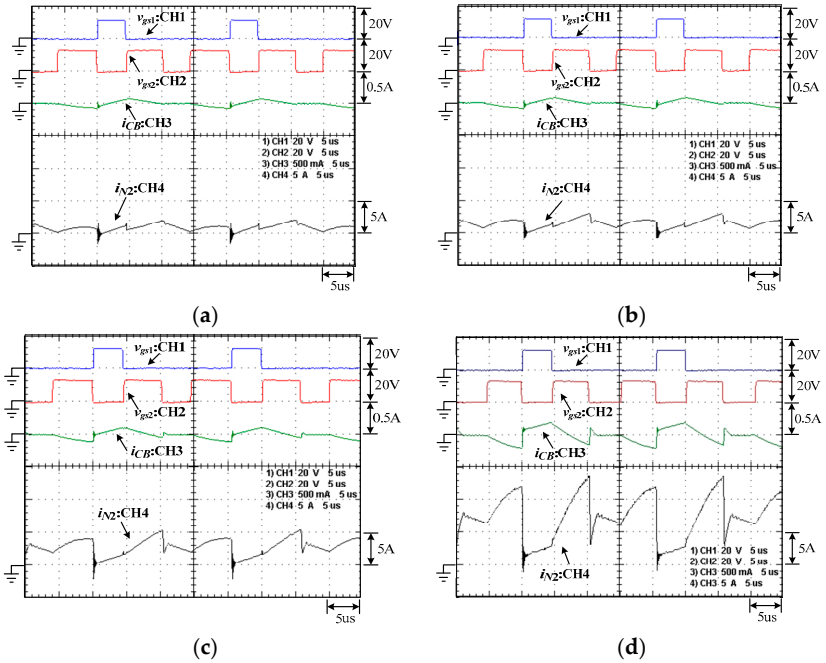


Figure 26. v_{gs1}, v_{gs2}, i_{CB}, and i_{N2} under Skip Mode 2: (**a**) 0.2 A; (**b**) 1 A; (**c**) 2 A; and (**d**) 4 A.

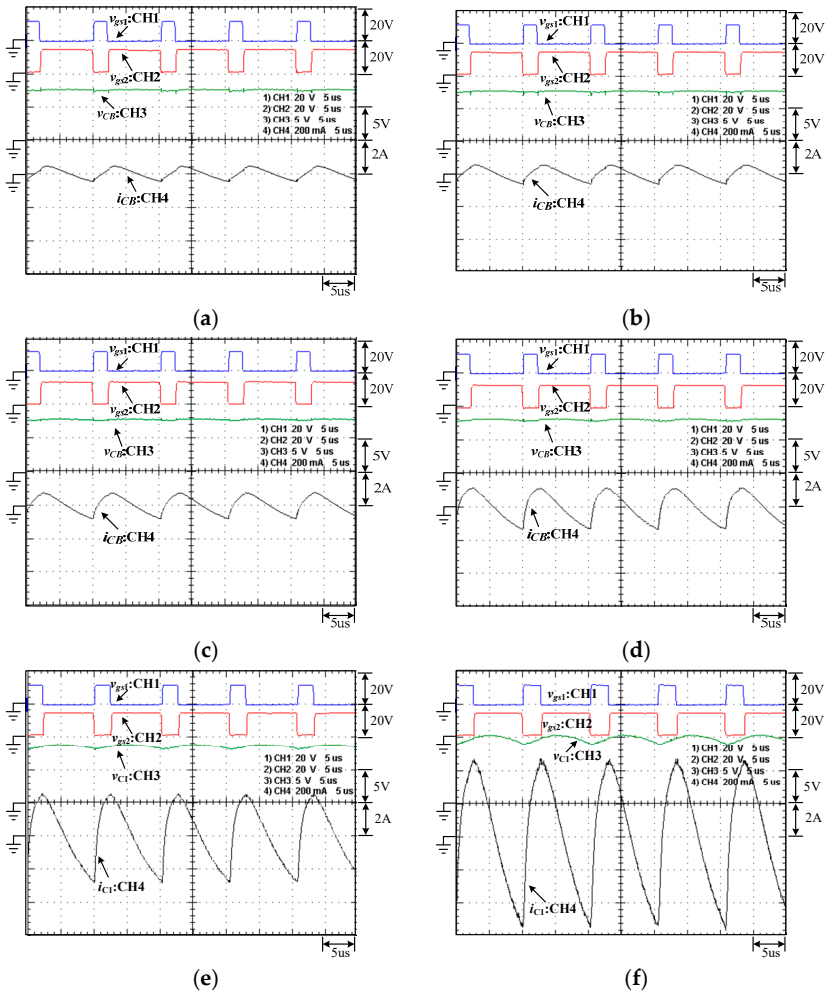


Figure 27. v_{gs1}, v_{gs2}, v_{CB}, and i_{CB} under normal Mode 2: (**a**) 0.2 A; (**b**) 1 A; (**c**) 2 A; (**d**) 4 A; (**e**) 10 A; and (**f**) 20 A.

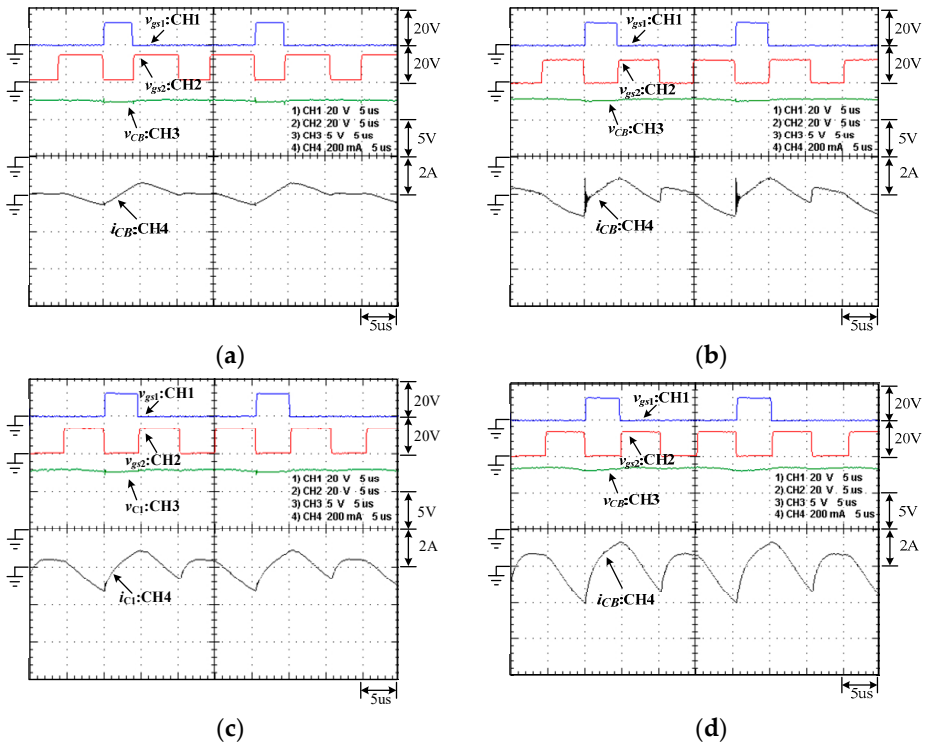


Figure 28. v_{gs1}, v_{gs2}, v_{CB}, and i_{CB} under Skip Mode 2: (**a**) 0.2 A; (**b**) 1 A; (**c**) 2 A; and (**d**) 4 A.

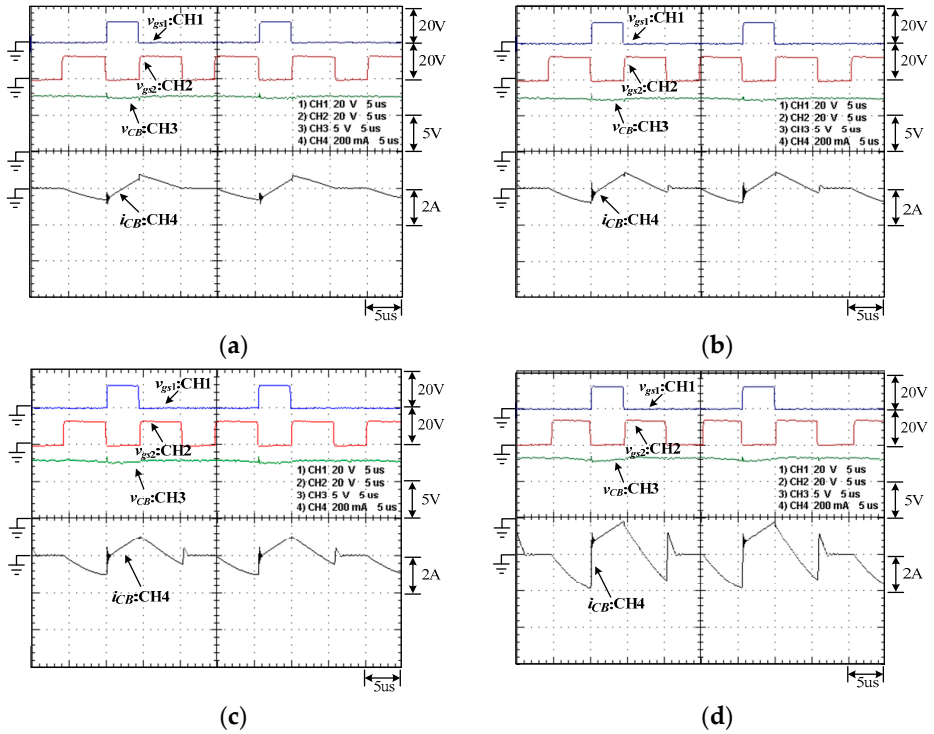


Figure 29. v_{gs1}, v_{gs2}, v_{CB}, and i_{CB} under Skip Mode 2: (**a**) 0.2 A; (**b**) 1 A; (**c**) 2 A; and (**d**) 4 A.

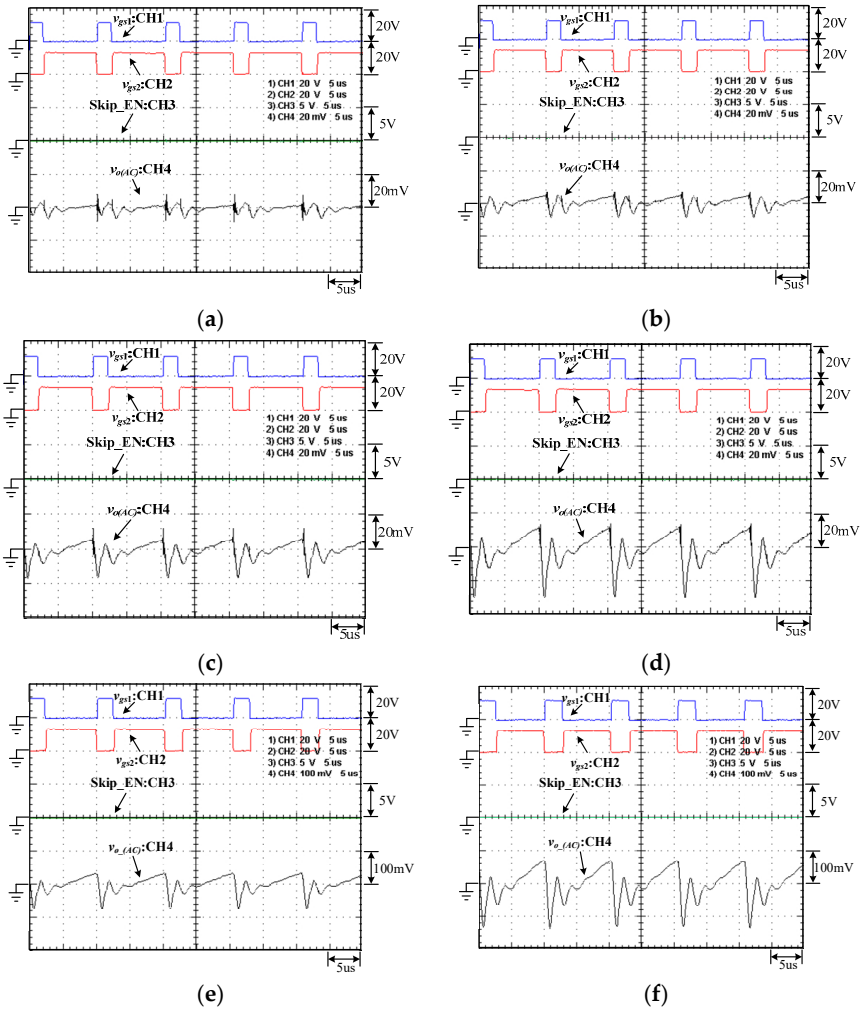


Figure 30. v_{gs1}, v_{gs2}, Skip_EN, and $v_{o(AC)}$ under Normal Mode: (**a**) 0.2 A; (**b**) 1 A; (**c**) 2 A; (**d**) 4 A; (**e**) 10 A; and (**f**) 20 A.

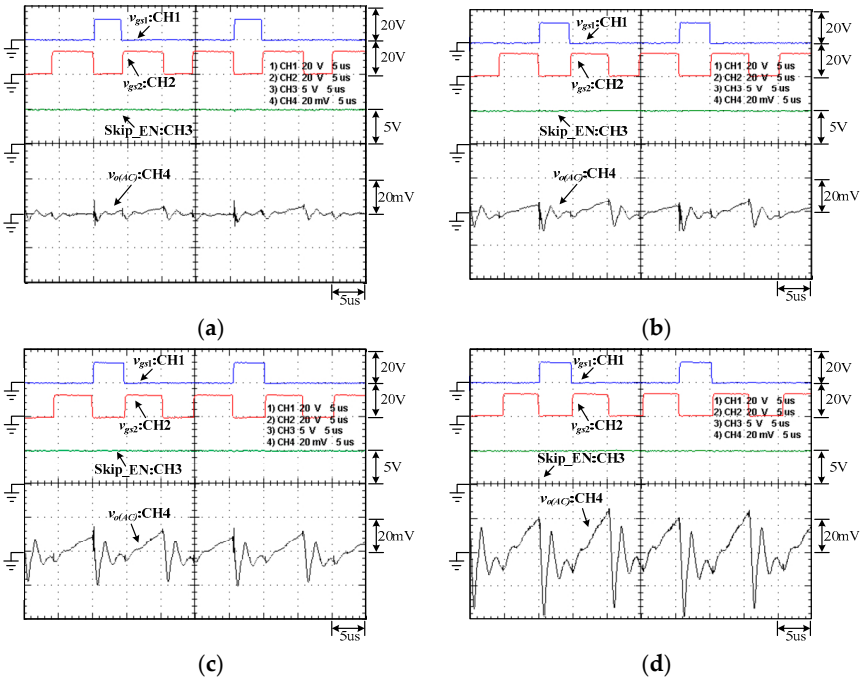


Figure 31. v_{gs1}, v_{gs2}, Skip_EN, and $v_{o(AC)}$ under Skip Mode 1: (**a**) 0.2 A; (**b**) 1 A; (**c**) 2 A; and (**d**) 4 A.

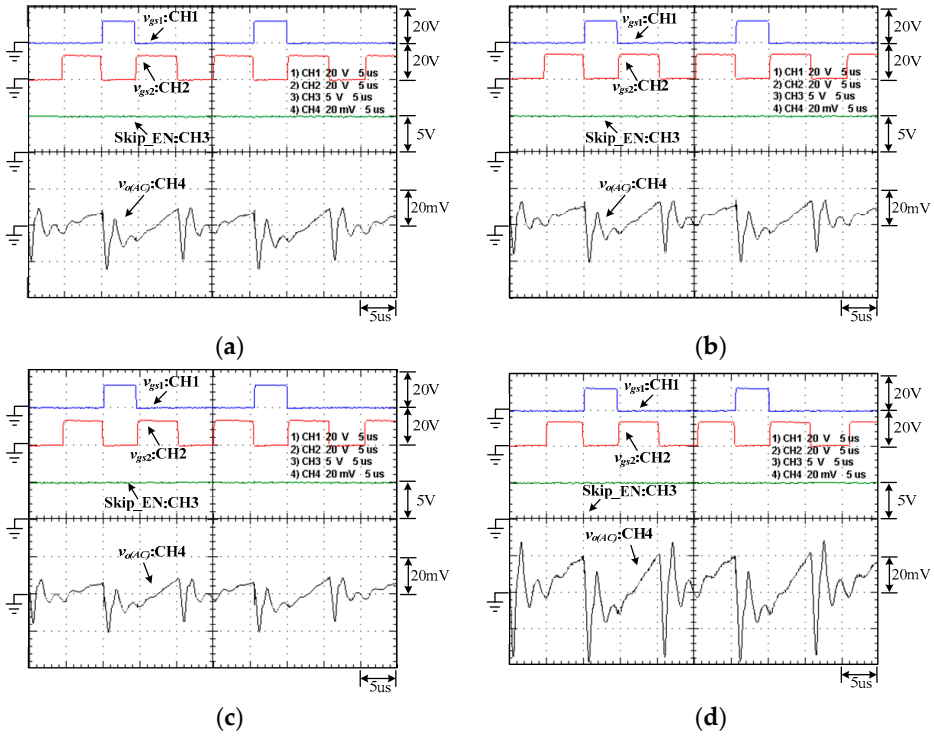


Figure 32. v_{gs1}, v_{gs2}, Skip_EN, and $v_{o(AC)}$ under Skip Mode 2: (**a**) 0.2 A; (**b**) 1 A; (**c**) 2 A; and (**d**) 4 A.

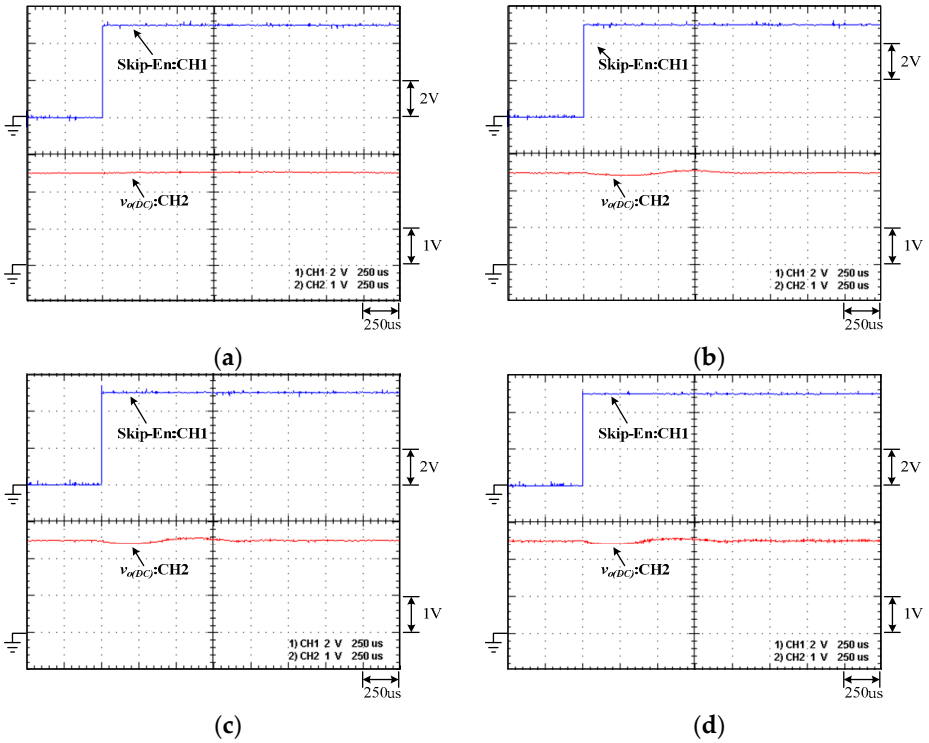


Figure 33. SkipEN and $v_{o(DC)}$ under Normal Mode switched to Skip Mode 1: (**a**) 0.2 A; (**b**) 1 A; (**c**) 2 A; and (**d**) 4 A.

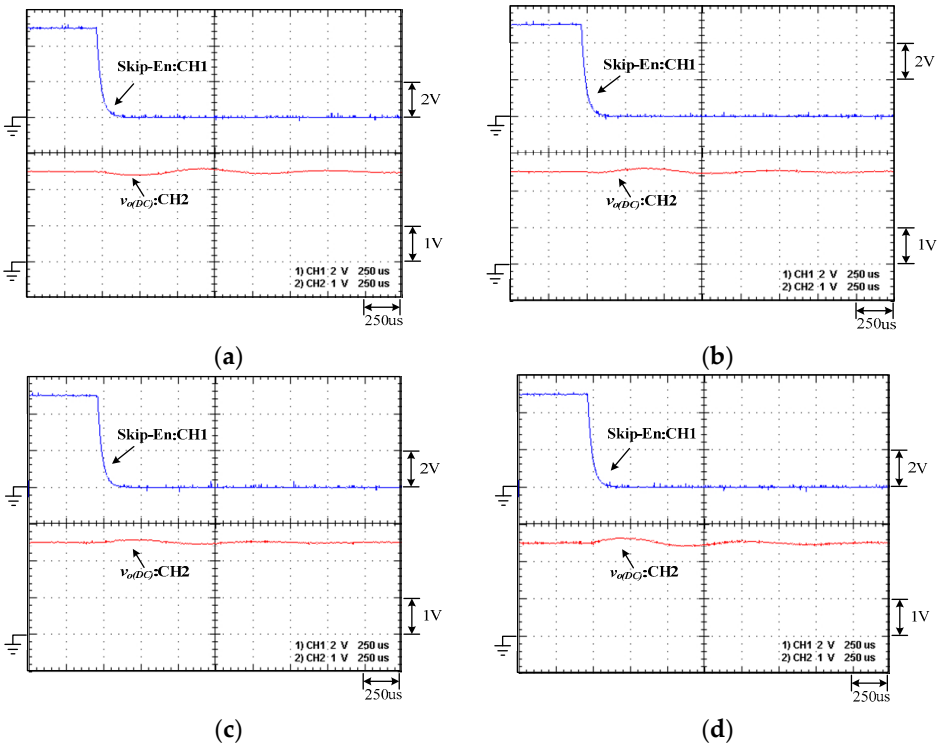


Figure 34. SkipEN and $v_{o(DC)}$ under Skip Mode 1 switched to Normal Mode: (**a**) 0.2 A; (**b**) 1 A; (**c**) 2 A; and (**d**) 4 A.

Figures 35 and 36 are the waveforms for the mode exchange between Normal Mode and Skip Mode 2 under different output current levels. Under different output current levels, the mode exchange has a slight effect on v_o.

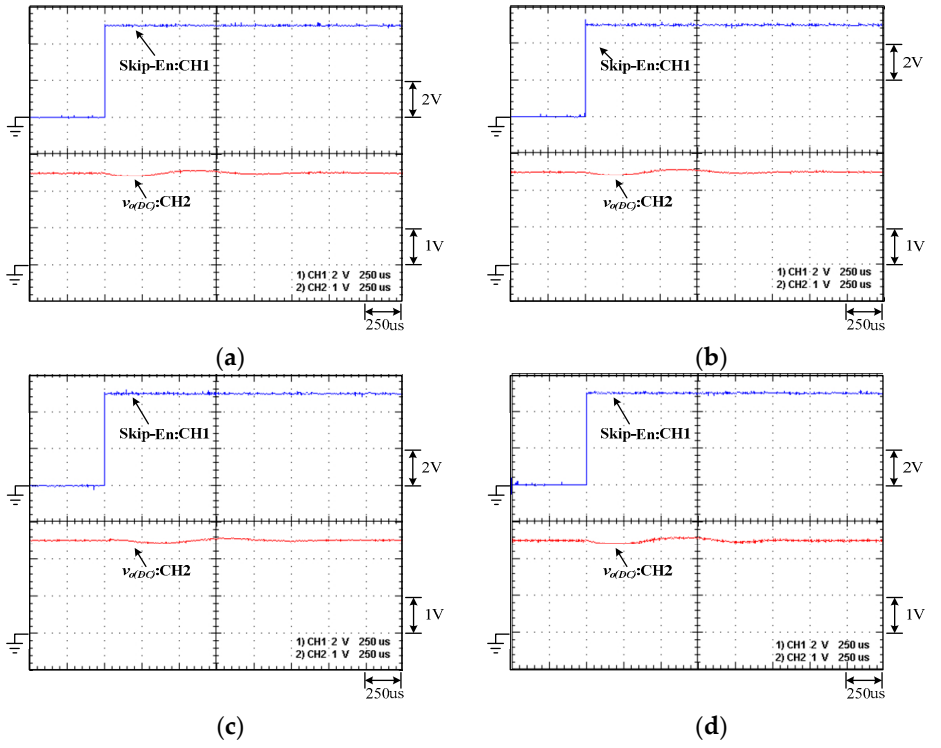


Figure 35. SkipEN and $v_{o(DC)}$ under Normal Mode switched to Skip Mode 2: (**a**) 0.2 A; (**b**) 1 A; (**c**) 2 A; and (**d**) 4 A.

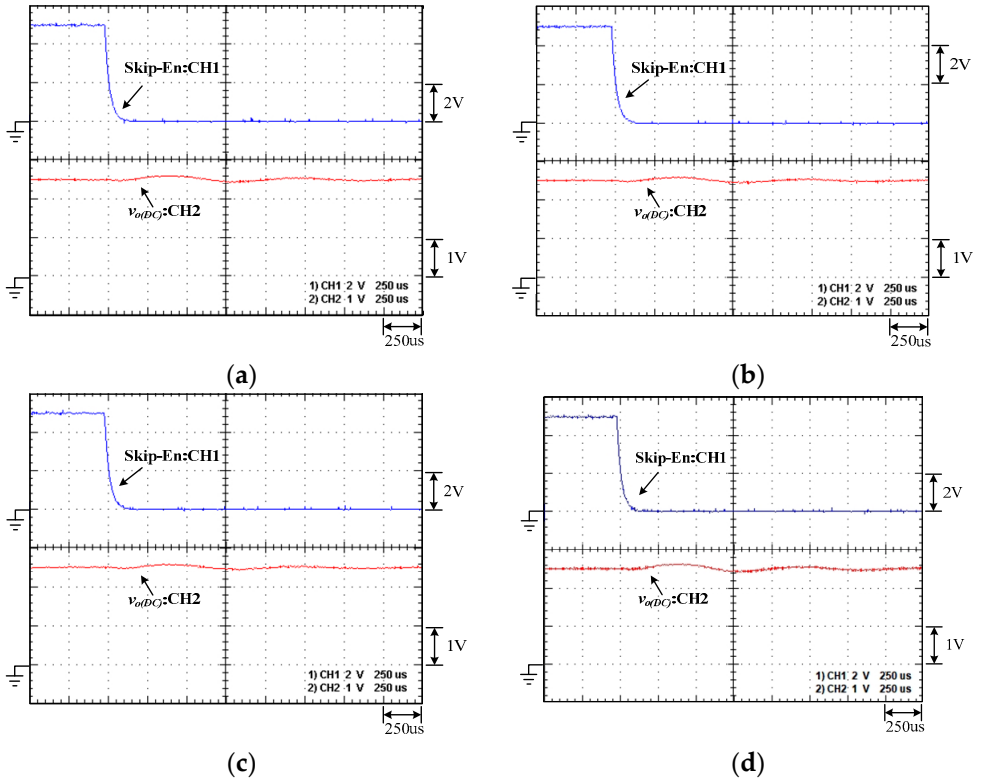


Figure 36. SkipEN and $v_{o(DC)}$ under Skip Mode 2 switched Normal Mode: (**a**) 0.2 A; (**b**) 1 A; (**c**) 2 A; and (**d**) 4 A.

Accordingly, the transient responses due to mode exchange between Normal Mode and Skip Mode 1 and between Normal Mode and Skip Mode 2 are quite similar.

5. Discussion

The light-load efficiency and the output voltage ripple discussed herein are under the condition that the traditional PWM control strategy used in [20,21] is considered as Normal Mode. Therefore, based on the same circuit structure as in [20,21], this paper presents two skip mode control strategies to improve the light-load efficiency. Although the switching frequency used in these two strategies is reduced, the transferred energy is unchanged, but the output voltage ripple is influenced to some extent as compared to Normal Mode. In addition, the mode exchange among the three control strategies is very smooth. The proposed PWM control strategies can be applied to the structures in [20,21] to improve the light-load efficiency.

6. Conclusions

This paper presents two PWM control strategies to increase the efficiency at the light-load condition for the high step-down converter. The experimental results show that the light-load efficiency can be effectively improved without generating a larger output voltage ripple. The skip mode is provided to improve the light-load efficiency up to 5% when the load is below 15% of rated load. The light-load efficiency can be improved by two types of modified PWM control sequence as Skip Mode 1 and Skip Mode 2. Furthermore, the mode exchange is quite smooth, and the output voltage ripple does not change significantly.

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Conflicts of Interest: The authors declare no conflict of interest.

Abbreviations

AC	Alternating Current
CCM	Continuous Current Mode
DC	Direct Current
IC	Integrated Circuit
POL	Power on Load
PWM	Pulse-Width-Modulated
ZVS	Zero Voltage Switching

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