


Article

A Broadband Asymmetrical GaN MMIC Doherty Power Amplifier with Compact Size for 5G Communications

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Abstract: This paper proposes a broadband asymmetrical monolithic microwave integrated circuit (MMIC) Doherty power amplifier (DPA) using 0.25- μm gallium-nitride process with a compact chip size of $2.37 \times 1.86 \text{ mm}^2$ for 5G communication. It adopts an unequal Wilkinson's power divider with a ratio of 2.5:1, where 71.5% of the total power is transferred to the main amplifier for higher gain. Different input matching networks are used to offset phase difference while completing impedance conversion. This design also applies a novel topology to solve the problem of large impedance transformer ratio (ITR) in conventional DPA, and it optimizes the ITR from 4:1 to 2:1 for wider band. Moreover, most of the components of the DPA including power divider and matching networks use lumped inductors and capacitors instead of long transmission line (TL) for a smaller space area. The whole circuit is designed and simulated using Agilent's advanced design system (ADS). The simulated small-signal gain of DPA is 8–11 dB and the saturation output power is more than 39.5 dBm with 800 MHz band from 4.5 GHz to 5.3 GHz. At 6-dB output power back-off, the DPA demonstrates 38–41.3% power added efficiency (PAE), whereas 44–54% PAE is achieved at saturation power.

Keywords: asymmetrical; Doherty power amplifier (DPA); 5G; monolithic microwave integrated circuit (MMIC); gallium-nitride (GaN)



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1. Introduction

To meet increasing demands for high data transmission speed and low transmission delay, 5th generation (5G) wireless systems have been formulated, which adopt new complex modulation schemes, such as orthogonal frequency division multiplexing (OFDM) [1]. This modulation can heavily enhance the spectrum utilization, but it will also generate unexpected high peak-to-average power ratio (PAPR) signals at the same time. The appearance of high PAPR signals enforces the power amplifiers to be operated at the back-off level from its saturated power, leading to low efficiency. Generally, base stations need power amplifiers with high efficiency at the back-off level to cut back the cost of cooling systems and extend battery lifetime. To enhance the efficiency at output power back-off (OPBO), various techniques have been proposed, such as dynamic biasing [2], harmonics tuning [3] and Doherty power amplifier (DPA) [4]. DPA has been adopted in this paper due to its concise circuit structure. The conventional DPA, consisting of two amplifiers operating at Class-AB for main amplifier and Class-C for auxiliary amplifier and two $\lambda/4$ transmission lines (TLs) for phase compensation and impedance transformation, utilizes active load

impedance modulation to improve efficiency at OPBO, as shown in Figure 1a. However, this implementation suffers from a narrow bandwidth which is less than 10% due to the dispersion behavior of $\lambda/4$ TLs, and DPA performance deteriorates outside the center frequency. Considering the broadband requirement of 5G for high-speed communication, the way to expand the bandwidth of DPA has become the focus of studies [5–7].

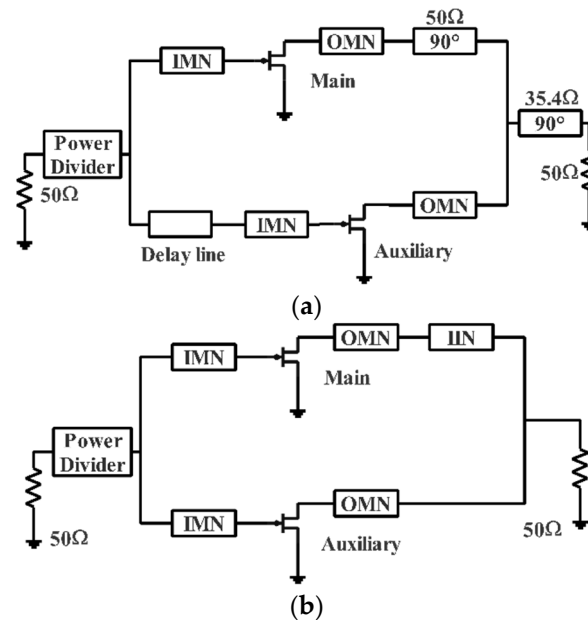


Figure 1. (a) The conventional Doherty power amplifier (DPA) (up); (b) The proposed asymmetric DPA (down).

The band below 6 GHz and millimeter wave band are in a new frequency range of 5G communication, which owns huge bandwidth for high-speed signal transmission. Due to the large path loss and sensitivity to raindrops, the application of the millimeter wave has many limitations, generally it can only be used indoors. Therefore, the band sub-6 GHz becomes the primary goal of research institutes and commercialization because of its easy-to-implement feature. On the other hand, the gallium-nitride (GaN) high electron-mobility transistor (HEMT) technology significantly improved the performance of radio frequency (RF) circuits, such as power amplifier (PA). Compared with traditional gallium-arsenide (GaAs) technology [8] GaN processes can not only achieve higher frequency, but also greater power density due to their large band gap. In addition, massive multiple-input multiple-output (MIMO) technology is adopted in base station for 5G communication, which contains over a hundred monolithic microwave integrated circuit (MMIC) power amplifiers for higher efficiency. Thus, miniaturization is another important issue for DPA used in base stations [9,10]. Many studies about high efficiency DPA used in 5G communication have been reported [11–17]. A compact transmission line network is used to invert impedance in [15] for a high efficiency at OPBO, but it only shows a good performance at single frequency. The research in [17] utilizes a mixed topology of lumped and distributed components to get optimum performance and a minimum chip size. Similarly, the effective bandwidth is extremely narrow, with only 200 MHz at a center frequency of 4.9 GHz. The three-way DPA demonstrated in [18–22] can indeed obtain high efficiency at more than 8-dB back-off. However, one more branch means more power loss and larger size of circuit. Moreover, various methods are applied to improve the performance of DPA [23–26]. This presents a new bandwidth enhancement technique by exploiting transformers and output-referred parasitic capacitances of the carrier and peaking transistors of DPA to achieve a 1500 MHz bandwidth, from 4.5 GHz to 6.0 GHz. Nevertheless, the efficiency is less than 30% at 6-dB back-off, which is considered to be improved.

In response to the increased demands of high efficiency at OPBO, broadband and miniaturization, this paper using HIWAFER 0.25 μm GaN technology designs a sub-6 GHz compact asymmetrical MMIC DPA with a chip size of only $2.37 \times 1.86 \text{ mm}^2$ that contains two $10 \times 100 \mu\text{m}$ devices, as shown in Figure 1b. An asymmetrical Wilkinson's power divider is introduced to transfer more power to main amplifier for higher gain and delay the opening of the auxiliary amplifier to ensure the depth of back-off. The proposed DPA's matching networks and power divider are made of lumped inductors and capacitors instead of TL for a reasonable chip area. Meanwhile, input matching networks (IIN) can offset the difference of phase, which is generated by bias condition and output matching networks (OMN), to avoid long offset lines [27]. The final DPA realized 39.5–40 dBm saturation output power and small-signal gain of 8–11 dB from 4.5 GHz to 5.3 GHz. The power added efficiency (PAE) of the DPA at 6-dB back-off power level is 38–41.3%, with corresponding 800 MHz frequency band, and the saturation PAE is 44–54% at the same band.

2. Circuit Design

2.1. Design of Power Cells

The saturated power density of the selected device simulated by load-pull is about 6 W/mm with a drain bias of 28 V at 4.9 GHz. Thus, two of the same $10 \times 100 \mu\text{m}$ devices are chosen to meet the power demand of 39.5 dBm and the high efficiency at 6-dB power back-off level. The main amplifier is biased in class-AB with a gate voltage of -3.2 V and the auxiliary amplifier operates in class-C with a bias voltage of -5.4 V , that means the auxiliary amplifier will not work if the input power is not big enough. Different from other studies [26,28,29], in this design, the drain voltages of main and auxiliary amplifiers are different to ensure the same saturation current for good load modulation; they are 32 V and 28 V respectively, considering more power loss in the main branch.

2.2. Design of Power Divider

The research in [30] uses an equal-split Wilkinson's power divider to split an input signal into two equal phase output signals, which suggests the small-signal gain drops by 3 dB as the auxiliary amplifier closed. In this design, an unequal split Wilkinson's power divider is applied with a ratio of 2.5:1, as shown in Figure 2, and more power is transferred to the main amplifier. Thus, the gain of the DPA consequently increases a lot, while the auxiliary amplifier receives less power so that it does not need to operate at a deep class-C. Figure 3 shows the gain comparison of power dividers with different power ratios; it is obvious that the overall gain is higher with a power ratio of 2.5:1 at the small-signal region and back-off region. This power divider adopts high-pass π -shape $\lambda/4$ transformers composed of lumped inductors and capacitors instead of traditional 90-degree TL which is not suitable for miniaturization, given that its physical length is more than 5 mm at 4.9 GHz. The following formulas and Figure 4 show the way to compute the parameters of unequal split Wilkinson's.

$$Z_a = Z_0 \times \left(\left(\frac{P_m}{P_a} \right)^{-1.5} + \left(\frac{P_m}{P_a} \right)^{-0.5} \right)^{0.5} \quad (1)$$

$$Z_b = Z_0 \times \left(1 + \frac{P_m}{P_a} \right)^{0.5} \left(\frac{P_m}{P_a} \right)^{0.25} \quad (2)$$

$$R_1 = Z_0 \times \left(\left(\frac{P_m}{P_a} \right)^{0.5} + \left(\frac{P_m}{P_a} \right)^{-0.5} \right) \quad (3)$$

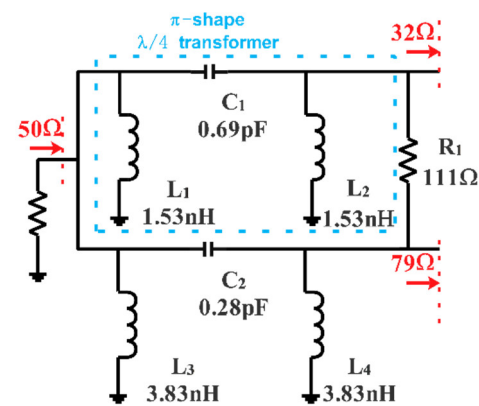


Figure 2. Proposed unequal split Wilkinson's power divider.

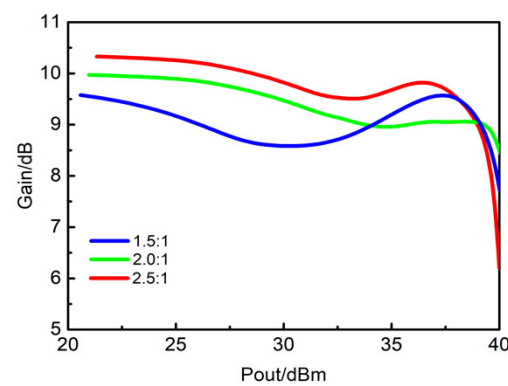


Figure 3. Gain comparison of power dividers with different power ratios.

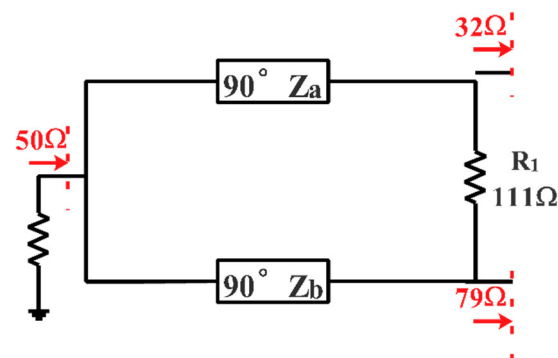


Figure 4. Traditional 90-degree transmission line (TL) power divider.

The Z_a and Z_b represent the characteristic impedances of two corresponding transmission lines, respectively. P_m/P_a in the equations is the power ratio of the main branch to the auxiliary branch and R_1 is the isolation resistance. The value of Z_0 is generally 50 ohms. Then, the next step is to convert obtained TL to compact lumped components. The value of the inductors and capacitors of high-pass π -type $\lambda/4$ transformers can be calculated as shown in Figure 5.

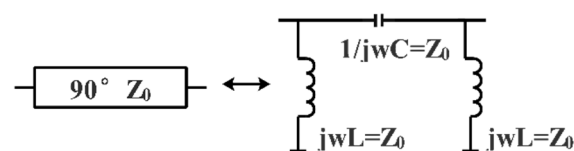


Figure 5. Ninety-degree TL converts to lumped π -type network.

2.3. Design of OMN

Figure 6 shows the whole novel output networks, including four parts as follows: OMNs of main and auxiliary branch, impedance invert network (IIN), compensation inductor of auxiliary amplifier. The OMN of the main amplifier matches the output impedance ($R_{m,opt}$) to $50\ \Omega$ first. Then, the impedance invert network following OMN needs to convert load impedance (R_{load}) of $50\ \Omega$ to $100\ \Omega$ at a low-power region. At this time, the auxiliary amplifier is pinched off and the efficiency of the main amplifier will reach its first peak. The shunt inductor L_9 is inserted to neutralize the output capacitance of auxiliary to realize open circuit in low-power region [29]. The small-signal simulation result of auxiliary's branch with shunt inductor L_9 is shown in Figure 7, and a high output impedance of auxiliary amplifier is ensured at target frequency. As the input power increases, the auxiliary begins to transmit current and load modulation also starts at the same time. An OMN with zero phase variation, which will not influence open circuit condition at low-power region, must be used in the auxiliary branch to convert from $100\ \Omega$ to $R_{a,opt}$ at saturation region [14].

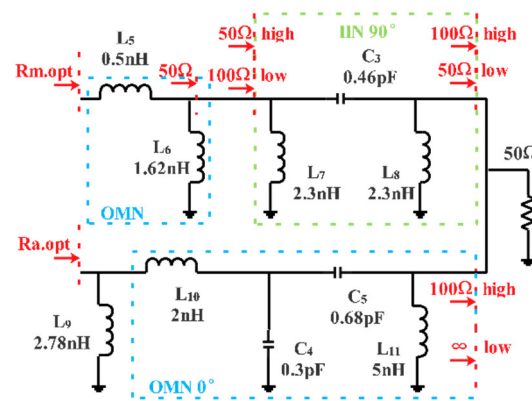


Figure 6. Output matching network.

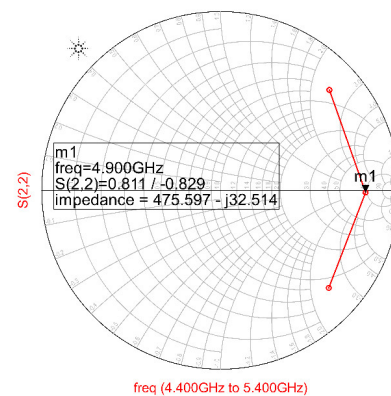


Figure 7. S-Parameters simulation of auxiliary branch.

Meanwhile, $100\ \Omega$ is converted to $50\ \Omega$ for impedance matching in the main branch by IIN at saturation region, and thus, the DPA reached its second peak efficiency. Apparently, the impedance transformer ratio (ITR) of this circuit is 2:1, which has wider bandwidth and less insertion loss than conventional ones, as shown in Figure 8 with ITR of 4:1. Moreover, the drain bias inductors L_6 and L_9 need to be replaced with transmission lines for larger current capacity. Although transmission lines occupy more chip area, they insert less loss and ensure higher efficiency.

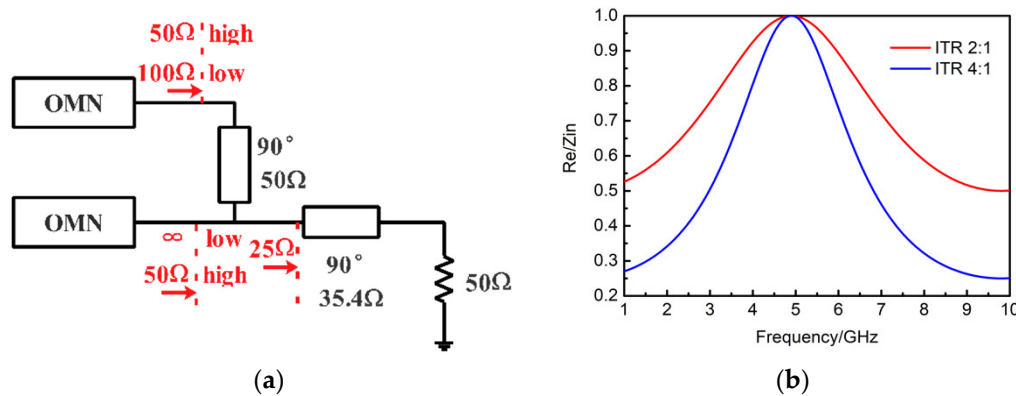


Figure 8. (a) Conventional topology (left); (b) The impact of different impedance transformer ratios (ITRs) on bandwidth (right).

2.4. Design of IMN

In addition to impedance matching, one of the most important function of input matching networks (IMNs) is to compensate phase difference generated by the different bias voltages and OMNs. The specific value of phase difference between main and auxiliary branch except IMNs is simulated as 102 degree. Therefore, the two IMNs of DPA should make up this gap while completing impedance matching and the IMNs of the DPA are shown in Figure 9. The R_2 is the stabilizing circuit of the main amplifier with the value of 5Ω to ensure that the circuit does not oscillate. The input impedance of main amplifier ($R_{m.in}$) is the optimal impedance simulated at 6-dB back-off power level with an equivalent load impedance of 100Ω . It is different from optimal impedance simulated at saturation region with a 50Ω equivalent load impedance and this way indeed improves the gain of the DPA at back-off power region. A band pass network, including four lumped elements, whose phase shift is -21 degree is applied to match the $R_{m.in}$ to 32Ω . The INM of auxiliary employs a high pass LC network for matching which has 81 - degree phase variation. Therefore, the phase difference between two branches is compensated by IMNs instead of long TL.

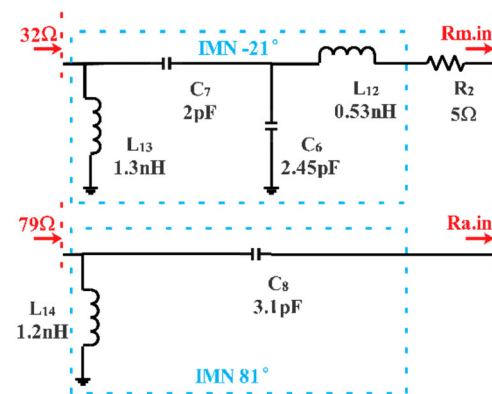


Figure 9. Input matching networks (IMNs) of the proposed DPA.

2.5. The Implementation of DPA

The complete schematic of DPA is shown in Figure 10. The design employs HIWAFER $0.25\mu m$ GaN technology to implement the DPA and the chip area is only $2.37 \times 1.86 mm^2$, which is very competitive in similar research. The main amplifier and auxiliary amplifier use the same $10 \times 100\mu m$ transistors to achieve a high efficiency at 6-dB back off power level. For a compact size, the whole circuit employs lumped inductors and capacitors as much as possible, while avoiding the use of long transmission lines. The shunt inductors are merged into nearby ones to realize a compact chip area. L_1 and L_3 are merged into

L_{1m} at the beginning of the power divider. L_2 and L_{13} , L_4 and L_{14} are merged into L_{3m} , L_{4m} respectively at the junction of power divider and IMNs. L_8 and L_{11} are merged into L_{8m} at the power combining point. The inductor merged by L_6 and L_7 is replaced with a transmission line TL_1 for low loss and TL_2 substitutes inductor L_9 in the same way. The gate bias voltage of main amplifier working in AB-class is set to -3.2 V. The auxiliary amplifier is biased in C-class with -5.4 V to ensure that device is turned on until 6-dB back-off power level. The drain voltage of 32 V and 28 V is added to the main amplifier and auxiliary amplifier respectively to obtain the same saturation current.

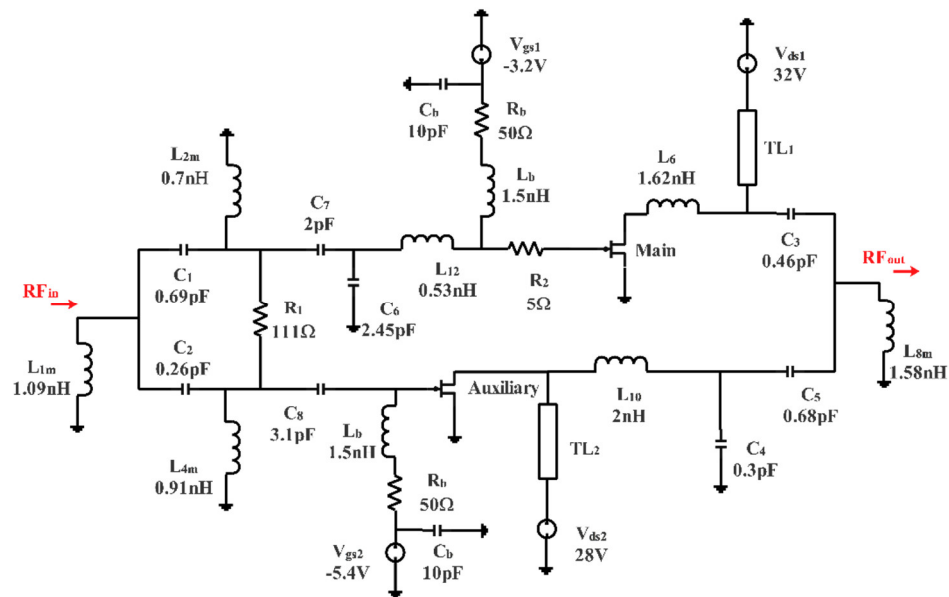


Figure 10. The schematic of the proposed DPA.

3. Simulation Results

The proposed circuit is simulated by the advanced design system of Agilent. The simulation result of S-parameters is shown in Figure 11. The gain of DPA is over 8 dB at a 1400 MHz bandwidth from 4.1 GHz to 5.5 GHz, with a small-signal input and input return loss is lower than -11 dB at the same bandwidth.

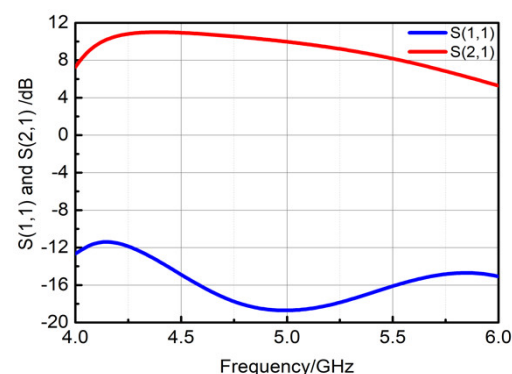


Figure 11. The Simulation of S-parameters.

Figure 12 shows the simulated results of PAE and power gain under a continuous wave (CW) signal from 4.5 GHz to 5.3 GHz. The saturation output power of DPA as shown is 39.5–40.6 dBm across the same band. The simulated PAE at 39.5 dBm power level is 44–54% from 4.5 GHz to 5.3 GHz with the step of 50 MHz, as shown in Figure 13. At the same frequency band, the PAE is 38–41.3% at the output power of 33.5 dBm, which is 6-dB back-off power level. The linearity of the DPA characterized by IMD_3 , using 2 tones

separated by 40 MHz, is simulated at 4.5 GHz, 4.9 GHz and 5.3 GHz respectively, as shown in Figure 14. It can be seen that IMD3 of proposed DPA working at OPBO is lower at the beginning and end of the frequency than center frequency, which proves that linearity can be improved by mismatch. The final layout of DPA is shown in Figure 15, which has a $2.37 \times 1.86 \text{ mm}^2$ chip area. Table 1 shows the comparison of performance between proposed DPA and the DPA mentioned before. This work adopts a novel low ITR output topology to overcome the defect of narrow bandwidth in [15,17]. Moreover, this output topology and IIN for phase compensation can provide less power loss by reducing extra circuit components to achieve a higher efficiency at OPBO than DPA of [26].

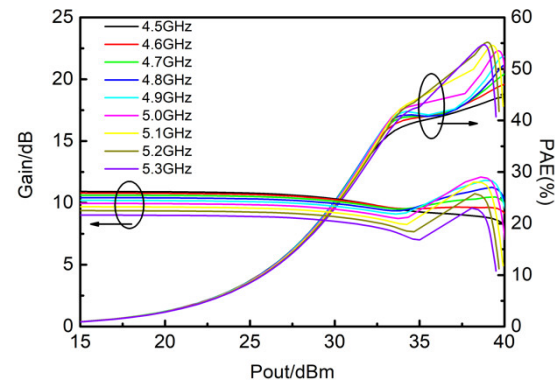


Figure 12. Simulated PAE and power gain of DPA under continuous wave (CW) simulation.

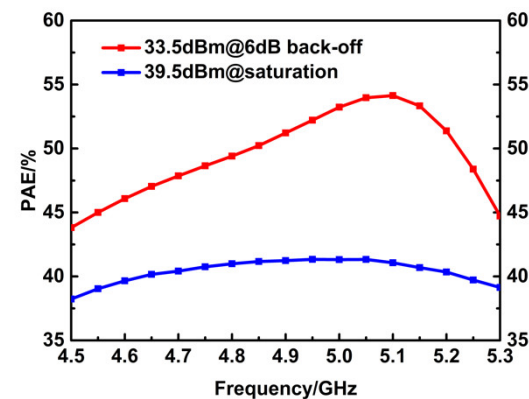


Figure 13. Simulated PAE from 4.5 GHz to 5.3 GHz.

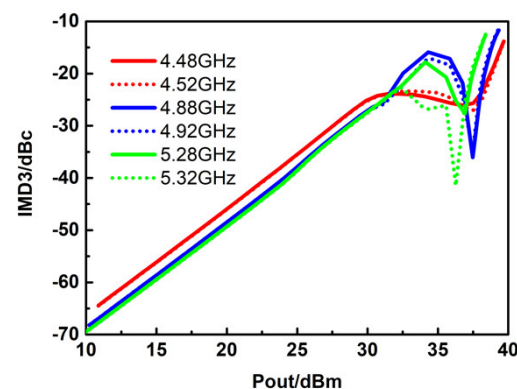


Figure 14. IMD3 of DPA at the center frequency of 4.9 GHz.

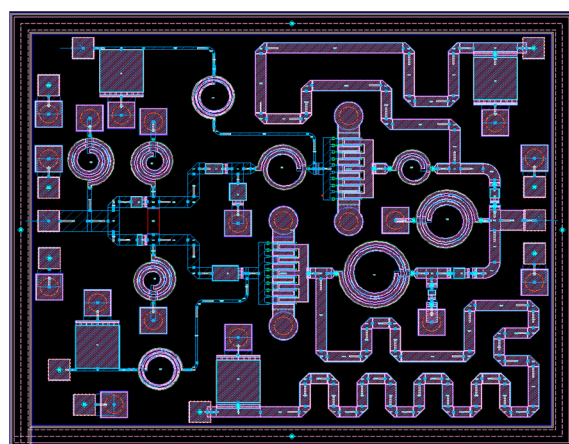


Figure 15. Layout of the DPA.

Table 1. Comparison of performance with other published DPA.

Parameter	Reference [15]	Reference [17]	Reference [26]	This Work
Fre (GHz)	5.9	4.8–5.0	4.5–6.0	4.5–5.3
Gain (dB)	14.4	9	11.6	11
Psat (dBm)	38.7	40.3	36	39.5
PAE (sat)	47.3%	60–63%(DE)	25.7%	44–54%
PAE (back-off)	49.5%@6 dB	51–53%(DE)@6 dB	22.5–27.6%@8 dB	38–41.3%@6 dB
Size (mm ²)	2.49 × 1.56	2.5 × 2.3	3.0 × 2.8	2.37 × 1.86

4. Conclusions

An ultra-compact two-way asymmetrical Doherty power amplifier based on a 0.25 um GaN HEMT MMIC process is presented in the paper. The high gain has been obtained with the asymmetrical Doherty, which has a 2.5:1 power ratio for the main and auxiliary PA. In addition, IMNs with phase compensation function have been introduced to reduce the size of the circuit. For a broadband operation, a novel topology with low ITR has been employed to alleviate the bandwidth limiting factor caused by the quarter-wavelength transformer. With the design concept, the simulated result shows that the proposed circuit achieves a small-signal gain of 11 dB, a 6-dB back-off PAE of 38–41.3%, a saturation PAE of 44–54% at a wide frequency band from 4.5 GHz to 5.3 GHz. Compared with other works, this circuit has a very compact chip size, while maintaining excellent performance.

Author Contributions: Conceptualization, P.C., X.W.; Data curation, P.C.; Formal analysis, P.C., L.J.; Investigation, P.C., Q.W., Y.J. and Z.L.; Methodology, P.C.; Software, P.C., Q.W. and Y.J.; Validation, P.C.; Writing—original draft, P.C.; Writing—review and editing, W.L., Y.J., C.F., H.X. and X.W. All authors have read and agreed to the published version of the manuscript.

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Conflicts of Interest: The authors declare no conflict of interest.

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