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Input-Series-Output-Parallel DC Transformer Impedance Modeling and Phase Reshaping for Rapid Stabilization of MVDC Distribution Systems

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Abstract: This paper focuses on the instability problem of the medium-voltage DC (MVDC) distribution system and proposes an impedance phase reshaping (IPR) method. To obtain the load impedance model of the MVDC distribution system, the input impedance of the input-series-output-parallel (ISOP) DC transformer (DCT) is derived by the generalized average modeling (GAM). Based on the obtained model, the traditional ISOP DCT controller optimization (IDCO) approach is discussed and the IPR method is developed. An impedance phase controller is introduced based on the original control method. According to the optimized impedance stability criterion, the parameters of the impedance phase controller are determined. Compared with the IDCO approach, the proposed method weakens the negative resistance characteristic of the load impedance at the resonant frequency. Therefore, the MV bus voltage oscillation is rapidly mitigated. Besides, the dynamic performance of the system using the IPR method can be classified as good. The simulation results show that the mathematical model is correct, and the proposed method is effective for the rapid stabilization of MVDC distribution systems.

Keywords: MVDC distribution system; input-series-output-parallel (ISOP); DC transformer; generalized average modeling (GAM); impedance phase reshaping (IPR)

1. Introduction

The medium-voltage DC (MVDC) distribution system has become the trend of the future energy internet power distribution due to the beneficial attributes, such as its flexibility and efficiency [1–3]. An MVDC grid was designed for the interconnection of high-power test benches at a university campus [4]. Furthermore, the MVDC power distribution has been widely applied in railway electrification systems and marine electrical distribution systems [5–10].

A typical DC distribution system is shown in Figure 1. The DC transformer (DCT) plays a prominent role in the modern MVDC distribution system. As the key device, it connects the MVDC bus and the low-voltage DC (LVDC) bus. Given the voltage stress of the switching devices, the inputs-series-output-parallel (ISOP) topology of several DC/DC converter modules has been introduced. For the ISOP DCT, the dual-active bridge (DAB) converter is a more suitable submodule than other converters, such as the bidirectional half-bridge converter and the series resonant converter [11,12]. In addition, an input voltage sharing (IVS) control strategy has been presented to ensure the power sharing of the ISOP DCT [13,14]. However, a tightly regulated converter behaves as a constant power load (CPL) [15–18], which exhibits a negative resistance characteristic and may destabilize the system. When a regulated ISOP DCT is connected to a power electronic converter or an inductive circuit as shown in Figure 1, the stability of the MVDC distribution system



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Copyright: © 2021 by the authors. Licensee MDPI, Basel, Switzerland. This article is an open access article distributed under the terms and conditions of the Creative Commons Attribution (CC BY) license (https:// creativecommons.org/licenses/by/ 4.0/). may become corrupted and substantial oscillations would occur. Besides, it has been confirmed that the system behaves in an unstable way with the increase of the source-side inductance [19–21]. Consequently, an impedance-based stability analysis for the ISOP DCT is essential to guarantee the stability of the MVDC distribution system.

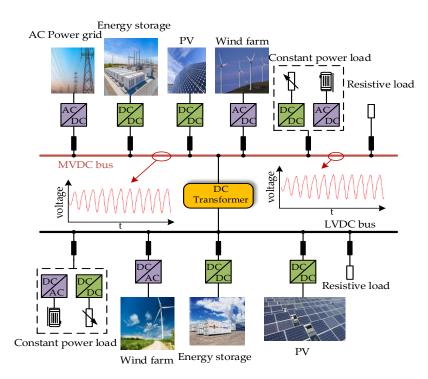


Figure 1. A typical DC distribution system.

The prerequisite for the impedance-based stability analysis is to develop the impedance model of the system, including the source impedance and the load impedance. Based on the model, the stability of the system can be analyzed by the impedance stability criterion.

Several theoretical modeling techniques have been proposed to obtain an impedance model. Taking the first harmonic approximation into consideration, the generalized average modeling (GAM) [22–24] is more accurate than the reduced-order modeling [25] for the DAB converter. Based on the impedance model, Middlebrook et al. discussed the stability criterion for voltage regulated DC/DC converters [26], and Sun et al. studied the stability criterion for grid-connected inverters [27]. The ratio of the source impedance and the load impedance is known as the minor loop gain, and the whole system is stable if it satisfies the Nyquist Criterion [28]. Moreover, various stability criteria have been proposed by defining the constraint boundary of the minor loop gain [29,30]. Riccobono et al. [31] presented a Passivity-Based Stability Criterion (PBSC), which increases the phase of the system total impedance up to 0° at the resonant frequency. Hence, the impedance becomes passive to guarantee the bus stability [32,33].

According to the above-mentioned stability criteria, the system stability can be improved by reshaping the impedance. Feng et al. [34] introduced two control methods to modify the impedance by building a virtual impedance connected in parallel or series with the input impedance of the DAB converter. There was no intersection of the impedance amplitude by increasing the input impedance amplitude. In [35], a resonance term was applied to dampen the bus impedance. However, this approach only relies on the source impedance and ignores the influence of the load impedance. Compared with the impedance amplitude reshaping, the phase modification takes into account that the amplitude must intersect. Zhang et al. [36] proposed a parallel virtual impedance (PVI) and a series virtual impedance (SVI) control strategy to modify the load impedance phase at a small range of frequency. According to the approaches introduced in [36], Feng et al. [37] analyzed the stability improvement of the system via the controller optimization. Meanwhile, an impedance shaping regulator has been proposed to reshape the impedance phase. Although they both enhance the stability of the DAB-based energy storage systems, the impedance shaping regulator has better dynamic responses than the optimized method of the DAB controller. The system with the optimized DAB controller requires minimum cost. Moreover, Guan et al. [38] proposed a three-closed-loop control strategy to reshape the input impedance of the DAB converter. On the basis of the control method introduced in [38], Wang et al. [39] investigated a triple-close-loop IVS control strategy, which improved the dynamic and steady-state performance of the ISOP DCT. However, the strategy has drawbacks with complicated parameter calculation and extra design steps.

This paper proposes an impedance phase reshaping (IPR) method, the load impedance model is obtained by the GAM method, and the impedance phase is modified for the MVDC distribution system rapid stabilization.

This paper presents the following major contributions.

- (1) Establish a GAM input impedance model for the ISOP DCT. The obtained model is accurate and programmable, which provides a theoretical basis for the stability analysis.
- (2) Propose an IPR method to modify the impedance phase, which weakens the negative resistance characteristic of the ISOP DCT. The ISOP DCT controller optimization (IDCO) method is investigated. Compared with the IDCO method, the proposed approach mitigates the MV bus voltage oscillation rapidly and improves the voltage quality of the ISOP DCT.

The paper is organized as follows. Section 2 introduces the configuration of the MVDC Distribution System, and the GAM input impedance model of the ISOP DCT is established as the load impedance. Section 3 describes the IDCO method. Section 4 discusses the proposed IPR method. Section 5 displays the simulation analysis results. Section 6 summarizes the major outcomes of this paper and its possible future extensions.

2. Impedance Modeling of the MVDC Distribution System

2.1. Configuration of the MVDC Distribution System

The MVDC distribution system includes the DC grid, the ISOP DCT, and the load. The structure of the MVDC distribution system is shown in Figure 2.

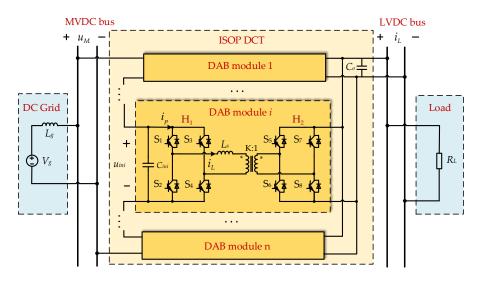


Figure 2. Structure of the MVDC distribution system.

 R_L is the load impedance. u_M and u_L are the MVDC and the LVDC bus voltage, respectively. Meanwhile, u_L is the voltage of the output capacitance C_o . In the DC grid, V_g is the DC grid voltage, L_g is the transmission line inductance. In the ISOP DCT, C_o is the

output capacitance, $n \ (n \in \mathbb{N}+, \mathbb{N}+ \text{ is a set of positive integers})$ is the number of the DAB modules of the ISOP DCT. In the *i*-th $(i = 1, 2 \dots n)$ DAB module, H_1 and H_2 are the rectifier and the inverter full bridges respectively. $S_1 \sim S_8$ are the switches of the bridge arms. i_L is the current of L_s . C_{ini} is the input capacitance. K is the turns ratio of the high-frequency transformer. L_s is the leakage inductance of the high-frequency transformer and resonant inductance. u_{ini} and i_p are the primary side voltage and current, respectively. Moreover, $u_M = \sum_{i=1}^n u_{ini}$.

In addition, the control block diagram of the ISOP DCT is descripted in Figure 3. The input voltage sharing (IVS) control strategy of the ISOP DCT is illustrated in Figure 3. It consists of an output voltage controller G_{u_L} and n - 1 input voltage sharing controllers G_{u_M} . u_M^* and u_L^* are the MV and the LV bus voltage, respectively. The commonly used single phase shift (SPS) method is adopted in this paper. d_L is the basic phase shift ratio of each DAB module and is generated by the output voltage controller G_{u_L} . d_{ini} (i = 1, 2 ... n) is the compensation in phase shift ratio of the *i*-th DAB module, which is generated by the input voltage sharing controller G_{u_M} . d_i (i = 1, 2 ... n) is the phase shift ratio.

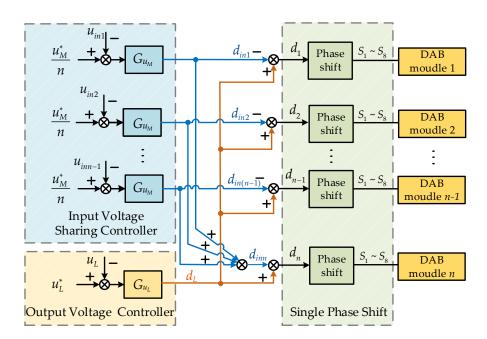


Figure 3. Control block diagram of the ISOP DCT.

As can be seen from Figure 3, the phase shift ratio d_i (i = 1, 2 ... n) is the difference between the two items, which can be expressed as

$$d_i = d_L - d_{ini},\tag{1}$$

Moreover, the decoupling condition of the basic phase shift ratio d_L and the compensation in phase shift ratio d_{ini} ($i = 1, 2 \dots n - 1$) is defined as follows:

$$d_{inn} = -\sum_{i=1}^{n-1} d_{ini},$$
 (2)

where d_{inn} is the compensation in the phase shift ratio of the *n*-th DAB module.

Based on (2), the controllers of the ISOP DCT can be decoupled from each other. The phase shift ratio d_i (i = 1, 2 ... n) is a constant value when power sharing is achieved. Thus, assuming that the phase shift ratio $d_i = d$ (i = 1, 2 ... n), then the load impedance modeling for the MVDC distribution system is as follows.

2.2. Generalized Average Modeling of the ISOP DCT

The load impedance model $Z_L(s)$ of the MVDC distribution system, i.e., the GAM input impedance model of the ISOP DCT is established in this section. The voltage u_L of the output capacitance C_o and the current i_L of the inductance L_s are selected as the state variables. Thus, the state equation of the ISOP DCT can be expressed as

$$\begin{pmatrix}
\frac{di_L}{dt} = \frac{s_1}{nL_s} u_M - \frac{Ks_2}{L_s} u_L, \\
\frac{du_L}{dt} = \frac{Kns_2}{C_o} i_L - \frac{1}{C_o} \frac{u_L}{R_L},
\end{cases}$$
(3)

where s_1 and s_2 are the switching functions of the bridge H_1 and H_2 in the DAB converter, respectively.

Besides, the primary side current i_p and the LV bus voltage u_L are selected as the output variables. The output equation of the ISOP DCT can be given as

$$\begin{cases} i_p = \mathbf{s}_1 i_L, \\ u_L = u_L. \end{cases}$$
(4)

Equations (3) and (4) are based heavily on the model in [22]. More detailed derivation of the state equation, output equation and switching functions s_1 and s_2 may be found therein.

Due to the pure alternating current characteristic of the inductor current i_L , the statevariable vector x is expressed as

$$\mathbf{x} = \left[\begin{array}{cc} < u_L >_0 & < i_L >_{1\mathrm{R}} & < i_L >_{1\mathrm{I}} \end{array} \right]^T, \tag{5}$$

where $\langle u_L \rangle_0$ denotes the zeroth coefficient in the Fourier series of u_L . $\langle i_L \rangle_{1R}$ and $\langle i_L \rangle_{1I}$ denote the real part and imaginary part of the 1st coefficient in the Fourier series of i_L , respectively.

Similarly, the output vector y can be expressed as

3

$$\mathbf{y} = \begin{bmatrix} i_p & u^L \end{bmatrix}^T.$$
(6)

Substitute (5) into (3) and (4) and apply the small perturbation to $d_{,u_{ini}}$ and the state variables at the steady-state operation point. After linearization, the small-signal matrix equation is given as

$$\begin{aligned}
\dot{\hat{x}} &= A\hat{x} + B\hat{u}, \\
\dot{\hat{y}} &= C\hat{x} + D\hat{u},
\end{aligned}$$
(7)

where *A*, *B*, *C* and *D* are the constant matrixs. *u* is the input vector. \hat{x} and \hat{u} represent the small signal value of the state-variable vector *x* and the input vector *u*, respectively. \hat{x} is the derivative of \hat{x} . \hat{y} is the small signal value of the output vector *y*.

$$\hat{\mathbf{x}} = \begin{bmatrix} \langle \hat{u}_L \rangle_0 \\ \langle \hat{i}_L \rangle_{1\mathrm{R}} \\ \langle \hat{i}_L \rangle_{1\mathrm{I}} \end{bmatrix}, \tag{8}$$

$$\hat{\boldsymbol{y}} = \begin{bmatrix} \hat{\boldsymbol{i}}_p \\ \hat{\boldsymbol{u}}_L \end{bmatrix},\tag{9}$$

$$\hat{\boldsymbol{u}} = \begin{bmatrix} \hat{u}_{ini} \\ \hat{d} \end{bmatrix},\tag{10}$$

$$\boldsymbol{A} = \begin{bmatrix} \frac{-1}{RC_o} & \frac{-4Kn\sin(d\pi)}{\pi C_o} & \frac{-4Kn\cos(d\pi)}{\pi C_o} \\ \frac{2K\sin(d\pi)}{\pi L_s} & 0 & \omega_s \\ \frac{2K\cos(d\pi)}{\pi L_s} & -\omega_s & 0 \end{bmatrix},$$
(11)

$$\boldsymbol{B} = \begin{bmatrix} 0 & -\frac{4Kn < i_L >_{1R} \cos(d\pi)}{C_o} + \frac{4Kn < i_L >_{1I} \sin(d\pi)}{C_o} \\ 0 & \frac{2K < u_L >_0 \cos(d\pi)}{L_s} \\ -\frac{2}{\pi L_s} & -\frac{2K < u_L >_0 \sin(d\pi)}{L_s} \end{bmatrix},$$
(12)

$$C = \begin{bmatrix} 0 & 0 & -\frac{4}{\pi} \\ 1 & 0 & 0 \end{bmatrix},$$
 (13)

$$D = \mathbf{0},\tag{14}$$

where $\omega_s = 2\pi f_s$ and f_s is the switching frequency of the ISOP DCT. $\langle \hat{u}_L \rangle_{0, <} \langle \hat{i}_L \rangle_{1R}$, $\langle \hat{i}_L \rangle_{1I}$, \hat{i}_p , \hat{u}_L , \hat{u}_{ini} and \hat{d} are the small signal values of $\langle u_L \rangle_{0, <} \langle i_L \rangle_{1R}$, $\langle i_L \rangle_{1I}$, i_p , u_L , u_{ini} and d respectively.

Thus, combining (7)–(14), the open-loop transfer functions $Y_{op}(s)$, $G_{i_pd}(s)$, $G_{u_Lu_{ini}}(s)$ and $G_{u_Ld}(s)$ can be defined as

$$\begin{bmatrix} \hat{i}_p \\ \hat{u}_L \end{bmatrix} = \begin{bmatrix} Y_{op}(s) & G_{i_pd}(s) \\ G_{u_L u_{ini}}(s) & G_{u_L d}(s) \end{bmatrix} \begin{bmatrix} \hat{u}_{ini} \\ \hat{d} \end{bmatrix}.$$
 (15)

where $Y_{op}(s)$ is the transfer function from \hat{i}_p to \hat{u}_{ini} , $G_{i_pd}(s)$ is the transfer function from \hat{i}_p to \hat{d} , $G_{u_L u_{ini}}(s)$ is the transfer function from \hat{u}_L to \hat{u}_{ini} and $G_{u_L d}(s)$ is the transfer function from \hat{u}_L to \hat{d} respectively.

According to (15) and Figure 3, the small-signal block diagram of the *i*-th (i = 1, 2 ... n - 1) DAB module is shown in Figure 4. \hat{u}_L^* is the small-signal value of the LVDC bus reference voltage. \hat{u}_{ini}^* is the small-signal value of the primary side reference voltage of the *i*-th (i = 1, 2 ... n - 1) DAB module.

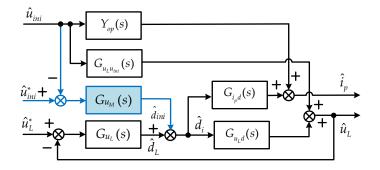


Figure 4. Control block diagram of the *i*-th ($i = 1, 2 \dots n - 1$) DAB module.

As can be seen from Figure 4, \hat{u}_L^* and \hat{u}_{ini}^* are zero. Given the input capacitance C_{ini} of the *i*-th (*i* = 1, 2 ... *n*) DAB converter, the close-loop input admittance $Y_{L_n-1}(s)$ for these n - 1 DAB modules is obtained as follows:

$$Y_{L_n-1}(s) = \sum_{i=1}^{n-1} \left[Y_{op}(s) + Y_{ci}(s) - \frac{G_{u_L u_{ini}}(s)G_{u_L}(s)G_{i_pd}(s)}{1 + G_{u_L}(s)G_{u_Ld}(s)} + \frac{G_{u_M}(s)G_{i_pd}(s)}{1 + G_{u_L}(s)G_{u_Ld}(s)} \right], \quad (16)$$

where Y_{ci} (*s*) is the admittance of the capacitance C_{ini} .

Similarly, the small-signal block diagram of the *n*-th DAB module is shown in Figure 5.

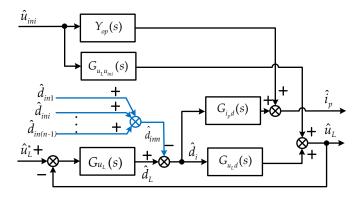


Figure 5. Control block diagram of the *n*-th DAB converter.

From Figure 5, we can see that the compensation in phase shift ratio d_{inn} for the *n*-th DAB converter is different from d_{ini} (i = 1, 2 ... n - 1) for the *i*-th DAB converter as shown in Figure 4, which is caused by the decoupling condition expressed in (2). Based on the control block diagram, the close-loop input admittance $Y_{L_n}(s)$ of the *n*-th DAB module is derived as follows:

$$Y_{L_n}(s) = Y_{op}(s) + Y_{ci}(s) - \frac{G_{u_L u_{ini}}(s)G_{u_L}(s)G_{i_pd}(s)}{1 + G_{u_L}(s)G_{u_Ld}(s)} - \sum_{i=1}^{n-1} \frac{G_{u_M}(s)G_{i_pd}(s)}{1 + G_{u_L}(s)G_{u_Ld}(s)}.$$
 (17)

The input impedance of the ISOP DCT is the sum of the input impedance for these n DAB modules. By adding (16) and (17), the admittance term $\sum_{i=1}^{n-1} \frac{G_{u_M}(s)G_{ipd}(s)}{1+G_{u_L}(s)G_{u_Ld}(s)}$ could be eliminated. The impedance generated by the input voltage sharing control is zero. Hence, the input impedance of the ISOP DCT, i.e., the load impedance $Z_L(s)$ of the MVDC distribution system can be calculated by

$$Z_L(s) = \frac{1}{Y_{L_n-1}(s) + Y_{L_n}(s)} = n/[Y_{op}(s) + Y_{ci}(s) - \frac{G_{u_L u_{ini}}(s)G_{u_L}(s)G_{i_p d}(s)}{1 + G_{u_L}(s)G_{u_L d}(s)}].$$
 (18)

Based on the impedance model obtained in (18), the inter connection of the sub-system for the system is shown as Figure 6. $Z_S(s)$ and $Z_L(s)$ are the source impedance and the load impedance of the MVDC distribution system, i.e., the transmission line inductance and the input impedance of the ISOP DCT, respectively. $G_S(s)$ and $G_L(s)$ are the transfer functions of the source sub-system and the load sub-system, respectively.

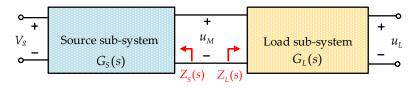


Figure 6. Inter connection of the sub-system for the MVDC distribution system.

The cascade of the two individually stable sub-systems is shown in Figure 6, and the total input-to-output transfer function $G_{gL}(s)$ is.

$$G_{gL}(s) = \frac{u_L}{V_g} = G_S(s)G_L(s) \cdot \frac{Z_L(s)}{Z_S(s) + Z_L(s)} = G_S(s)G_L(s) \cdot \frac{1}{1 + T_m},$$
(19)

where the minor loop gain T_m is defined as

$$T_m = \frac{Z_S(s)}{Z_L(s)},\tag{20}$$

According to (19), since $G_S(s)$ and $G_L(s)$ are stable transfer functions, the minor loop gain T_m is the one responsible for the system stability. Therefore, a necessary and sufficient condition for stability of the MVDC distribution system can be obtained by applying the Nyquist Criterion to T_m , i.e., the stability of the system is guaranteed if and only if the Nyquist contour of T_m does not encircle the (-1, j0) point. Otherwise, the MV bus voltage oscillation would occur. The amplitude intersection f_0 in the Bode diagram of $Z_S(s)$ and $Z_L(s)$ is the oscillation frequency. Besides, the Nyquist criterion is also met by ensuring that the phase difference is less than 180° .

3. Stability Improvement via the IDCO Method

In an unstable MVDC distribution system, the original proportional coefficient and the integral coefficient of the output voltage controller are K_{p0} and K_{i0} , respectively. Similarly, the proportional coefficient and the integral coefficient of the input voltage sharing controller are K_{pi} and K_{ii} , respectively. The parameters of the system are listed in Table 1. The bode diagram of the source impedance $Z_S(s)$ and the load impedance $Z_L(s)$ are shown in Figure 6. α is the phase difference at the intersection frequency f_0 . β_0 is the phase of the load impedance $Z_L(s)$ at f_0 .

As can be seen from Figure 7, $Z_S(s)$ and $Z_L(s)$ intersect at $f_0 = 70$ Hz. $\beta_0 = -91.5^{\circ}$ and the phase difference $\alpha = 181.5^{\circ}$. According to the stability criterion, the MVDC distribution system is unstable and the oscillation frequency of the MV bus voltage is 70 Hz.

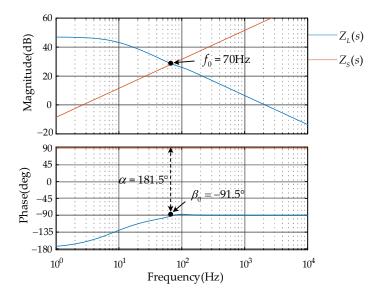


Figure 7. Bode diagram of $Z_S(s)$ and $Z_L(s)$.

	Parameters	Description	Value
DC Grid	L_{φ}	Transmission line inductance	0.06 H
	$L_g V_g$	DC grid voltage	10 kV
ISOP DCT	u_M	MVDC bus voltage	10 kV
	u_L	LVDC bus voltage	750 V
	Κ	Turns ratio of the high-frequency transformer	3
	п	Number of DAB modules	3
	u _{ini}	The primary side voltage of the <i>i</i> -th DAB module	3.33 kV
	L_s	The leakage inductance of the high-frequency transformer and resonant inductance of every DAB module	112.5 μH
	f_s	Switching frequency	20 kHz
	C_{ini}	Input capacitance of the i -th DAB module	225 μF
	C_o	Output capacitance	3 mF
	P_r	Rated power	0.9 MW
Input Voltage	K _{pi}	Proportional coefficient	0.7754
Sharing Controller	K_{ii}	Integral coefficient	136.3038
Output Voltage Controller	K _{p0}	Original proportional coefficient	1.0449
	K_{i0}	Original integral coefficient	1520.6999
	K_p	Optimized proportional coefficient	0.1682
	K_i	Optimized integral coefficient	344.7928
	θ	Impedance phase interval	(0.90)
Impedance Phase Reshaping	k	Gain of impedance phase controller	0.45
Method	f	Cut-off frequency of first-order low-pass filter	450 Hz

Table 1. Parameters of the MVDC distribution system.

According to the analysis in Section 2, the input impedance generated by the input voltage sharing control is zero. Therefore, the input voltage sharing controller optimization can hardly affect the input impedance of the ISOP DCT.

The traditional ISOP DCT controller optimization (IDCO) method is used to optimize the output voltage controller, which ensures that the phase difference at the impedance intersection frequency f_0 is less than 180°. According to Section 2, the open-loop transfer function of the output voltage controller is $G_{u_L}(s)G_{u_Ld}(s)$. Based on the open-loop transfer function, the optimized PI parameters of the output voltage controller can be obtained by limiting the cut-off frequency and the phase margin. The objective function and constraints of the IDCO method are expressed as

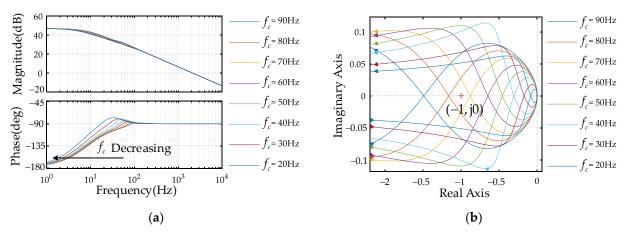
min
$$\left| \arg \frac{Z_S(s, f_c, PM, K_p, K_i)}{Z_L(s, f_c, PM, K_p, K_i)} \right|_{s=j\omega_0}$$
, (21)

$$s.t.\begin{cases} |Z_{S}(s, f_{c}, PM, K_{p}, K_{i})/Z_{L}(s, f_{c}, PM, K_{p}, K_{i})|_{s=j\omega_{0}} = 1, \\ |\arg[Z_{S}(s, f_{c}, PM, K_{p}, K_{i})/Z_{L}(s, f_{c}, PM, K_{p}, K_{i})]|_{s=j\omega_{0}} < 180^{\circ}, \\ |G_{u_{L}}(\omega_{c}, K_{p}, K_{i}) \cdot G_{u_{L}d}(\omega_{c}, K_{p}, K_{i})| = 1, \\ 180^{\circ} + \arg[G_{u_{L}}(\omega_{c}, K_{p}, K_{i}) \cdot G_{u_{L}d}(\omega_{c}, K_{p}, K_{i})] = PM, \\ 30^{\circ} \leq PM \leq 60^{\circ}, \\ \omega_{c} = 2\pi f_{c}, \omega_{0} = 2\pi f_{0}, \end{cases}$$

$$(22)$$

where f_c and *PM* are the cut-off frequency and the phase margin for the transfer function $G_{u_L}(s)G_{u_Ld}(s)$, respectively. K_p and K_i are the optimized proportional coefficient and optimized integral coefficient, respectively. ω_c and ω_0 are the angular frequencies corresponding to f_c and f_0 , respectively.

The reasonable value of *PM* of the control system is $30-60^{\circ}$. With other parameters unchanged, the larger the *PM*, the more stable the system. Thus, *PM* = 60° is selected. To investigate the influence of the output voltage controller on the system stability, eight sets of controller parameters with different cut-off frequency f_c are selected. The Bode diagram



of the load impedance $Z_L(s)$ and the Nyquist diagram of the minor loop gain T_m are shown in Figure 8.

Figure 8. MVDC distribution system stability analysis with different cut-off frequencies: (a) Bode diagram of $Z_L(s)$, (b) Nyquist diagram of T_m .

From Figure 8a, we can see that the phase of $Z_L(s)$ varies obviously with the change of f_c at low frequency. The phase at high frequency is -90° due to the capacitance characteristic. Moreover, the phase at low frequency exhibits negative resistance characteristics and can easily cause oscillation of the MV bus voltage. The phase of $Z_S(s)$ is 90° as shown in Figure 7. Therefore, the impedance phase difference can be less than 180° at 70 Hz by optimizing the output controller in Figure 8a. When the cut-off frequency f_c is 20 Hz or 30 Hz, the stability criterion is satisfied and the MV bus voltage is stable.

As can be seen from Figure 8b, the Nyquist contour of T_m does not encircle (-1, j0) with the decrease of f_c from 90 Hz to 20 Hz. Thus, the stability of the MVDC distribution system is improved with the reduction of the cut-off frequency f_c . However, the bandwidth of the system relies on the cut-off frequency, which will affect the dynamic performance. To improve the dynamic performance and system stability, the cut-off frequency $f_c = 30$ Hz is selected. The optimized output controller parameters K_p and K_i can be obtained based on (22), which are given in Table 1.

4. Proposed IPR Method

Although the traditional IDCO method improves the system stability, it is slow to respond due to the large phase margin *PM* and small cut-off frequency f_c . To stabilize the bus voltage rapidly, an impedance phase reshaping (IPR) method is proposed, and the flowchart is shown in Figure 9.

As shown in Figure 9, the stability criterion is optimized based on $Z_S(s)$ and $Z_L(s)$. Then, an impedance phase controller $G_{ph}(s)$ is introduced to the traditional controller. By adjusting the parameters k and f, the phase θ of load impedance could meet the optimized stability criterion. Therefore, the bus voltage oscillation is rapidly damped and the stability of the MVDC distribution system is guaranteed.

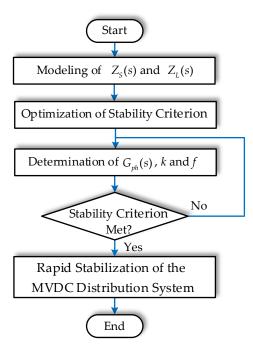


Figure 9. Flowchart of the proposed IPR method.

4.1. Optimization of the Stability Criterion

Since the analysis of Section 2 shows that the input impedance term generated by the input voltage sharing controllers is zero, the input voltage sharing loop transfer function $G_{u_M}(s)$ can be ignored. The small-signal block diagram of the *i*-th (*i* = 1, 2 ... *n*) DAB converter with the impedance phase controller $G_{ph}(s)$ is shown in Figure 10.

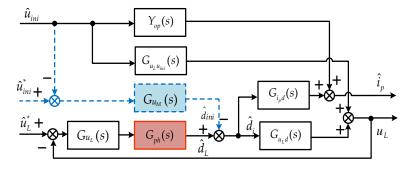


Figure 10. Small-signal block diagram of DAB with $G_{ph}(s)$.

$$Z_{L_{_{_{_{_{_{_{}_{_{}_{}}}}}}}}(s) = n/[Y_{op}(s) + Y_{ci}(s) + \frac{G_{u_{_{_{L}}}u_{ini}}(s)G_{ph}(s)G_{u_{_{_{L}}}}(s)G_{i_{pd}}(s)}{1 + G_{u_{_{_{L}}}}(s)G_{ph}(s)G_{u_{_{_{I}}}}(s)}].$$
(23)

At the intersection of the source impedance amplitude and the load impedance amplitude, the load impedance $Z_{L_{IPR}}(j\omega_0)$ can be expressed as

$$Z_{L_{IPR}}(j\omega_0) = |Z_{L_{IPR}}(j\omega_0)|e^{j\theta}, \qquad (24)$$

where θ is the phase of load impedance at the intersection, ω_0 is the angular frequency of the intersection and $\omega_0 = 2\pi f_0$.

The traditional stability criterion is described as

$$\begin{cases} |Z_S(j\omega_0)| = |Z_L(j\omega_0)|,\\ |\arg[Z_S(j\omega_0)] - \arg[Z_L(j\omega_0)]| < 180^\circ. \end{cases}$$
(25)

In the MVDC distribution system, the phase of $Z_S(j\omega_0)$ is 90°. According to (25), the phase of the load impedance at f_0 should be satisfied $\theta \in (-90^\circ, 270^\circ)$.

To weaken the negative resistance characteristic of the ISOP DCT, the load impedance phase interval is optimized by narrowing $\theta \in (-90^\circ, 0^\circ)$. According to (24), the optimized stability criterion can be obtained as

$$\begin{cases} |Z_{L_{IPR}}(s)/Z_{S}(s)|_{s=j\omega_{0}} = 1, \\ -90^{o} < \theta < 0^{o}. \end{cases}$$
(26)

4.2. Design for the Impedance Phase Controller

As the order of the low-pass filter increases, the phase increases by 90° gradually. In this paper, a first-order low-pass filter is used to reshape the impedance phase at the intersection. The transfer function $G_{ph}(s)$ of the impedance phase controller can be expressed as

$$G_{ph}(s) = \frac{k\omega}{s+\omega},\tag{27}$$

$$\omega = 2\pi f, \tag{28}$$

where ω and f are the cut-off angular frequency and cut-off frequency of the first-order low-pass filter, respectively. k is the gain of the impedance phase controller.

In this section, the determination of k and f is discussed. The constraint condition is to ensure that the intersecting impedance phase θ satisfies the optimized stability criterion in (26), while the amplitude is rarely affected. To analyze the influence of the gain k on the stability of the MV bus voltage, the initial cut-off frequency of the low-pass filter f is 30 Hz. The system stability analysis versus the gain k and cut-off frequency f are shown in Figures 11 and 12.

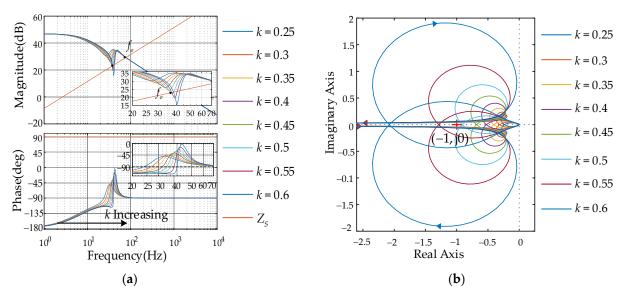


Figure 11. Stability analysis of the MVDC distribution system: (a) Bode diagram of $Z_{L_{IPR}}(j\omega_0)$, (b) Nyquist diagram of T_m .

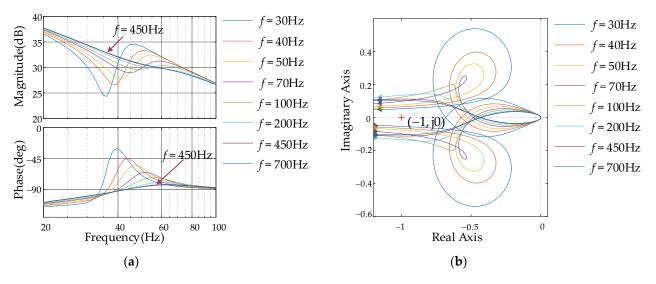
 

Figure 12. Stability analysis of the MVDC distribution system: (a) Bode diagram of $Z_{L_{IPR}}(s)$, (b) Nyquist diagram of T_m .

In summary, the proposed method can solve the instability problem of the MVDC distribution system by weakening the negative resistance characteristic of the load impedance. When the gain k = 0.45 and the cut-off frequency f = 450 Hz, the impedance satisfies the optimized stability criterion, resulting in the MV bus voltage oscillation being rapidly damped. Moreover, the impedance amplitude is rarely affected, and the dynamic performance of the system is good.

4.3. Comparison between the IDCO Method and IPR Method

4.3.1. Negative Resistance Characteristic of the Input Impedance for ISOP DCT

The negative impedance characteristics of the ISOP DCT may destabilize the system. At the impedance intersection f_0 , the weakening of the negative impedance characteristic can suppress the bus voltage oscillation. Therefore, the suppression ability of the bus voltage oscillation based on the two methods can be evaluated by

$$\beta_{IDCO} = \arg[Z_L(j \cdot 2\pi f_o)], \qquad (29)$$

$$\beta_{IPR} = \arg[Z_{L_{IPR}}(j \cdot 2\pi f_o)], \qquad (30)$$

where β_{IDCO} and β_{IPR} are the phases of $Z_L(j \cdot 2\pi f_o)$ and $Z_{L_IPR}(j \cdot 2\pi f_o)$, respectively. $Z_L(j \cdot 2\pi f_o)$ is the load impedance at f_0 based on the IDCO method and $Z_{L_IPR}(j \cdot 2\pi f_o)$ is the load impedance at f_0 based on the IPR method.

Figure 7 shows that the impedance phase of the original system at f_0 is $\beta_0 = -91.5^\circ$. Substituting (18) and (23) into (29) and (30), respectively and combining the parameters in Table 1, $\beta_{IDCO} = -85^\circ$ and $\beta_{IPR} = -83^\circ$ can be obtained at $f_0 = 70Hz$. Both methods weaken the negative impedance characteristics of the ISOP DCT. However, the negative resistance characteristic of the load impedance based on the IPR method ($\beta_{IPR} = -83^\circ$) is weaker than that of the IDCO method ($\beta_{IDCO} = -85^\circ$), indicating that the system can achieve stability faster based on the IPR control.

4.3.2. Dynamic Performance of the MVDC Distribution System

The objective of the IDCO method and the IPR method is to improve the stability of the MVDC distribution system. Both can accomplish the goal by reshaping the load impedance as shown in Figure 8, 11, and 12. To further analyze the dynamic performance of the system, the voltage control closed-loop transfer functions are expressed as

$$G_{IDCO_CL}(s) = \frac{G_{u_L}(s)G_{u_Ld}(s)}{1 + G_{u_L}(s)G_{u_Ld}(s)},$$
(31)

$$G_{IPR_CL}(s) = \frac{G_{u_L}(s)G_{ph}(s)G_{u_Ld}(s)}{1 + G_{u_L}(s)G_{ph}(s)G_{u_Ld}(s)},$$
(32)

where $G_{IDCO_CL}(s)$ is the voltage control closed-loop transfer function based on the IDCO method and $G_{IPR_CL}(s)$ is the voltage control closed-loop transfer function based on the proposed IPR method.

The Bode diagram of $G_{IDCO_OL}(s)$, $G_{IPR_OL}(s)$, $G_{IDCO_CL}(s)$, and $G_{IPR_CL}(s)$ are shown in Figure 13, and the system parameters are listed in Table 1. $G_{IDCO_OL}(s)$ and $G_{IPR_OL}(s)$ are the output voltage control open-loop transfer functions, which are the numerator of (31) and (32), respectively. The comparisons between the IDCO method and the IPR method are summarized in Table 2.

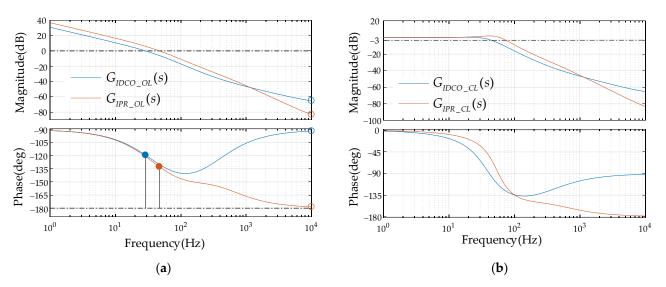


Figure 13. Bode diagram of the transfer functions based on the IDCO method and the proposed IPR method: (**a**) open-loop transfer functions, (**b**) closed-loop transfer functions.

	$G_{IDCO_CL}(s)$	$G_{IPR_CL}(s)$
Bandwidth	44 Hz	74 Hz
Phase Margin (PM)	60°	47°

As can be seen from Table 2, the bandwidth of $G_{IPR_CL}(s)$ is 30 Hz greater than that of $G_{IDCO_OL}(s)$. Thus, compared with the IDCO approach, the dynamic performance of the MVDC distribution system with the proposed method is better. Moreover, the *PMs* of both control methods are in the proper range, and the *PM* of the IDCO method is larger.

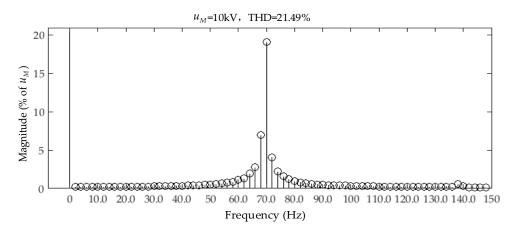
In conclusion, although the system stability is improved in both methods, the negative impedance characteristics of the system are weaker based on the IPR method. Therefore, the proposed IPR method could achieve the rapid stabilization of the MVDC distribution system. In addition, the bandwidth of the IPR method is larger than that of the IDCO method. Thus, the dynamic characteristics of the system are better. However, due to the small *PM*, the IPR method may produce a large overshoot in the dynamic process.

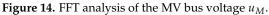
5. Simulation Results and Discussion

Based on the structure as shown in Figure 2, a 10 kV MVDC distribution system was built in MATLAB/Simulink. The ISOP DCT consists of three DAB modules, whose rated power $P_r = 0.9$ MW. The parameters of the simulation model are given in Table 1.

5.1. Verification of the Voltage Instability in the MVDC Distribution System

Fourier transform is a basic method in transform analysis from the time domain to the frequency domain. To verify the unstable problem of the MVDC distribution system, the MV bus voltage u_M was analyzed by the fast Fourier transform (FFT) analysis function in MATLAB. The FFT analysis result of u_M is illustrated in Figure 14. THD is the total harmonic distortion of u_M .





As can be seen from Figure 14, the oscillation frequency is mainly concentrated at 70 Hz and the THD is 21.49%. The results confirm that the original MVDC distribution system is unstable and the oscillation frequency of the MV bus voltage u_M is consistent with Figure 7.

5.2. Verification of the Load Impedance Models

To verify the correctness of the developed impedance models, the bode diagrams of the analytical models are compared with the simulation results. The measurement method of the impedance simulation results is depicted in Figure 15. Moreover, the analytical modeling results and the simulation results of the load impedance are shown in Figure 16.

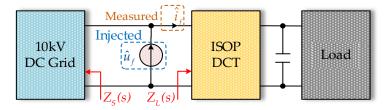


Figure 15. Impedance measurement by the disturbance injection method.

As shown in Figure 15, the sinusoidal perturbations \hat{u}_f are superimposed on the MV bus. The frequency varies from 2 Hz to 10 kHz, and the peak amplitude of \hat{u}_f is 500 V. Meanwhile, the disturbance current \hat{i}_f is extracted by FFT analysis. The measured load impedance of the simulation system is expressed as

$$Z_L(s) = \frac{\hat{u}_f}{\hat{i}_f}.$$
(33)

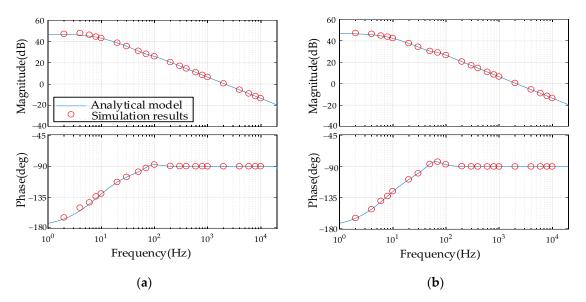


Figure 16. Bode diagram of the load impedance: (**a**) input impedance $Z_L(s)$ based on the IDCO method, (**b**) input impedance $Z_{L,IPR}(s)$ based on the proposed IPR method.

5.3. Verification of the IPR Method

The simulation model is tested under different working conditions to validate the proposed method. When t = 0.2, the system is switched from the original control to the IDCO control or the IPR control. When t = 0.5, the system changes from half load (p = 0.45 MW) to full load (p = 0.9 MW), i.e., the load steps from 1.25Ω to 0.625Ω . Besides, the reference value u_L^* of the LV bus voltage steps from 100% ($u_L^* = 750$ V) to 80% ($u_L^* = 600$ V) at t = 0.7 s. The damping ability to bus voltage oscillation of these two methods is illustrated in Figures 17–19. The dynamic performance of the MVDC distribution system is shown in Figures 20–22.

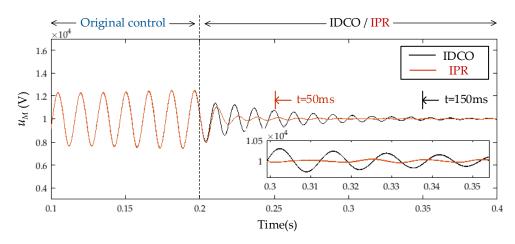


Figure 17. Damping results of the MV bus voltage u_M .

From Figure 17, we can see that for the IDCO and the IPR method, the oscillation of the MV bus voltage u_M is suppressed within 150 ms and 50 ms, respectively. This confirms that the IPR method rapidly suppresses the MV bus voltage oscillation. Moreover, the ripple of u_M using the proposed IPR method is smaller than that of the IDCO approach, because the negative resistance characteristic of the ISOP DCT is weakened.

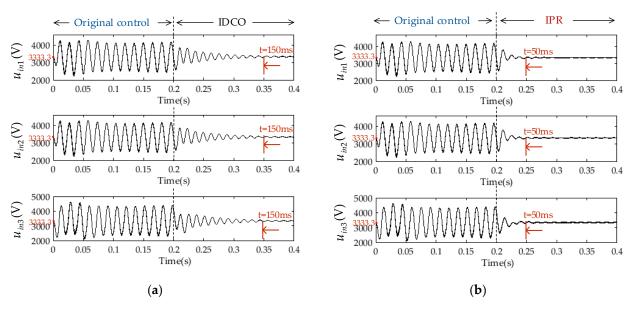


Figure 18. Input voltage of three DAB modules: (a) IDCO method, (b) proposed IPR method.

In the observation from Figure 18a,b, the DAB modules voltage u_{in1} , u_{in2} , and u_{in3} are stable at 3333.3 V. The simulation results demonstrate that the ISOP DCT achieves input voltage sharing. It indicates that the input voltage sharing controller optimization could be ignored, which is consistent with Figure 10. In addition, the transient period of the proposed IPR method is 100 ms shorter than that of the IDCO method. These results indicate that the proposed method can stabilize the voltage faster.

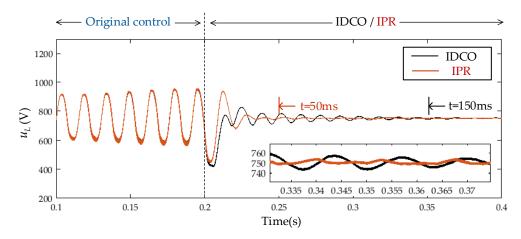


Figure 19. Damping results of the LV bus voltage u_L .

As shown in Figure 19, when the IPR controller is activated, the stabilization time of the LV bus voltage u_L is reduced from 150 ms to 50 ms. This validates that the proposed method is effective. The voltage ripple rate of u_L with the proposed method (about 2%) is lower than that of the IDCO approach (about 2.7%). This illustrates that compared with the IDCO method, the waveform quality based on the IPR method is significantly better. This also indicates that the impedance phase satisfies the phase interval, which further weakens the negative resistance characteristic of the load impedance.

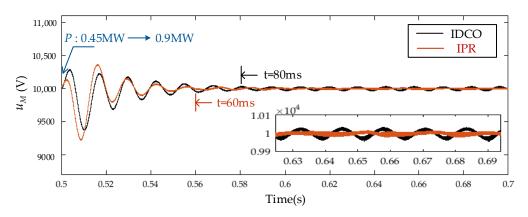


Figure 20. Dynamic waveforms of the MV bus voltage u_M based on the IDCO or IPR control method under a load step-change.

As can be seen from Figure 20, the transient recovery time of the proposed IPR method is 60 ms, which is faster than that of the IDCO approach (about 80 ms). Although the ripple rates are both less than 1%, the result shows that the voltage is more stable with the proposed IPR method than the IDCO method. This validates the effectiveness of the proposed method at the full-load condition. Furthermore, the dynamic performance is good due to the proper bandwidth and phase margin as shown in Table 2.

The waveforms of the LV bus voltage u_L also confirm the good dynamic performance of the IPR method as shown in Figures 21 and 22. It is evident that u_L tracks the step reference well as shown in Figure 21, and the corresponding transient voltage has a short settling time (40 ms). As can be seen from Figure 22, the overshoot of u_L with the proposed IPR control approach is 25 V and the overshoot rate is 4%. It can be seen from Figures 21 and 22 that compared with the IDCO method, the overshoot based on the IPR control is larger, but is still within a reasonable range. These results validate the robustness and effectiveness of the proposed control.

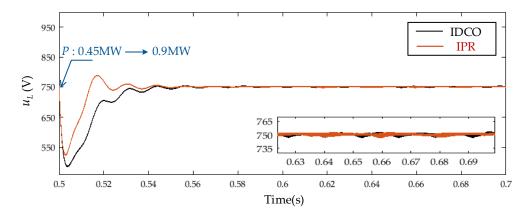


Figure 21. Dynamic waveforms of the LV bus voltage u_L based on the IDCO or IPR control method under a load step-change.

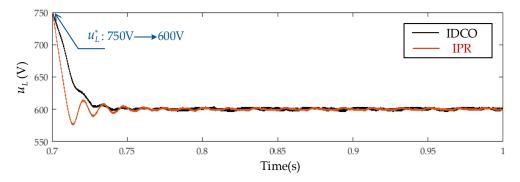


Figure 22. Dynamic waveforms of the LV bus voltage u_L based on the IDCO or IPR control method under a reference value step-change.

6. Conclusions

This paper proposes an IPR method to rapidly stabilize the MVDC distribution system. Based on the obtained load impedance model, the 10 kV MVDC distribution system using the traditional IDCO method and the proposed IPR method was analyzed and simulated. The following relevant conclusions were obtained:

- (i) Due to the decoupling condition of the control strategy for the ISOP DCT, the load impedance is hardly affected by the input voltage sharing controller optimization.
- (ii) Compared with the IDCO method, the proposed method further weakens the negative resistance characteristic of the ISOP DCT and suppresses the voltage oscillation rapidly. Moreover, regardless of load step-change or voltage reference step-change, the proposed method has a good dynamic performance and stability for the system. The overshoot of the proposed IPR method is larger than that of the traditional IDCO method, but it is still reasonable. This is a tradeoff for the rapid stabilization of the MVDC distribution systems.
- (iii) Compared with the method of modifying the impedance amplitude, the proposed IPR method considers the problem that the amplitude must intersect. The phase interval of the optimized stability criterion is adjustable. Furthermore, the impedance phase controller can be designed by the high order low-pass filter and bandpass filter, which are flexible and can be applied to the stability analysis for other systems.

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