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An Efficient Carrier Synchronization Scheme for Demodulation Systems

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Abstract: A simple data-aided carrier synchronization scheme is proposed for variable modulation (VM) communication systems under the initial conditions of a low signal-to-noise ratio (SNR) and normalized carrier frequency offset (CFO) symbol rate of 20%. The proposed carrier synchronization scheme is simplified into two steps; a reconfigurable L&R (RLR) algorithm and pilot-aided (PA) phase linear interpolation algorithm is applied for carrier frequency recovery (CFR) and carrier phase recovery (CPR), respectively. Furthermore, the autocorrelation values of multi-pilot blocks are superimposed to improve the accuracy of the CFR algorithm, and the algorithm formulas are decomposed and modularized to simplify the implementation complexity of the RLR algorithm. Simulation results show that the RLR algorithm can track and lock the CFO up to a 33.2% symbol rate and reduce the CFO to 0.024%. The bit error rate (BER) performance of the carrier synchronization scheme almost coincides with the theoretical curve results. Comparison of hardware complexity shows that the multiplication resource consumption can be reduced by at least 72.47%.

Keywords: variable modulation systems; carrier synchronization; RLR; pilot-aided phase linear interpolation algorithm

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1. Introduction

The proliferation of bandwidth caused by the factors of low-order modulation, spatial channel spectrum resource constraint, and increasing transmission inefficiency are becoming increasingly prominent. To meet the demand of payload data transmission, we can fix the situation in three ways: channel band utilization, power consumption utilization, and signal power utilization. The data transmission efficiency is usually improved by increasing the channel band utilization. The existing satellite–ground link data transmission system is often based on the modulation method applicable to the lowest inter-satellite link gain for data transmission, which will lead to the waste of satellite–ground channel resources and satellite resources. To make full use of the satellite link resources and improve the data transmission efficiency, a variable modulation (VM) system is proposed. The VM system can switch various Modulation modes according to the gain of inter-satellite links.

The receiver of a VM communication system usually adopts a low-cost oscillator, which introduces large initial carrier frequency offset (CFO) to the process of digital transmission for various reasons, such as system oscillation frequency error and Doppler shift, while the receiver of a VM communication system usually needs to achieve high phase estimation accuracy with a low signal-to-noise ratio (SNR). Carrier synchronization is often used for carrier frequency offset recovery (CFR) and carrier phase recovery (CPR). A CFR algorithm consists of a data-aided CFR algorithm and a non-data-aided CFR algorithm, and a CPR algorithm consists of a data-aided CPR algorithm and a non-data-aided CPR algorithm. The commonly used data-aided CFR algorithms are Kay, C&S, M&M, Jiang, Fitz, and L&R algorithms, and the widely used data-aided CPR algorithms are pilot-aided (PA) phase linear interpolation algorithms.

The existing CFR scheme requires at least two steps, including initial frequency recovery, the coarse CFR algorithm, and the fine CFR algorithm. The CPR scheme requires at least one step, including coarse CPR and fine CPR. The four-step carrier synchronization scheme is proposed in [1], including the M&M algorithm for initial CFR, the improved L&R algorithm for coarse CFR, the pilot block interpolation for fine CFR, and the phase difference of the pilot symbols for CPR. A three-step carrier synchronization scheme is proposed in [2], which uses a Delay & Multiply (D&M) algorithm for coarse CFR, then an L&R algorithm for fine CFR, and the PA phase linear interpolator for CPR. The three-step carrier synchronization scheme is proposed, utilizing the Fitz algorithm for coarse CFR, the simple pilot block correlation algorithm for fine CFR, and the PA phase linear interpolator for CPR in [3,4]. The three-step carrier synchronization scheme that adopts the M&M algorithm for coarse CFR, the simple pilot block correlation algorithm [5] for fine CFR, and the pilot-aided block for CPR is proposed in [6]. The study of the features of the application of the coarse frequency synchronization algorithm in [7] reduces the synchronization time, but it does not reduce the complexity of the scheme. A three-step scheme is given in [8]; its purpose is not to simplify the scheme, but to optimize performance. Among them, the alternative carrier synchronization scheme proposed in [3] is less complex compared with [1,2,6], but the scheme is still more complicated.

In this paper, a simplified data-aided carrier synchronization scheme for the VM system is proposed, where the CFO estimation algorithm utilizes the RLR algorithm, and the CPR utilizes the PA phase linear interpolation algorithm. In comparison with the Kay [9], C&S [10], M&M [11], Jiang [12], Fitz [13], and L&R algorithms [14–16], the RLR algorithm is reconfigurable with higher accuracy. The residual frequency offset and residual phase offset can be reduced to the correctable range of the CPR algorithm. The proposed carrier synchronization scheme is simulated under the condition that the symbol rate is 25 Mbaud and the CFO is 20% symbol rate, and its performance almost coincides with the theoretical curve results. In addition, its operating frequency can be up to 200 MHz, with less resource consumption and less complexity of implementation.

2. Conventional Carrier Synchronization Algorithm

2.1. Conventional Carrier Synchronization Scheme

As shown in Figure 1, the physical layer (PL) frame of the VM system consists of three parts: the frame header, the data block, and the pilot block. The physical layer header (PLHEADER) consists of 26 symbols of start of frame (SOF) code and 64 symbols of physical layer signaling (PLS) code (PLSCODE). The data block consists of 16 slots, each with 90 symbols. The pilot block consists of 36 pilot symbols, and each unmodulated pilot symbol can be defined as $I = \frac{1}{\sqrt{2}}$ and $Q = \frac{1}{\sqrt{2}}$. The conventional carrier synchronization scheme is illustrated in Figure 2, which consists of three parts: coarse CFR, fine CFR, and CPR, and the scheme is more complicated [13].

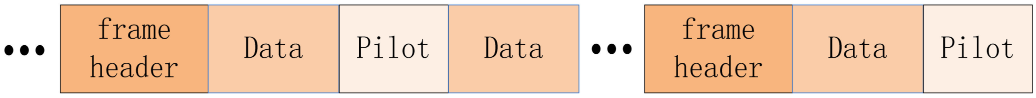

Figure 1. Frame structure.

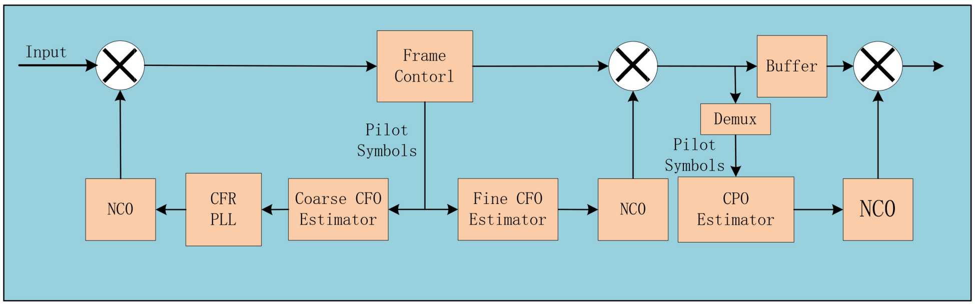

Figure 2. Conventional carrier synchronization scheme.

2.2. *Proposed Carrier Synchronization Scheme*

The frame header position needs to be detected before the carrier synchronization algorithm. Therefore, frame header detection is the key to the whole carrier synchronization scheme. As shown in Figure 3, the proposed carrier synchronization scheme is simplified from three steps to two steps. Differential detection of the SOF and PLSCODE algorithm is adopted to detect the frame header and calculate the location of the pilot block, the distance between pilot blocks, and the index according to the position of the frame header. The RLR algorithm is used to calculate the CFO, the loop filter, and the numerically controlled oscillator (NCO), which are used for CFO compensation. The RLR algorithm locked at a 33.2% CFO with high accuracy. A PA phase linear interpolation algorithm is applied to CPR.

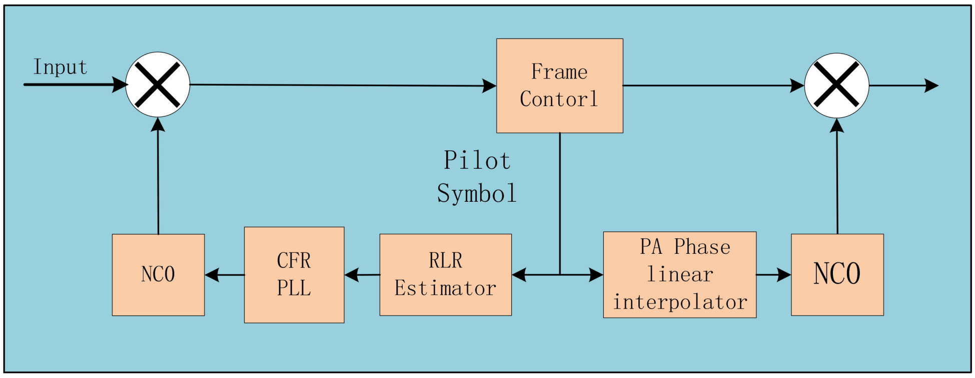

Figure 3. Proposed carrier synchronization scheme.

3. Proposed Carrier Synchronization Algorithm

3.1. *Frame Header Detection Algorithm*

The commonly used frame header detection algorithm is the differential detection of the SOF and PLSCODE [17]. The algorithm first performs differential operations on the input signal, then correlates on both the SOF and PLSCODE differentially using 89 registers and 57 taps. Finally, the outputs of the two parts are, respectively, added and subtracted to produce two values, the maximum of which is the final output of this correlation circuit. When the SOF is detected, we get:

$$\begin{aligned} S_1(k) &= \sum_{k=1}^{25} \left(a_k {a^*}_{k+1} e^{-j2\pi\Delta f} + {n_k}' \right) \cdot T_{1,k} \\ &= 25e^{-j2\pi\Delta f} + {n_k}'' \end{aligned} \tag{1}$$

where $k = 1, 2, \cdots, 25$, ${n_k}''$ represents the noise, a_k is the symbol sent, r_k is the symbol received, $T_{1,k}$ is the SOF register tap, and Δf is the CFO. ${a^*}_i$ is the conjugate of a_i.

When the PLSCODE is detected, we get:

$$\begin{aligned} S_2(k) &= \sum_{k=1}^{32}\left(a_{2k-1}{a^*}_{2k}e^{-j2\pi\Delta f}\cdot e^{-j\pi b_7}+{n_k}'\right)\cdot T_{2,k} \\ &= 32e^{-j2\pi\Delta f-j\pi b_7}+{n_k}''' \end{aligned} \tag{2}$$

where $k = 1, 2, \cdots, 32$, ${n_k}'''$ denotes the noise, $T_{2,k}$ is the PLSCODE register tap, and b_7 is 0 or 1.

When the frame header is detected, the correlation detector output of the SOF and PLSCODE can be expressed as:

$$\begin{aligned} Z(k) &= \max\{|S_1(k)+S_2(k)|, |S_1(k)-S_2(k)|\} \\ &= \left|57e^{-j2\pi\Delta f}+{n_k}''''\right| \end{aligned} \tag{3}$$

where ${n_k}''''$ is the noise. The correlation value is insensitive to the CFO Δf and phase offset θ_0. When the maximum correlation value is about 57, it indicates that the frame header is detected.

3.2. Carrier Frequency Recovery Algorithm

The data-aided CFO estimation algorithm is implemented based on pilot autocorrelation in the VM system. The commonly used data-aided CFO estimation algorithms are Kay, C&S, M&M, Jiang, Fitz, and L&R. Figure 4 shows the CFO estimation range of different algorithms using 36 pilot symbols. In [3], when the CFO estimation algorithm needs to satisfy the two conditions that the CFO can be tracked and locked to 20% of the symbol rate and the algorithm has high accuracy, only D&M, L&R, Fitz, M&M, and improved M&M algorithms can meet this need, but the complexity of D&M, M&M, and Fitz algorithms is higher compared with the L&R algorithm. Therefore, the L&R algorithm is more suitable for CFR. When $N = 2$, the L&R algorithm can track the locked CFO up to 33.2% of the symbol rate.

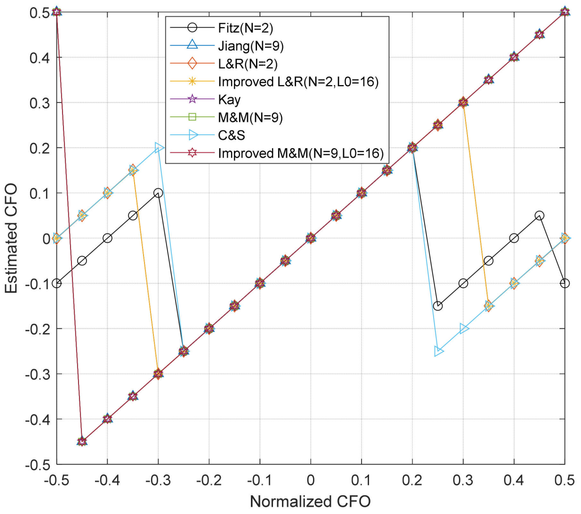

Figure 4. Estimation range of different CFO estimation algorithms.

$z(k)$ is the de-modulated pilot signal, and the autocorrelation function $R(m)$ is expressed as:

$$R(m) = \frac{1}{L-m}\sum_{k=m}^{L-1} z(k)z^*(k-m), 1 \le m \le L-1 \tag{4}$$

where L represents the number of pilot symbols, $L = 36$.

The expression of the L&R algorithm [7] is:

$$\Delta\hat{f} = \frac{1}{\pi(N+1)T_s}\arg\left[\sum_{m=1}^{N} R(m)\right], 1 \leq m \leq N \tag{5}$$

To simplify the complexity of the L&R algorithm implementation and to modularize each function, the RLR algorithm is proposed in this paper, in which the conjugate of $z(i)$ is redefined as:

$$z^{**}(i) = \begin{cases} z^{*}(i), & 1 \leq i \leq L \\ 0, & \text{others} \end{cases} \tag{6}$$

$z^{*}(i)$ is the conjugate of $z(i)$. Then, $\sum\limits_{m=1}^{N} R(m)$ can be expressed as:

$$\begin{aligned} \sum_{m=1}^{N} R(m) &= \sum_{m=1}^{N}\sum_{k=m}^{L-1} \tfrac{1}{L-m} z(k)z^{*}(k-m) \\ &= \sum_{m=1}^{N}\sum_{i=1}^{L-1} \tfrac{1}{L-m} z(i)z^{**}(i-m) \\ &= \sum_{i=1}^{L-1}\sum_{m=1}^{N} \tfrac{1}{L-m} z(i)z^{**}(i-m) \end{aligned} \tag{7}$$

where $1 \leq i \leq L-1$ and $0 < m \leq N$. The i-th sub-autocorrelation function $r_i(m)$, with $m - interval$, can be written as:

$$r_i(m) = \frac{1}{L-m} z(i) * z^{**}(i-m) \tag{8}$$

The sum $R_i(m)$ of different intervals' autocorrelation values of the i-th demodulated signal in the pilot block can be written as:

$$R_i(m) = \sum_{m=1}^{N} r_i(m), 0 < N \leq L \tag{9}$$

Then:

$$\sum_{m=1}^{N} R(m) = \sum_{i=1}^{L-1} R_i(m) = \sum_{i=1}^{L-1}\sum_{m=1}^{N} r_i(m) \tag{10}$$

Figure 5 shows the block diagram of function $r_i(m)$. The $valid_m$ signal can be used to indicate whether the $m - interval$ sub-autocorrelation function module is in the operation. According to different conditions, the $valid_m$ signal can be flexibly controlled in this algorithm to implement the RLR architecture under different parameters, N, in which $r_i{}'(m)$ can be defined as:

$$r_i{}'(m) = \begin{cases} r_i(m), & valid = 1 \\ 0, & valid = 0 \end{cases} \tag{11}$$

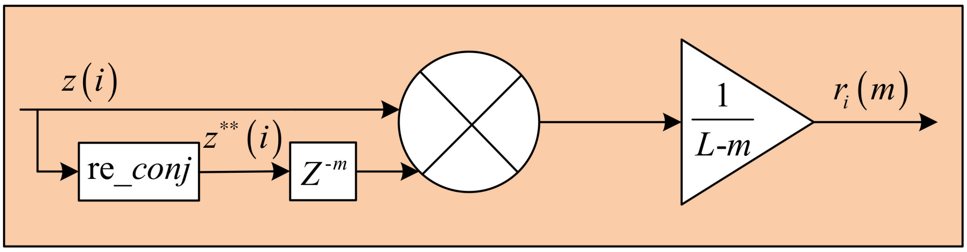

Figure 5. Sub-autocorrelation function module.

The estimation accuracy of the algorithm can be improved by superimposing consecutive L_0 pilot blocks. The frequency estimate value $\Delta\hat{f}_{L0}$ of the RLR algorithm is:

$$\Delta\hat{f}_{L0} = \frac{1}{\pi(N+1)T_s}\arg\left[\sum_{l=0}^{L_0-1}\sum_{m=1}^{N} R_l(m)\right], 1 \le m \le N \tag{12}$$

where $R_l(m)$ is the autocorrelation function of the l-th pilot block. Then:

$$\sum_{l=0}^{L_0-1}\sum_{m=1}^{N} R_l(m) = \sum_{l=0}^{L_0-1}\sum_{i=1}^{L-1} R_{l_i}(m) = \sum_{l=0}^{L_0-1}\sum_{i=1}^{L-1}\sum_{m=1}^{N} r_{l_i}(m) \tag{13}$$

As shown in Figure 6, the structure of the CFO estimation algorithm is mainly composed of Unit1, Unit2, Unit3, Unit4, and Unit5. Unit1 realizes the autocorrelation function at different intervals; Unit2 accumulates the autocorrelation values of different intervals; Unit3 calculates the cumulative sum of the autocorrelation values of the pilot block with different intervals; Unit4 realizes the cumulative autocorrelation values of multiple pilot blocks; and Unit5 estimates the CFO. Assuming that the number of cumulative autocorrelations of multiple pilot blocks is L_0, then the accumulator loop is set from 0 to $L_0 - 1$, and the *pilot_en* signal is the enable signal of the accumulator. When the accumulator number is equal to $L_0 - 1$, the cumulative autocorrelation result *R_Sum* of multiple pilot blocks is an arctangent calculation to obtain the frequency estimate value $\Delta\hat{f}_{L0}$, and the enable signal is generated to clear the accumulation value $\sum\limits_{l=0}^{L_0-1}\sum\limits_{i=1}^{L-1} R_{l_i}(m)$ to zero. It can be seen from Unit4 that the increased resource consumption is limited. The RLR algorithm calculates the CFO and recovers the CFO through the feedback loop.

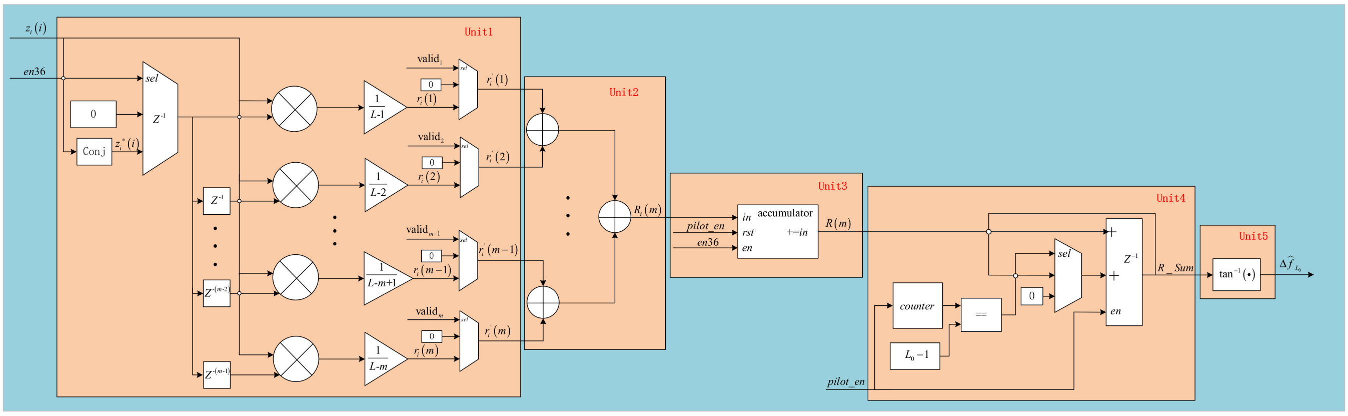

Figure 6. Block diagram of carrier frequency offset estimation regarding RLR algorithm.

3.3. *Carrier Phase Recovery Algorithm*

After the CFO compensation, residual frequency offset and residual phase offset still exist in the signal, so residual phase estimation and phase compensation are also needed. In this paper, the PA phase linear interpolator algorithm is used for phase estimation and compensation, and the phase error detector uses the pilot block to estimate the phase error. The expression is:

$$\theta_k = \arg\left[\sum_{n=1}^{36} x(n)\cdot p^*(n)\right] \tag{14}$$

where $x(n)$ is the input sequence of the CPR, $p(n)$ is the known pilot sequence, and $p^*(\mathrm{n})$ is the conjugate of $p(\mathrm{n})$. The PA phase linear interpolator algorithm implements linear interpolation between the preamble pilot block and the current pilot block, which is shown in Figure 7. The phase linear interpolation expression is:

$$\theta_{\mathrm{k}_\mathrm{i}} = \theta_{\mathrm{k}-1} + \frac{(\theta_\mathrm{k} - \theta_{\mathrm{k}-1}) \times i}{L_k} \tag{15}$$

where $\theta_{\mathrm{k}_\mathrm{i}}$ represents the estimated phase of the i-th data symbol between the $(k-1)$-th pilot block and the k-th pilot block, θ_k is the phase offset evaluation value of the k-th pilot block, and L_k denotes the number of symbols between the $(k-1)$-th block and the k-th pilot block. The estimated range of the phase error detector should be between $[-\pi, \pi]$.

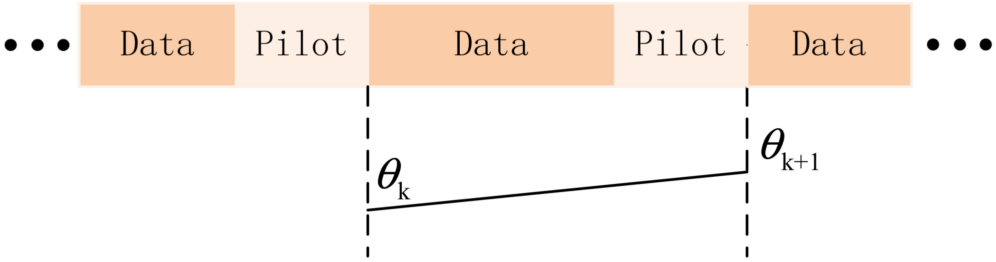

Figure 7. Pilot-aided (PA) phase linear interpolator.

As shown in Figure 8, the implementation structure of the CPR algorithm is composed of Unit6 and Unit7. The de-modulated pilot block is selected to accumulate. Moreover, the current pilot block phase θ_k is calculated in Unit6. The phase difference value $\Delta\theta_\mathrm{k}$ between the current pilot block phase θ_k and the preamble block $\theta_{\mathrm{k}-1}$ is calculated. Moreover, the phase difference $\Delta\theta_\mathrm{k}$ is limited between $[-\pi, \pi)$ in Unit7. The index value *index* and the distance *len* between the preamble block and the current pilot block are used to calculate a linear interpolation $\theta_{\mathrm{k}_\mathrm{i}}$, which is limited to between $[-\pi, \pi)$, and the linear interpolation is input to the DDS for feedforward compensation.

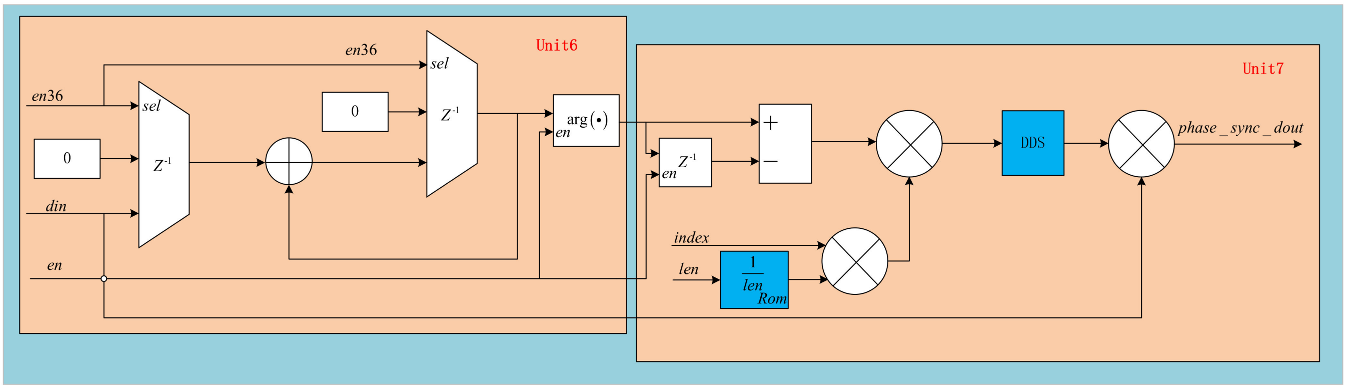

Figure 8. Block diagram of CPR implementation.

4. Carrier Synchronization Scheme Simulation and Hardware Implementation

4.1. Carrier Synchronization Scheme Simulation and Performance Analysis

Under the conditions of pilot-aided environment of symbol rate of 25 Mbaud, initial CFO of 5 MHz, initial phase offset of 2°, and a code length of 8160, the proposed carrier synchronization scheme is simulated with QPSK, 8PSK, 16APSK, and 32APSK BER curves. The multiplication resource consumption of the RLR algorithm is proportional to the parameter N, which is 2 × N. The larger the value of N, the more the multiplication resource is consumed, the smaller the capture range, and the higher the algorithm accuracy. Therefore, combining various factors, the valid signal can be controlled to make the RLR architecture work in the N = 2 architecture. When the carrier frequency offset is reduced to a smaller range, the valid signal can be controlled to make the RLR architecture work in the N = 15 architecture so that the carrier frequency offset accuracy can reach the carrier phase offset.

The number of superimposed pilot segments will affect the precision of the RLR algorithm. The larger the superimposed blocks, the higher the accuracy. In Figure 9, the root mean square error (RMSE) changes little when the number of superimposed blocks is less than 64. In the four modulations, the RMSE is almost the smallest when the number of superimposed blocks is L = 16 or L = 32. In this paper, the RLR algorithm with 16 superimposed blocks is selected for CFR.

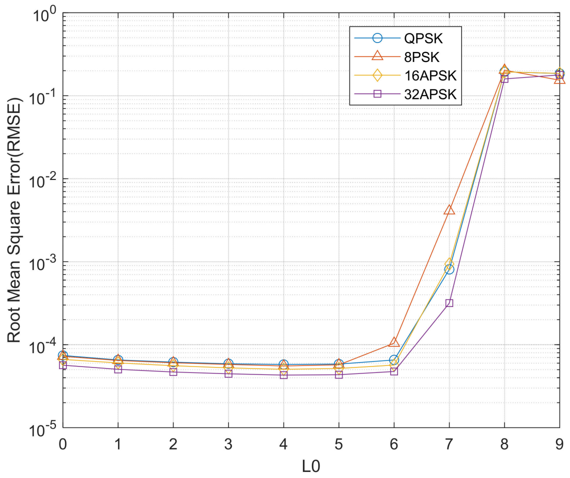

Figure 9. Effect of the number of superimposed pilot blocks on the performance of the RLR algorithm.

The differential detection of the SOF and PLSCODE algorithm detects the frame header and deduces the position of the pilot block. Furthermore, CFR reduces the CFO to 0.024% using 36 pilot symbols. The PA phase linear interpolator algorithm can correct the residual frequency deviation and phase deviation. As shown in Figure 10, the BER curve of the proposed carrier synchronization scheme almost coincides with the theoretical curve under four different modulations, and the demodulation performance loss is close to 0 dB. Therefore, the proposed carrier synchronization scheme is reliable under the condition of a low SNR and a normalized CFO of 20% of the symbol rate.

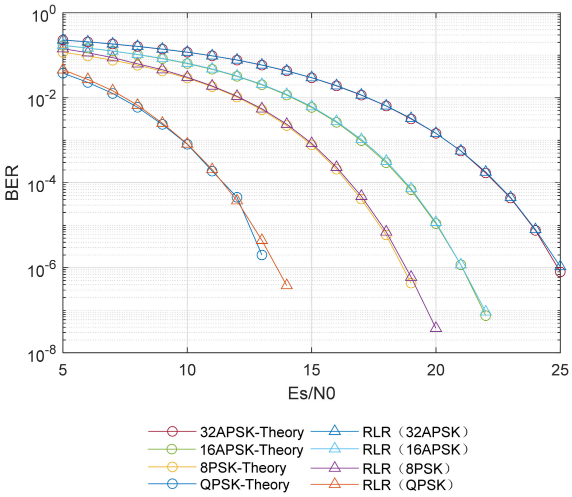

Figure 10. Simulation of BER curves of the proposed carrier synchronization scheme.

The hardware complexity of the conventional carrier frequency synchronization scheme and the proposed carrier frequency synchronization scheme are compared in

Table 1, where the proposed scheme simplifies the carrier frequency synchronization scheme from two-step to one-step. According to Table 1, compared with studies [2–4], multiplication resource consumption can be reduced by 90.68%, 72.47%, and 90.53%, respectively.

Table 1. Hardware complexity comparison.

		Literature 2	**Literature 3**	**Literature 4**	**This Paper**
Coarse CFR		D&M (M = 2)	Fitz (M = 2)	Modified M&M algorithm (M = 9)	RLR (N = 2 and N = 15)
	Multiplier	34	73	281	30
	Arc-tangent operations	1	2	1	1
Fine CFR		L&R (M = 9)	Simple Pilot Block Correlation algorithm	Simple Pilot Block Correlation algorithm	None
	Multiplier	288	36	36	0
	Arc-tangent operations	1	1	1	0

4.2. Carrier Synchronization Scheme Hardware Implementation

The proposed scheme was verified in the simulation environment of vivado2017.4 and the hardware platform of xcku040-ffva1156-2-e FPGA. The resource consumption and the maximum operating frequency for different functional modules were analyzed, as shown in Table 2. Frame synchronization utilizes 1.67% DSP resources, the CFR algorithm utilizes 12.50% DSP resources, and the CPR algorithm utilizes 0.73% DSP resources. The proposed RLR architecture can be realized by controlling the valid signal.

Table 2. Hardware utilization.

Resource Consumption	**Frame Synchronization**	**CFR Algorithm**	**CPR Algorithm**	**CR Scheme**
DSP	32 (1.67%)	240 (12.50%)	14 (0.73%)	290 (15.1%)
Register	13,970 (2.88%)	148,18 (3.06%)	6640 (1.37%)	35,905 (7.41%)
LUT	10,048 (4.15%)	10,293 (4.25%)	6511 (2.69%)	27,353 (11.28%)
Workable clock (MHz)	250	178.57	185.18	200.00

The operating frequency of the proposed scheme can be up to 200 MHz with less resource consumption and less complexity of implementation. Only 15.1% of the DSP resources are utilized.

5. Conclusions

Compared with the conventional scheme, the proposed scheme simplifies the carrier synchronization from three steps to two steps and dramatically reduces the multiplication of carrier synchronization, which is relatively simple and practical. In the pilot-aided VM system, the BER curve of the proposed carrier synchronization scheme is almost the same as the theoretical BER curve. The operating frequency of the proposed scheme can be up to 200 MHz. Therefore, it has a wide range of application prospects in high-speed equipment.

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