Article

An Optimum Structure of Scalable Capacitors in 3D Crosspoint Memory Technology

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Abstract: Memory chips need large capacitors in their periphery to drive boosted word-lines and bit-lines for read and write operations. In a previous work, scalable capacitors were proposed for 3D crosspoint memory to keep the area for the capacitors constant over technology generations. This paper proposes the capacitance models of three types of wiring capacitors: (1) vertical capacitor, (2) vertical and horizontal capacitor with next-neighbor wires connected with the other terminal, and (3) vertical and horizontal capacitor with next-neighbor pairs connected with the other terminal. These models are based on Wong's crossover capacitor model to determine the capacitor structure with the highest capacitance density in 3D crosspoint memory technology. One can determine the best structure through optimizing the process parameters such as the height H of the insulation material between the metal wires and the thickness T of the metal wires and the design rules such as the width W and space S of metal wires. The model accuracy was in good agreement with the measurement of twelve types of capacitor structures fabricated in a 180 nm 6 metal standard CMOS process with the maximum error of 20%. Contour plots of the capacitance density across H vs. S where it is assumed that $W = T = S$ are shown. As a result, the boundary condition regarding H and S is determined per 3D crosspoint memory technology with three, four, or five levels of wires.

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1. Introduction

Three-dimensional (3D) crosspoint memory has been developed to fill the performance gap between main memory and NAND Flash for improving the performance of the memory system with the minimum additional cost [1–8]. Memory elements are typically composed of phase change material [1–3] or conductive metal–oxide material [4–8]. To have a sufficient On–Off ratio between a selected memory and deselected ones even with two terminal devices, each memory cell has a selector connected in series with a non-volatile memory element vertically between a word-line (WL) and a bit-line (BL).

Figure 1a illustrates a 3D crosspoint memory array. In this example, the array has two levels of word-lines (WLs) and one level of bit-lines (BLs). There is a non-volatile memory cell at the crosspoint across a WL and a BL. Each cell has non-volatile material and a selecting device, which is shown by a diode in Figure 1a. To increase the bit density, the number of levels of WLs and BLs increases. When the number of accessible memory cells increases for higher performance in terms of read and write bandwidth as the number of levels of WLs and BLs increases, charge pump circuits driving WLs need to have increased drive current every time when the technology is advanced. The area of the charge pump circuits is basically proportional to that of the capacitors required for the demanded drive current. As a result, the control circuit placed in periphery tends to increase as the technology is advanced.

Figure 1. A structure of the crosspoint non-volatile memory array (a) and cross-sectional view of the chip where CMOS is fabricated under the array (b).

How has that issue been resolved in other memories? In [9–12], one can find circuit designs using memory structures as dense capacitors. Trench capacitors in DRAM have very high dense capacitance. The area of switched capacitor DC–DC voltage converters and decoupling capacitors can be reduced significantly by using trench capacitors [9,10]. Similarly, in [11], a highly efficient DC–DC converter using ferroelectric capacitors is developed. For 3D NAND Flash memory, charge pump circuits using tier capacitors that are composed of multiple WLs are developed in [12]. Even in logic chip, charge pumps are sometimes required to generate higher voltages on-chip for power gating. In [13], a voltage doubler was developed using wiring capacitance together with gate capacitance to minimize the capacitor area.

Likewise, to keep the circuit area constant over 3D crosspoint memory technology, a scalable capacitor structure was proposed in [14], as shown in Figure 1b. By using the wires for multiple WLs and BLs as wiring capacitors, the capacitance density is expected to increase in proportion to the number of wires in memory array. Thus, the charge pump area can be constant with scalable capacitors beyond technology transition. Then, what is the best capacitor structure to have the highest capacitance density? The answer would be dependent on the process parameters such as the height of the insulation material between the metal wires and the thickness of the metal wires and the design rules such as the width and space of the metal wires. We have capacitor models for parallel wires [15–17] and for crossover wires [18] at this point. In [15], an effective computation program was developed to obtain the capacitance of wires. In [16], wiring capacitance extraction was presented for post layout simulation with SPICE. In [17], explicit formulas were presented in terms of wire width, wire thickness, dielectric film thickness, and inter-wire spacing for covering arbitrary layouts. In [18], crossover capacitance was focused to have an explicit model for VLSIs with multilevel metal interconnect of arbitrary dielectric and wire thickness, width, and spacing in all layers. Various capacitor structures including both wires and vias are compared in terms of capacitance density, quality factor, and resonant frequency in [19]. However, one cannot determine the best structure for the scalable capacitors in 3D crosspoint memory technology based on those previous studies. Therefore, it should be beneficial for circuit designers to determine it with a simple capacitor model.

In this paper, the capacitance models of three types of wiring capacitors—(1) vertical capacitor, (2) vertical and horizontal capacitor with next-neighbor wires connected with the other terminal, and (3) vertical and horizontal capacitor with next-neighbor pairs connected with the other terminal—are developed based on Wong’s crossover capacitor model [18] to determine the capacitor structure with the highest capacitance density in 3D crosspoint memory technology. One can determine the best structure through optimizing the process parameters such as the height H of the insulation material between the metal wires and the thickness T of the metal wires and the design rules such as the width W and space S of metal wires. Section II discusses modeling of the capacitance of scalable capacitors. The model accuracy was in good agreement with the measurement of twelve types of capacitor

structures fabricated in a 180 nm 6 metal standard CMOS process with the maximum error of 20%. The measured data are shown in Section III. Contour plots of the capacitance density across H vs. S where it is assumed that $W = T = S$ are also shown.

2. Capacitor Model

2.1. Fabrication Steps

Figure 2 illustrates fabrication steps for the chip structure shown in Figure 1b. CMOS is fabricated for word-line (WL) and bit-line (BL) decoders in memory array and control circuits in the periphery at step (a). The first level WL is patterned above the decoding transistors at step (b). The same pattern remains above the control circuits in the periphery, which will be used as terminals of scalable capacitors. The first-level memory elements are formed in the memory array at step (c). The material for the memory elements is removed out of the periphery. Dielectric film is placed across a wafer to create isolation between the next-neighbor memory elements in the memory array and between the first and second metal wires in the periphery. The second level wires are patterned for the first-level BL in the memory array and for scalable capacitors in the periphery at step (d). The second-level memory elements are formed in the memory array and they are removed out of the periphery at step (e). One can repeat steps (b) through (e) to have multiple levels of WLs and BLs in the memory array and a denser capacitor structure in the periphery. After the memory array structure is finalized, additional metal wires are placed to connect the WLs and BLs with the decoding transistors in the memory array and to connect the wires in scalable capacitors with circuits in the periphery at step (f).

Figure 2. Fabrication steps from CMOS (a) through wiring (b–f).

2.2. Three-Capacitor Structures Studied in This Paper

To investigate which structure is the best in terms of capacitance density, i.e., capacitance per area as a function of process parameters such as the height (H) and thickness (T) of wires and design rules such as the width (W) and space (S) of wires, three capacitor structures are modeled. Figure 3 shows the three capacitor structures: vertical capacitor C_V (a) and vertical and horizontal capacitors C_{VH} (b) and C_{VH2} (c). Even and odd numbers of wires are connected to the first and second terminals in C_{VH} , whereas two next-neighbor wires are connected to the first and second terminals in C_{VH2} , alternately. It is assumed that every level of wires has the same values for H , T , W , and S .

Figure 3. Three capacitor structures studied in this paper: vertical capacitor C_V (a), and vertical and horizontal capacitors C_{VH} (b) and C_{VH2} (c).

2.3. Modeling

To estimate the capacitance of each structure of Figure 3, Wong's model [18] is utilized. The vertical capacitance component C_{VER} as shown in Figure 4a is composed of C_1 , C_2 , and C_3 as shown in Figure 4b. According to [18], each of the capacitance components are given by (2), (3), and (4), respectively.

$$C_{VER} = C_1 + C_2 + C_3 \quad (1)$$

$$\frac{C_1}{\epsilon} = \frac{W^2}{H} \quad (2)$$

$$\frac{C_2}{\epsilon} = 3.73W^{0.6}S^{0.4} \times \left(\frac{T}{T+0.035H} \right)^{0.64} \times \left(\frac{T}{T+0.851S} \right)^{0.12} \times \frac{H}{H+0.051S} \times \exp\left(\frac{-H}{0.7(S+0.4H)} \right) \quad (3)$$

$$\frac{C_3}{\epsilon} = 3.73W^{0.6}S^{0.3} \times \left(\frac{T}{T+0.035H} \right)^{0.64} \times \exp\left(\frac{-H}{0.7(S+0.4H)} \right) \times \left(\frac{H}{H+0.015S} \right)^3 \quad (4)$$

Figure 4. Breakdown of the capacitor; vertical capacitance components (a,b) and horizontal capacitance components (c–e).

The horizontal capacitance component C_{HOR} as shown in Figure 4c is given by either C_{h1} or C_{h2} , as shown in Figure 4d or Figure 4e, respectively. C_{h1} is the horizontal capacitance that sees adjacent levels of wires above and below, whereas C_{h2} is the horizontal capacitance that does not see adjacent levels of wires above and below. Based on [18], each of the capacitance components are given by (5) and (6), respectively.

$$\begin{aligned} \frac{C_{h1}}{\epsilon} = & 1.144 \frac{T}{S} \left(\frac{2H+T}{2H+T+2.059S} \right)^{0.0944} + 0.7428 \left(\frac{W}{W+1.592S} \right)^{1.144} \\ & + 1.158 \left(\frac{W}{W+1.874S} \right)^{0.1612} \times \left(\frac{2H+T}{2H+T+0.9801S} \right)^{1.179} \end{aligned} \quad (5)$$

$$\frac{C_{h2}}{\varepsilon} = 1.412 \frac{T}{S} \exp\left(-\frac{2S}{S+8.014H} - \frac{2S}{S+8.014H}\right) + 1.1852 \left(\frac{W}{W+0.3078S}\right)^{0.25724} \times \left\{ \left(\frac{H}{H+8.961S}\right)^{0.7571} + \left(\frac{H}{H+8.961S}\right)^{0.7571} \right\} \times \exp\left(-\frac{2S}{S+6H}\right) \quad (6)$$

For simplicity, this paper discusses the capacitors whose shape is square with a length of L . Therefore, the number of wires in each level (N) is $L/(W + S)$. When the number of levels of wires is M , the number of each capacitance component is given by Table 1.

Table 1. Number of capacitance components for the three capacitor structures.

	C_{VER} (Figure 4a)	C_{HOR} (Figure 4c)
C_V (Figure 3a)	$(M - 1) N^2$	None
C_{VH} (Figure 3b)	$(M - 1) N^2 / 2$	$M (C_{h1} N (N - 1) + C_{h2} (N - 1)^2)$
C_{VH2} (Figure 3c)	$(M - 1) N^2 / 2$	$M (C_{h1} N / 2 (N - 1) + C_{h2} (N / 2 - 1) (N - 1))$

As a result, C_V , C_{VH} , and C_{VH2} are given by (7), (8), and (9), respectively.

$$C_V = (M - 1) N^2 C_{VER} \quad (7)$$

$$C_{VH} = (M - 1) N^2 / 2 C_{VER} + M (C_{h1} N (N - 1) + C_{h2} (N - 1)^2) \quad (8)$$

$$C_{VH2} = (M - 1) N^2 / 2 C_{VER} + M (C_{h1} N / 2 (N - 1) + C_{h2} (N / 2 - 1) (N - 1)) \quad (9)$$

2.4. Comparison of the Capacitance Density between the Three Structures

In this section, various projections of the capacitance density based on the model given by (1) through (9) are studied. It is assumed that $S = W$ to minimize the bit cost. The aspect ratio of T/W can be more arbitrary, e.g., 1, 1.5 or 2 as a scaling rule, but in this study, the aspect ratio is assumed to be one. H is varied regardless of S , W , and T . Since Wong's model has a good accuracy when the ratio of the maximum value among W , S , T , and H to the minimum value among them is between 1 and 8 [15], those four parameters are varied from 5 to 40 nm in this study.

Figure 5a shows the capacitance of the vertical capacitor C_V shown in Figure 3a as a function of H when $M = 3$. The “parallel plate model” indicates that the capacitance is modeled by parallel plates where $C = \varepsilon/H$ as if three levels of wires are treated as plates rather than wires. When C_V is approximated by a form of $C_V \sim H^\alpha$, the power α is about -0.90 and -0.60 for $W = S = T = 5$ nm and 40 nm, respectively. It seems that the parallel plate model can predict the capacitance well for $W = S = T = H$, but the discrepancy increases when the difference between $W (=S = T)$ and H increases. Figure 5b shows the capacitance of the vertical/horizontal capacitor C_{VH} shown in Figure 3b as a function of $W (=S = T)$. The “parallel plate model” indicates that the capacitance is modeled by parallel plates where $C = \varepsilon/4(2M/S + (M - 1)/H)$. The first term is originated from the capacitance between next neighbors such as C_{h1} and C_{h2} of Figure 5, and the second term is from the crossover capacitance as C_1 of Figure 5.

To see which capacitor structure has the highest capacitance across the S - H plane, the capacitance ratios of C_V/C_{VH} and C_{VH1}/C_{VH} in case of M of 3 are shown in Figure 6a,b, respectively. There is a boundary between C_V and C_{VH} in Figure 6a; the more scaled in S , the larger C_{VH} , and the more scaled in H , the larger C_V . On the other hand, there is no boundary between C_{VH} and C_{VH2} in Figure 6b. As a result, the capacitor structure with the highest capacitance density can be either C_V or C_{VH} depending on the parameter condition on S and H .

Figure 5. (a) H vs. C_V and (b) $W (=S = T)$ vs. C_{HV} in case the number of wires is three.

Figure 6. (a) C_V/C_{VH} and (b) C_{VH1}/C_{VH} in case the number of wires is three.

The boundary condition depends on the number of metal wires, as shown in Figure 7. As the number of metal wires increases, C_{VER} has more impact on the total capacitance than C_{HOR} because C_{VER}/C_{HOR} is proportional to $1 - 1/M$. As a result, the boundary shifts toward the left top with a larger slope, as shown in Figure 7.

Figure 7. Boundary conditions on the S - H plane for the memory with three, four, and five metal wires.

When the parameters are somewhere in the area below the boundary line of Figure 8, the C_V structure should be used for higher capacitance density; otherwise, the C_{VH} structure

should be used. One can determine the best structure and the value of the capacitance density based on such a figure as Figure 8 easily once the process and design rules have been determined.

Figure 8. Contour plot of wiring capacitance across the H - S plane in case of $M = 5$.

2.5. Scalability of Capacitance across 3D Crosspoint Memory Technology

Figure 9 shows increases in capacitance across 3D crosspoint memory technology. C_{VH} is the best structure for $S = W = T = 10$ nm and $H = 20$ nm, as shown in Figure 9a, whereas C_V is the best one for $S = W = T = 10$ nm and $H = 20$ nm, as shown in Figure 9b. One can expect the increase in capacitance density by 8.2 nF/mm² or 7.1 nF/mm² per increase in the number of layers of two, respectively.

Figure 9. Capacitance vs. the number of wiring layers: (a) $S = W = T = 10$ nm, $H = 20$ nm, (b) $S = W = T = 25$ nm, $H = 7$ nm.

3. Measurement

To validate the model, twelve types of capacitor structure as shown in Table 2 were fabricated in 180 nm 6 metal CMOS, as shown in Figure 10. Each structure has $500 \mu\text{m} \times 300 \mu\text{m}$. Note that the H and T parameters are not allowed to be disclosed.

Table 2. Fabricated test structures for scalable capacitors.

	1	2	3	4	5	6	7	8	9	10	11	12
$S = W$ [μm]			0.28 μm						3.0 μm			
# wires		3			4			3			4	
C structure	C_V	C_{VH}	C_{VH2}	C_V	C_{VH}	C_{VH2}	C_V	C_{VH}	C_{VH2}	C_V	C_{VH}	C_{VH2}

Figure 10. Die photo.

The capacitance of each capacitor is measured and is subtracted by that of no structure, which only has pad and wiring capacitance to connect to a measurement tool. Two dies were measured and compared with the model, as shown in Figure 11. The errors between the measured data and the calculated one using the model were 20% at the largest. As projected by the model, C_{VH} is the best capacitor structure when the wires are as narrow as $0.28\ \mu\text{m}$ and as short space as $0.28\ \mu\text{m}$, while C_V is the best capacitor structure when the wires are as wide as $3.0\ \mu\text{m}$ and as large space as $3.0\ \mu\text{m}$. Even though the number of capacitor types was limited, the model was validated.

Figure 11. Measured vs. model capacitance.

4. Discussions

Table 3 summarizes the differences from the previous studies. In [18], it is assumed that each level of wires is routed perpendicularly to lower and upper levels, and there is no via placed on the wires. Thus, three-dimensional crossover capacitance was modeled. In [19], vias are included to increase the capacitance per area, and vertical parallel plate and vertical bars are considered as well as a horizontal parallel plate. On the other hand, in this work, wires are routed as in [18] with no vias because the design rule of the capacitor is the same as the memory array where the pitch is tighter than the design rule allowing vias, but other capacitor structures such as C_V and C_{VH2} are discussed as well as C_{VH} .

Table 3. Comparison with the previous studies [18,19].

	Wong [18]	Aparico [19]	This Work
Studied structure	C_{VH}	Horizontal and vertical parallel plate, Vertical bars	C_V, C_{VH}, C_{VH2}
With vias?	No	Yes	No

In this work, only the capacitance density is considered. To design the capacitor array, one needs to determine the size of the unit capacitor. Since the wires of the capacitor need to be connected at the edges of the array due to mismatch in the design rules between the inside and outside of the memory array, the operation frequency of the capacitors decreases as the capacitor array size increases. Therefore, how to determine the capacitor unit size needs to be given for circuit designers as a function of the required operation frequency, which needs to be done in the future work. When the capacitors are used in DACs and comparators, the matching property of the capacitors can limit the accuracy of such analog circuits. The matching property also needs to be addressed in the future work.

5. Conclusions

This paper studied the design of scalable capacitors for 3D crosspoint memory. Three types of structures namely C_V , C_{VH} , and C_{VH2} were modeled, and their capacitance density was compared across S ($=W=T$) and H . The boundary conditions to determine the best capacitor structure were shown under the condition of $W=S=T$ for the memory technology with three, four, and five levels of wires as demonstration. The test structures were fabricated in 180 nm standard CMOS to validate the models. Since the capacitance model includes W , S , T , and H as independent parameters, one can identify the best structure based on the models once the technology including the number of wires and process parameters such as H and T , and the design rules of S and W are determined. In this paper, only the capacitance density was focused. Therefore, how to determine the capacitor array size needs to be given for circuit designers as a function of the required operation frequency, which should be done in the future work.

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Nomenclature

W	Width of each wire
S	Space between wires
T	Thickness of wires
H	Height of dielectric film between levels of wires
C_{VER}	Vertical capacitance component
C_{HOR}	Horizontal capacitance component
C_V	Vertical capacitor
C_{VH}	Vertical and horizontal capacitors where even and odd numbers of wires are connected to the first and second terminals
C_{VH2}	Vertical and horizontal capacitors where two next neighbor wires are connected to the first and second terminals

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