Article

A 6.89-MHz 143-nW MEMS Oscillator Based on a 118-dB Ω Tunable Gain and Duty-Cycle CMOS TIA

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Abstract: This article presents a 6.89 MHz MEMS oscillator based on an ultra-low-power, low-noise, tunable gain/duty-cycle transimpedance amplifier (TIA) and a bulk Lamé-mode MEMS resonator that has a quality factor (Q) of 3.24×10^6 . Self-cascoding and current-starving techniques are used in the TIA design to minimize the power consumption and tune the duty-cycle of the output signal. The TIA was designed and fabricated in TSMC 65 nm CMOS process technology. Its open-loop performance has been measured separately. It achieves a tunable gain between 107.9 dB Ω and 118.1 dB Ω while dissipating only 143 nW from a 1 V supply. The duty-cycle of the output waveform can be tuned from 23.25% to 79.03%. The TIA has been interfaced and wire bonded in a series-resonant oscillator configuration with the MEMS resonator and mounted in a small cavity standard package. The closed-loop performance of the whole oscillator has been experimentally measured. It exhibits a phase noise of -128.1 dBc/Hz and -133.7 dBc/Hz at 1 kHz and 1 MHz offsets, respectively.

Keywords: oscillator; transimpedance amplifier (TIA); microelectromechanical systems (MEMS); bandwidth trade-off; duty-cycle; low-noise; phase noise; reference frequency; ultra-low power

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1. Introduction

Timing and frequency reference oscillators are pivotal blocks in almost all electronic systems. Emerging applications, including internet-of-things (IoT) and mobile devices, impose stringent requirements on power consumption (battery life), cost, and size [1]. In recent years, MEMS-based reference oscillators have become a key alternative to those based on quartz crystal resonators to enable miniaturized systems along with high performance levels [2–4]. Figure 1 shows the block diagram of a MEMS-based oscillator system, where a transimpedance amplifier (TIA) and a MEMS resonator are connected in a positive feedback loop. R_M , C_M , L_M , C_f , and C_P are the MEMS resonator's electrical model motional resistance, motional capacitance, motional inductance, feedthrough capacitance, and parasitic capacitance, respectively.

The loop sustains oscillation if the forward gain of the TIA overcomes the resonator series losses represented by R_M . Typically, MEMS resonators are actuated by either piezoelectric or capacitive transduction mechanisms. Piezoelectrically transduced resonators have smaller R_M (less losses) but require specialized fabrication technologies that are not available in many standard semiconductor foundries. Capacitively transduced resonators have a higher R_M in the range of tens of k Ω but are more suited for monolithic CMOS integration [5], and these devices offer a high-quality factor (Q), small size, and good stability [6–11]. Capacitive MEMS resonators require a high gain TIA to compensate for the high R_M . Further, a low phase shift near the oscillation frequency (f_o) is needed to sustain oscillation. This results in the trade-off between the need for a high gain-bandwidth product and low power consumption.

Figure 1. MEMS-based series resonant oscillator.

In this work, a 6.89 MHz MEMS oscillator based on a high Q bulk Lamé-mode MEMS resonator and an ultra-low-power, low-noise TIA is presented. A design methodology to achieve low power consumption and low phase noise is proposed, demonstrating the efficacy of using a high (Q) resonator to reach an ultra-low power design for the CMOS sustaining circuitry. The novel use of the self-cascoding and current-starving techniques in the TIA design has been introduced to minimize the power consumption and tune the duty-cycle of the output signal. Duty-cycle tuning is an added feature that can be used by other applications that requires a tunable duty-cycle, including switched-capacitor filters [12] and pulse-width control [13]. The fully integrated and packaged oscillator solution at this frequency achieves a very competitive performance in terms of power consumption and phase noise. The entire mounted system in a small cavity standard package significantly reduces the system cost and form factor compared using an external quartz crystal as a reference resonator.

Section 2 discusses the MEMS-based oscillator, showing the resonator and the sustaining amplifier circuit used in forming the oscillator. It presents the proposed methodology, TIA circuit design, and noise analysis. Section 3 covers the performance and robustness of the proposed TIA circuit. Section 4 shows the experimental validation used to test the stand-alone TIA performance, the measurement results of the overall oscillator system, and provides a comparison with the state-of-the-art designs. Finally, Section 5 provides the conclusion of the presented work.

2. MEMS-Based Oscillator

Figure 2 shows the MEMS-based oscillator block diagram. The oscillator is based on a differential bulk square resonator connected in a positive feedback loop with the TIA. The oscillator is then to be connected to an integer- N PLL to synthesize a higher output frequency from the proposed input MEMS-based reference oscillator. The focus of the work here is the MEMS-based oscillator (not the PLL).

Figure 2. Proposed MEMS-based oscillator block diagram.

2.1. Bulk Lamé-Mode Square Resonator

The MEMS resonator used in this work is a bulk Lamé-mode wafer-level vacuum encapsulated at 10 mTorr. The resonator is fabricated using the MEMS Integrated Design for Inertial Sensors (MIDIS) technology, a pure-play commercial process provided by Teledyne DALSA Semiconductor Inc. It features low-leakage and vacuum level ultra-clean encapsulation. At a polarization voltage (V_P) of 40 V, the measured resonance frequency (f_r) is 6.8953 MHz, with a Q factor of 3.24×10^6 . This leads to a frequency-quality factor (f -Q) product of 2.23×10^{13} Hz. Figure 3 shows the measured frequency response of the resonator at a V_P of 40 V.

Figure 3. Measured MEMS electrical transmission (S21): the blue curve is the magnitude (left y-axis), and the green curve is the phase (right y-axis) [14].

Figure 4 shows the fitted linear RLC electrical equivalent model extracted by measuring the output of the resonator at 6.89 MHz while being biased at a V_P of 40 V [14].

Figure 4. Extracted RLC equivalent model.

2.2. Sustaining Amplifier Configurations and Topologies

Figure 5 shows simple diagrams of different TIA configurations and topologies. There are two main general configurations used to realize a TIA: the open-loop configuration and the closed-loop (feedback) configuration. The open-loop TIA configuration is based on amplifying the input current using a current amplifier (A_I), then converting it into an output voltage by passing the output current through a resistive load. Although open-loop TIAs may offer a lower power consumption than the closed-loop ones, they have a higher noise that cannot be tolerated for some applications [15]. On the other hand, the closed-loop configuration offers a lower noise and a more flexible gain–bandwidth (GBW) trade-off relationship. This makes it the most used for micromechanical oscillators. This configuration is based on a voltage amplifier (A_V) with a negative shunt–shunt feedback from the output to the input. The shunt–shunt feedback lowers the system input and output impedances by the loop gain, which helps in increasing the TIA’s bandwidth. In addition, the amplifier’s input-referred noise is reduced by the square of the feedback resistor, bringing an extra advantage for low phase-noise MEMS-based oscillator applications.

Figure 5. Different TIA configurations and topologies.

Different topologies, including common-source (CS), common-gate (CG), and common-drain (CD), are used to realize the single stage or multistage amplifier. The CG topology, such as the regulated-cascode (RGC) amplifier, inherently, has low input impedance but suffers from a high input-referred noise. This makes the CG topology unsuitable for low-phase noise and low-power applications [16]. The CD topology offers a low output impedance but exhibits a poor linearity and a low dynamic range, resulting in higher phase-noise. The CS topology offers a larger output swing and can be operated from a lower supply, which further helps in reducing the power consumption. In addition, the dynamic range is improved due to the higher output swing resulting in a lower phase-noise floor. All these features make the closed-loop configuration, negative shunt-shunt feedback CS topology better suited for capacitive MEMS resonators and an optimum choice for our application.

2.3. Proposed Methodology and TIA Circuit

For an RLC circuit in a closed loop with a TIA, as shown in Figure 1, the total phase in the loop at the frequency of oscillation (f_o) is, theoretically, zero. For a TIA phase shift (φ), where $|\tan \varphi| \ll Q$, Equations (1) and (2) from [17] can be applied:

$$f_o \approx f_r \left(1 + \frac{\tan \varphi}{2Q}\right), \quad (1)$$

where f_r is the resonance frequency. A unity loop gain should be maintained at f_o ; hence, a TIA gain (R_{TIA}) is required as:

$$R_{TIA} \geq \frac{R_M}{|\cos \varphi|}. \quad (2)$$

Thus, for a very high Q MEMS resonator as the one used here, which has a Q of 3.24×10^6 , a phase shift of -80° changes f_o by only 2 ppm. Equations (1) and (2) show that a tolerable phase shift can be used to save significant power, which would have otherwise been needed to obtain a large bandwidth while not taking the full advantage of the high Q of the resonator. Thus, as shown in Figure 6a, the proposed TIA uses three distinct features: (a) self-cascode, (b) current-starving, and (c) long transistor channel length (L). Figure 6b shows the self-cascode technique that is used for low-voltage operation. It reduces the channel length modulation effect while offering high output swing and DC gain [18].

Figure 6. Proposed TIA circuit diagram: (a) one half of the differential signal path for simplicity and (b) self-cascode composite structure.

The self-cascode structure consists of two transistors forming a composite transistor that mimics the same DC characteristics of a single long-channel transistor with a uniform width. It introduces two advantages over its DC-equivalent uniform-width single transistor: (a) a substantial area saving and (b) a higher cut-off frequency [19]. M_2 in Figure 6b always operates in the triode region, while M_1 can be operating either in the triode or the saturation regions. At the edge of saturation, the composite drain-source voltage ($V_{DSsat-composite}$) can be expressed as:

$$\begin{aligned} V_{DSsat-composite} &= V_{DSsat1} + V_{DS2} \\ &= V_{OV1} + I_{D2}R_{DS2}, \end{aligned} \quad (3)$$

where V_{OV1} is the overdrive voltage of M_1 . R_{DS2} is the on resistance of M_2 while operating in the triode region. This implies that the V_{DS2} is very small and makes no discernible difference in the composite V_{DSsat} compared to that of its equivalent single transistor. This qualifies the self-cascode structure for low-power and low-voltage applications compared to regular-cascode structures that need a higher operating voltage [20,21]. The composite achieves a larger effective L —lower output conductance—by stacking smaller, shorter-length transistors. Assuming $L_1 = L_2$ and $W_1 = mW_2$, the composite effective aspect ratio is expressed as:

$$\frac{W}{L}|_{composite} = \frac{1}{m+1} \cdot \frac{W}{L}|_1 = \frac{m}{m+1} \cdot \frac{W}{L}|_2. \quad (4)$$

From a layout perspective in advanced CMOS process technology nodes, most foundries strongly recommend in their process design kits (PDKs) building a long gate transistor length by stacking short gate transistors. This improves matching and the uniformity of the layout, which results in a more compact area by reducing the use of extra dummy layout cells used to ensure transistor layout uniformity post-fabrication. In addition, it is more precise in terms of the device model introduced by the PDK, as the device models may become inaccurate for very long gate lengths. The sum of the area footprints of M_1 and M_2 is smaller than that of the equivalent simple transistor. In addition, stacking reduces the leakage when the transistors are off. A stack of 2-transistors has $10\times$ reduced leakage than that of an equivalent single transistor. This helps in reducing power dissipation. For equal chip areas, the voltage-gain (A_V) relationship between the regular-cascode, the self-cascode, and a simple transistor is given by:

$$A_{V_{regular-cascode}} > A_{V_{self-cascode}} > A_{V_{simple-transistor}}. \quad (5)$$

although the regular cascode has a higher A_V , this comes at the expense of a higher voltage drop (less headroom) and more power consumption.

The current starving technique controls the charging/discharging current flow to tune the duty-cycle, offering better noise performance [22,23], and reduces the power consumption. Finally, increasing the transistor channel length helps in reducing the output phase noise and the power consumption.

2.4. Noise Analysis

In MEMS oscillators, there are two main noise sources: (a) thermal noise from the resonator represented by $4k_B T/R_M$, where T is the absolute temperature and k_B is the Boltzmann constant, and (b) the TIA's input-referred current noise $\overline{i_n^2}$. From [10,17,24], for a $|\tan\phi| \ll Q$ and at low-frequency offsets (Δf), close to the carrier, the phase noise will be low as it is shaped by the resonator high Q , and it is given by:

$$\mathcal{L}(\Delta f)|_{Resonator} = \frac{1}{v_{drive}^2} \frac{K_B T R_M}{Q^2} \frac{f^2}{\Delta f^2}, \quad (6)$$

the phase noise floor is proportional to R_M^2 and $\overline{i_n^2}$ and can be expressed as:

$$\mathcal{L}(\Delta f)|_{Floor} = \frac{1}{v_{drive}^2} \overline{i_n^2} \frac{R_M^2}{\Delta f}, \quad (7)$$

where v_{drive} is the resonator input driving voltage. Thus, it is important to minimize $\overline{i_n^2}$. The shunt-shunt negative feedback reduces the amplifier's input-referred noise power spectral density by the square of the feedback resistance and helps compensate for the direct proportionality of the noise floor to R_M^2 . Neglecting the flicker noise, the thermal input-referred current noise for the design proposed here can be expressed as

$$i_n^2 = 4k_B T \left[\frac{\omega^2 C_{in}^2 \gamma}{g_{m1} + g_{m4}} + \frac{1}{R_{ctrl}} \right], \quad (8)$$

where k_B is the Boltzmann constant, T is the absolute temperature, ω is the angular frequency, C_{in} is the TIA total input capacitance, γ is a noise coefficient that depends on the transistor channel length (L), g_{m1} and g_{m4} are the transconductances of M_1 and M_4 , respectively, and R_{ctrl} is the shunt-shunt feedback resistor realized by transistor M_f .

3. System Performance and Robustness

3.1. Specifications and Performance

To sustain oscillations, an enough high gain is required to compensate for the MEMS resonator losses that are modeled with the resonator motional resistance (R_M) in the electrical model. The used bulk Lamé-mode resonator has an R_M of 199.1 k Ω , which corresponds to 105.97 dB Ω losses. The designed TIA should at least have a gain of 105.97 dB Ω to compensate for the resonator losses. Practically, at start-up, a higher gain may be needed to start the oscillation, where having a tunable gain feature becomes valuable.

The proposed TIA is developed in the TSMC 65 nm CMOS process technology. An open-loop simulation test is performed while loading the TIA with the MEMS resonator electrical model to check the TIA gain (G_{TIA}) and performance. The designed TIA has a minimum gain of 107.6 dB Ω , which covers the minimum required gain to compensate for the resonator losses and any extra parasitic losses. The gain is tunable between 107.6 dB Ω and 118.2 dB Ω . The duty-cycle of the output waveform tested after the driving stage is tunable between 23.9% and 79.7%.

3.2. Robustness

To test the sensitivity of the proposed TIA circuit over transistor mismatches, a spectre post-layout *conservative* simulation was carried out on the circuit shown in Figure 6a using a Monte-Carlo analysis with a number of runs $N = 500$. Figure 7a shows the histogram of the TIA's maximum gain: $G_{TIA-Max} = 118.2$ dB Ω . It reports a mean of 118.17 dB Ω and a standard deviation (std) of 0.226 dB Ω . For the TIA's minimum gain, $G_{TIA-Min} = 107.6$ dB Ω , as shown by the histogram in Figure 7b, the mean and the std are 107.66 dB Ω and 0.864 dB Ω , respectively.

Figure 8 shows the post-layout TIA gain over three process corners (FF, TT, SS), supply variation range ($1 \text{ V} \pm 0.05 \text{ V}$), and temperature between ($-10 \text{ }^\circ\text{C} \rightarrow 80 \text{ }^\circ\text{C}$) to test the design robustness over the process, voltage, and temperature (PVT) variations. The graph indicates a maximum gain tuning range of 10.6 dB Ω under the TT corner and a minimum gain tuning range of 9.3 dB Ω under the SS corner.

Figure 7. Monte-Carlo histograms of the proposed TIA ($N = 500$): (a) $G_{TIA-Max} = 118.2$ dBΩ and (b) $G_{TIA-Min} = 107.6$ dBΩ.

Figure 8. The TIA gain control under PVT variations.

4. Experimental Results

To validate the fabricated design, the CMOS circuits have been tested in an open-loop configuration while considering all parasitic loads to validate the TIA open-loop performance. Then, a closed-loop testing has been performed after wire bonding the CMOS circuits to the MEMS resonator to test the closed-loop feedback oscillator performance. Five CMOS dies have been tested in total, and all the results are within 0.3% of the TT corner performance, which is in a good agreement with our Monte Carlo simulations.

4.1. Open-Loop Validation

The stand-alone performance of the proposed TIA has been tested separately, without the MEMS resonator. Figure 9a shows the micrograph of the fabricated die highlighting the TIA block. The total active TIA CMOS area is $150.29 \mu\text{m}^2$ ($12.38 \mu\text{m} \times 12.14 \mu\text{m}$).

Figure 9. (a) Fabricated die micrograph and (b) photograph of the PCB used to test the TIA.

The prototype CMOS die is assembled in an 80-pin ceramic quad flat pack (CQFP) package and mounted on a custom 4-layer printed circuit board (PCB), as shown in Figure 9b. The test board includes SMA connectors for the input/output signals, coupling capacitors (1 μF) at the input signals to filter out the DC component, and a voltage regulator (Analog Devices ADP1707ARDZ-1.2-R7) to regulate the input supply from a DC power supply source (Agilent E3646A). In addition, all power nets are decoupled with a network of decoupling capacitors (10 nF, 100 nF, 1 μF) connected in parallel and in an ascending order from the integrated circuit (IC) package lead. There are other components on the PCB—Figure 9b—that are not related to this specific TIA test.

A measurement setup has been built to test the TIA in an open-loop configuration without being connected to the MEMS resonator. First, we have built a post-layout simulation environment on Cadence that only includes the TIA in an open-loop configuration. Second, we modeled all the loading and the parasitic effects added by the measurement equipment and the PCB in the simulation environment to fairly compare the simulation

results with the measurements. This validates the TIA performance and assures proper functionality when bonded to the MEMS resonator in a closed-loop feedback configuration.

To mimic the MEMS resonator, an excitation voltage at a frequency of 6.89 MHz was used, and a resistor (R_{v-i}) was placed in series with the TIA input to convert this excitation voltage to a current in the range of the MEMS resonator sensed current. Figure 10 depicts the testing method, including all sources of parasitics.

Figure 10. TIA open-loop test method, showing one-half of the differential signal path for simplicity.

The test has been applied in both the Cadence simulation environment and the measurement setup. Figure 11 shows the matching of the transient differential outputs obtained from both the simulation and the measurement.

Figure 11. TIA differential output transient response, both measured and simulated.

The amount of parasitics seen by the TIA on the PCB while being connected to the measurement equipment is very large compared to when being only connected directly to the MEMS resonator. When the TIA is connected to the MEMS resonator in a closed feedback loop—which is the case in the end application—it is only loaded by less than 0.5 pF parasitic capacitance. On the other hand, in this PCB measurement setup, as will be shown shortly, the total parasitic capacitances loading the TIA output and input are 74.85 pF and 105.4 pF, respectively. Adding these loads in the Cadence simulation model will decrease the output signal amplitude by a considerable amount. This is expected as the TIA is designed to interface directly with the MEMS resonator where the level of parasitics is greatly reduced. By replicating the PCB parasitics in our Cadence model simulations, we can directly compare the results to see if the TIA is performing as expected. Table 1 shows the list of loads and parasitic effects.

Table 1. Loading and Parasitic Capacitances.

Parasitic/Load Type	Symbol	Value
Oscilloscope	C_{Osc}	11 pF
	R_{Osc}	1 M Ω
SMA Connector	C_{SMA1}	104.15 pF
	C_{SMA2}	62.6 pF
Package Lead	C_{Pkg}	0.25 pF
PCB Trace	C_{Tr}	1 pF

The capacitances of the used SMA connector cables (C_{SMA1} , C_{SMA2}) have been measured using a bench LCR/ESR meter (BK Precision 889B). The PCB traces capacitances and the CQFP package lead capacitance have been estimated based on [25] and [26], respectively. The oscilloscope loading resistance (R_{Osc}) and capacitance (C_{Osc}) were found in the oscilloscope (Agilent InfiniiVision DSO-X 2004A) manual [27]. After de-embedding the loading effects of the parasitics, the TIA performance has been captured. Figure 12 shows the measured transimpedance gain of the TIA. It reports the maximum gain at the resonance frequency (f_r). The corresponding phase shift is -75.41° , which is the maximum phase shift that can occur. It is within the acceptable range, as discussed and shown earlier using Equations (1) and (2). For a lower gain, the phase shift will decrease.

Figure 12. Measured TIA transimpedance gain compared to simulation.

It is worth noting that, in this work, the main objective all along has been to minimize power consumption while delivering an acceptable noise performance. The goal was not to solely minimize noise.

After an oscillator starts up, Equation (1) determines the noise performance. The effect of the phase shift, namely how far it occurs away from the resonator peak, is directly reflected in the phase noise performance. What permits the design to achieve very low power consumption is the very high Q -factor of the resonator used.

If we were to solely target noise minimization with this high Q -factor MEMS resonator instead of minimizing power, we could have achieved a much better noise performance than what we report here, but this obviously would have come at the expense of more power consumption and may have affected the overall figure of merit (FoM) achieved. This is a classic example of design parameters “balancing” based on the resources at hand

and on the ultimate target objectives of the work: minimize power consumption while delivering a competitive *FoM*.

The measured tunable TIA gain with V_{ctrl} is shown in Figure 13. It can be tuned between 107.9 dB Ω and 118.1 dB Ω . Figure 14 shows that the duty-cycle is tunable between 23.25% and 79.03%. All results are in a good agreement with the simulations. The actual measurement setup and its block diagram are depicted in Figure 15.

Figure 13. Measured tunable TIA gain from 108 dB Ω up to 118.03 dB Ω compared to simulation.

Figure 14. Measured tunable duty-cycle from 23.25% to 79.03% compared to simulation.

(a)

(b)

Figure 15. TIA open-loop validation: (a) picture of the actual setup and (b) setup block diagram.

4.2. Closed-Loop Validation

The loop is closed to measure the oscillator's performance after de-embedding the loading effects. The two die—MEMS and CMOS—are wire bonded together and packaged in an 80-pin quad flat no-lead (QFN) package. The QFN package has been chosen instead of the QFP due to the lower loading capacitance of its leads [26,28]. The package is mounted on a new custom PCB. All power nets are decoupled with a network of decoupling capacitors (10 nF, 100 nF, 1 μ F) connected in parallel and in an ascending order from the IC package lead. A resistor of 1 M Ω has been connected in series between the MEMS V_P and the DC power supply source (BK PRECISION 9110) to limit the maximum current on the polarization terminal in the case of an accidental pull-in between the electrodes of the

MEMS device. Another DC power supply source (Agilent E3646A) was used to supply the CMOS circuits with a 1 V supply voltage. The (V_P) has been raised up gradually, reaching a stable output at $V_P = 40$ V. Oscillation start-up was ensured by design: The nominal gain of the TIA was set to be higher than the absolute minimum theoretical value in order to account for all process corners and potential PVT variations. The natural nonlinearities of the TIA/resonator act as intrinsic gain control. The provision of an additional/backup manual gain control could be used to reduce the gain to emulate an AGC whenever that was needed. Figure 16 shows the phase noise of the oscillator's output. It reports a phase noise (PN) of -128.1 dBc/Hz and -133.7 dBc/Hz at 1 kHz and 1 MHz offsets, respectively. The TIA total power consumption (P_{DC}) is 143 nW from a 1 V supply. Figure 17 shows the testing PCB and the wire bonded dies in the mounted package.

Figure 16. Measured 6.89 MHz oscillator phase noise compared to simulation.

Figure 17. (a) Photograph of the testing board used to test the oscillator. (b) Picture of the wire-bonded dies, CMOS and MEMS, in the package.

4.3. Figure of Merit

Table 2 compares this work with previously published state-of-the-art. To fairly compare different oscillators with different resonator R_M and f_o values, the figure of merit (FoM), as proposed by Seth et al. [17], was used:

$$FoM = \frac{1}{\mathcal{L}(\Delta f \rightarrow f_o)} \frac{k_B T}{P_{DC}} R_M^2 f_o^2, \quad (9)$$

where $\mathcal{L}(\Delta f \rightarrow f_o)$ is the phase noise 1 MHz offset, and P_{DC} is the DC power consumption in Watt.

Table 2. Oscillator Performance Summary and Comparison to the State-of-the-Art.

Ref. No.	[2]	[17]	[29]	[30]	[31] *	[32]	[33]	[34]	[35]	This Work
Trans Mech ^{''}	Piezo ⁺	Cap [†]	Cap	Cap	Piezo	Cap	Cap	Cap	Cap	Cap
Process	65 nm	0.35 μm	0.13 μm	0.35 μm	0.18 μm	65 nm	0.35 μm	0.35 μm	0.35 μm	65 nm
f_o (MHz)	14.42	20	20	0.551	75.01 **	17.93	61	1.23	1.12	6.89
V_P $\otimes$ (V)	-	-	5	18	-	100	7.45	7	25	40
Q	4.9×10^3	1.6×10^5	10^4	2×10^3	9.5×10^3	8.9×10^5	80×10^3	1.9×10^3	2.1×10^3	3.24×10^6
R_M (k Ω)	0.9	65	31	930	0.0326	35	13.8	16×10^3	2×10^3 •	199.1
G_{TIA} (dB Ω)	69	-	112.5	157	-	98	-	138	121	118.1
P_{DC}	1.4 mW	6.9 mW	360 μW	8.5 μW	7.8 mW	900 μW	78 μW	150 μW	930 μW	143 nW
PN _{1 kHz} (dBc/Hz)	-116	-	-125.6	-103.8	-108	-120	-130	-106	-	-128.1
PN _{1 MHz} (dBc/Hz)	-130	-131 \$	-131.9	-121 \$	-133.15	-127	-152 \$	-111 \$	-	-133.7
$FoM _{1 \text{ MHz}}$ (Hz ² Ω^2)	4.98×10^{15}	1.4×10^{19}	6.8×10^{19}	1.6×10^{20}	6.56×10^{13}	3.8×10^{19}	5.96×10^{22}	1.44×10^{21}	-	1.3×10^{24}

^{''} Trans Mech: Transduction Mechanism. ⁺ Piezo: Piezoelectric. [†] Cap: Capacitive. $\otimes V_P$ is the MEMS resonator polarization voltage.

• Deduced, approximately, from the measured motional resistance plot in the paper. * This paper includes a PLL as a part of the whole oscillator. The reported performance (f_o , PN, P_{DC}) includes the PLL. ** This is the oscillator center/carrier frequency output from the PLL after being converted up from the MEMS ($f_r = 27.19$ MHz). \$ Deduced, approximately, from the measured phase noise plot in the paper.

It considers several points including: (a) for a very high Q , the $1/f^2$ and $1/f^3$ regions occur at low-frequency offsets. Thus, the PN at 1MHz offset dominates and becomes the primary performance metric in these reference oscillators. (b) The DC power consumption, and hence, the PN should be normalized to it. (c) The PN at 1MHz offset of a reference oscillator in a PLL is scaled by the square of the division ratio; thus, the reference oscillator's PN should be scaled to the inverse square of the reference frequency ($1/f_o^2$). (d) The PN at 1MHz offset also scales with the square of the resonator motional resistance R_M , which is not part of the TIA circuit design, so the PN should be scaled as well by $1/R_M^2$.

This FoM is used in Table 2 to compare this work with previously published state-of-the-art. This work reports the highest FoM compared to other works reported in the literature.

5. Conclusions

In this paper, we have successfully implemented an extremely low-power, tunable gain/duty-cycle TIA. The TIA was integrated with a very high-quality factor (Q) bulk Lamé-mode MEMS resonator to implement an oscillator with competitive performance in terms of power consumption and phase noise. The TIA structure is based on the self-cascoding technique. The TIA has been fabricated in a TSMC 65 nm CMOS process. Experimental validations, open-loop and closed-loop, have been carried out to test the TIA performance. The TIA has a tunable gain from 107.9 dB Ω to 118.1 dB Ω and a tunable duty-

cycle between 23.25% and 79.03% while consuming only 143 nW from a 1 V supply. The proposed design enables the TIA to be easily transferred and adopted into new, advanced CMOS technologies with lower supply conditions, thanks to the self-cascoding technique used. The oscillator reaches a phase noise of -128.1 dBc/Hz and -133.7 dBc/Hz at 1 kHz and 1 MHz offsets, respectively.

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