Article

Common-Mode Voltage Reduction Algorithm for Photovoltaic Grid-Connected Inverters with Virtual-Vector Model Predictive Control

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Abstract: Model predictive control (MPC) has been proven to offer excellent model-based, highly dynamic control performance in grid converters. The increasingly higher power capacity of a PV inverter has led to the industrial preference of adopting higher DC voltage design at the PV array (e.g., 750–1500 V). With high array voltage, a single stage inverter offers advantages of low component count, simpler topology, and requiring less control tuning effort. However, it is typically entailed with the issue of high common-mode voltage (CMV). This work proposes a virtual-vector model predictive control method equipped with an improved common-mode reduction (CMR) space vector pulse width modulation (SVPWM). The modulation technique essentially subdivides the hexagonal voltage vector space into 18 sub-sectors, that can be split into two groups with different CMV properties. The proposal indirectly increases the DC-bus utilization and extends the overall modulation region with improved CMV. The comparison with the virtual-vector MPC scheme equipped with the conventional SVPWM suggests that the proposed technique can effectively suppress 33.33% of the CMV, and reduce the CMV toggling frequency per fundamental cycle from 6 to either 0 or 2 (depending on which sub-sector group). It is believed that the proposed control technique can help to improve the performance of photovoltaic single-stage inverters.

Keywords: common-mode voltage; delay; inverters; multi-step model predictive control; non-zero vector; space vector pulse width modulation

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1. Introduction

Solar photovoltaic (PV) energy generation, wind energy generation, and other new energy technologies are constantly being developed. Control and modulation techniques of voltage source inverter (VSI), which is the main physical interface between renewable energy sources and the power grid, have garnered considerable research attention [1]. In standard MPC schemes, the use of all actual voltage vectors inherently results in elevated CMV. On the other hand, MPC schemes with SVPWM uses virtual vector vectors and the CMV performance depends primarily on the modulation design. High peak CMV and frequent toggling of CMV of converters may reduce the system reliability, posing potential safety concerns [2,3].

Numerous research works on CMV suppression have been reported to date. In general, these solutions on CMV performance can be categorized into hardware-based and software-based techniques. In the hardware-based solutions, CMV is typically mitigated by incorporating a passive filter or optimizing the voltage source inverter topology [4,5].

However, this approach necessitates additional hardware, resulting in higher maintenance effort and costs. On the other hand, software-based CMV suppression methods can be subdivided further into those based on direct control scheme and those based on pulse width modulation (PWM). In the direct control group, e.g., direct MPC with actual voltage vectors, it is common to augment the cost objective into considering CMV as a cost component [6,7]. These approaches necessitate the design of a suitable weight factor to balance the various cost components in the cost function. L. Guo et al. suggests an MPC scheme with preselected voltage vectors having low CMV [8,9]. However, the preselection has limited the amount of voltage vectors available, and therefore results in a higher harmonic distortion. MPC-based CMV suppression methods have been studied in conjunction with various inverter topologies [10–12].

PWM modulation techniques can be modified to restrain CMV. For example, the CMV can be suppressed by only using either odd or even voltage vectors [13]. However, the corresponding DC-bus utilization factor is very poor. In addition, non-zero voltage vector modulation approaches, such as active zero-state switch PWM [2], near-state PWM [14,15], and remote-state PWM [16] have been reported in the past. Moreover, [17,18] compare the performance indices of various modulation schemes, in terms of e.g., CMV amplitude, output THD. Table 1 summarizes the advantages and disadvantages of the proposed techniques. Moreover, other CMV-related works have attempted to improve other inverter efficiency indicators, such as switching losses [15,19], restraining common-mode electromagnetic interference [20], or leakage current in photovoltaic grid-connected inverter [21,22]. Furthermore, [23] suggests a hybrid modulation based on the modulation magnitude, resulting in varying CMV performance. Another hybrid modulation is studied in [24] but it requires a common-mode inductor, which increases the system cost and design complexity. In [25], an enhanced discontinuous modulation is proposed to reduce the line switching loss while suppressing CMV. However, if the switching sequences in the subdivided sectors of the hexagonal voltage vector space can be ordered more optimally, further improvement may be achieved. There are other simplified PWM techniques [26–28], each with respective merits and demerits. Similarly, PWM-based CMV improvement have been studied in conjunction with different inverter topologies [29–32].

Table 1. Advantages and disadvantages of different modulations.

Advantages		Disadvantages
SVPWM	Lower switching losses [33]	Potentially high calculation burden [33]
AZSPWM	High modulation index range, high DC-bus utilization [22]	Line-to-line voltage pulse reversal [34]
NSPWM	Low CMV amplitude, less switching losses [34]	Higher in ripple and switching losses [33]
RSPWM	Theoretically non-changing CMV [16]	Low DC-bus utilization [16]

This paper’s contribution is as follows: (1) In the proposed improved common-mode reduction space vector pulse width modulation (CMRSVPWM) with 18 sub-sectors organizes the switching sequences in each sub-sector into resulting lower CMV amplitude and oscillation frequency; (2) MPC uses a large amount of virtual voltage vectors, such that all the 18 subsectors can be fully utilized. By combining the virtual vector MPC and CMRSVPWM, the CMV performance of the single-stage inverter can be improved.

The following is the structure of the article: Section 2 introduces the mathematical model and MPC for a three-phase two-level photovoltaic inverter, together with the standard SVPWM and its CMV property. Section 3 proposes the virtual vector MPC with the improved CMRSVPWM modulation, where the details of division, vector selection, and CMV amplitude and frequency are described. Section 4 compares the performance with the standard SVPWM and the proposed CMRSVPWM method using simulation studies. Section 5 summarizes and concludes the overall findings. Section 6 provides proposes directions for future work. The Appendix A contains two tables. Table A1 shows the definition of acronym. Meanwhile, Table A2 shows the definition of notations in this paper.

2. Virtual-Vector MPC

2.1. Three-Phase PV VSI Model

Figure 1 shows the topology of the three-phase two-level single-stage photovoltaic inverter that is connected to a three-phase grid (emulated using ideal three-phase source). As described, this topology is relevant to photovoltaic application with high DC array voltage (e.g., 750 V to 1500 V).

Figure 1. Model of the grid connected PV system.

In Figure 1, V_{dc} is the output voltage of PV array, V_a , V_b and V_c are the inverter output voltages, L and R are filter inductor and its internal resistance, and e_a , e_b , and e_c are the emulated AC grid voltages. Point O is the grounded neutral of the AC grid. The plant under control can be represented by the set of Equation (1):

$$\begin{cases} V_a = L \frac{di_a}{dt} + Ri_a + e_a \\ V_b = L \frac{di_b}{dt} + Ri_b + e_b \\ V_c = L \frac{di_c}{dt} + Ri_c + e_c \end{cases} \quad (1)$$

Through Clarke transformation, the circuit voltage equations are transformed from the three-phase coordinate to the $\alpha\beta$ two-phase stationary coordinate, giving Equation (2):

$$\begin{cases} L \frac{di_\alpha}{dt} = V_\alpha - Ri_\alpha - e_\alpha \\ L \frac{di_\beta}{dt} = V_\beta - Ri_\beta - e_\beta \end{cases} \quad (2)$$

Each symbol in Equation (2) has the same meanings as defined above, but now the $\alpha\beta$ coordinate. Since the PV inverter contains three sets of switches, they are capable of producing a total of eight switching states. The relationship between the output voltages and the switching states can be described by Equation (3), where parameter a defines the unit vector that introduces 120° phase difference among phases:

$$\begin{cases} V_i = \frac{2}{3} V_{dc} (S_a + a S_b + a^2 S_c) \\ a = e^{j\frac{2\pi}{3}} = -\frac{1}{2} + j\frac{\sqrt{3}}{2} \end{cases} \quad (i = 0, 1 \dots 7) \quad (3)$$

where V_i represents the output voltage obtainable from different switching states, S_a , S_b , and S_c represent, respectively, the states of each switch, and V_{dc} is the DC-bus voltage. The combination of these eight switching states corresponds to eight actual/basic voltage vectors that can be denoted as $V_0 \sim V_7$. V_0 and V_7 are zero voltage vectors, and the other six are non-zero voltage vectors, with the same amplitude, but different phase angles.

2.2. Model Predictive Control of VSI

Using forward-Euler method to discretize the grid current model [9]:

$$\begin{cases} i_{\alpha}(k+1) = \frac{1}{RT_s+L}[Li_{\alpha}(k) + T_s V_{\alpha}(k) - T_s e_{\alpha}(k)] \\ i_{\beta}(k+1) = \frac{1}{RT_s+L}[Li_{\beta}(k) + T_s V_{\beta}(k) - T_s e_{\beta}(k)] \end{cases} \quad (4)$$

where $i_{\alpha}(k+1)$ and $i_{\beta}(k+1)$ are the predicted values of $\alpha\beta$ -axis currents at $(k+1)$ th time instant, $i_{\alpha}(k)$ and $i_{\beta}(k)$ are the $\alpha\beta$ -axis current feedback at k th sampling instant, T_s is the sampling period in seconds, and $e_{\alpha}(k)$ and $e_{\beta}(k)$ are the $\alpha\beta$ -axis grid voltage at k th sampling instant.

Standard single-vector MPC analyzes only eight actual voltage vectors per control cycle to identify the switching state with the lowest cost value. If the control sampling frequency is insufficiently high, three-phase currents will suffer from higher harmonics. To improve this aspect, virtual voltage vectors, or sub-voltage vectors, are considered in this study.

It has been well-established that the inherent digital implementation delay has to be compensated in MPC implementation in conjunction with power electronic application. Two-step ahead prediction technique is utilized to compensate the inherent delay [6]. With this two-step MPC, the cost function can be written as Equation (5):

$$g = |i_{\alpha}^* - i_{\alpha}(k+2)| + |i_{\beta}^* - i_{\beta}(k+2)| \quad (5)$$

where i_{α}^* and i_{β}^* are the reference values of the $\alpha\beta$ -axis currents that can be obtained from inverse-Clarke transformed of synchronous-axis current. $i_{\alpha}(k+2)$ and $i_{\beta}(k+2)$ are the $\alpha\beta$ -axis currents at $(k+2)$ th instant.

2.3. CMV of Basic Voltage Vectors

Equation (6) is used to calculate the PV inverter's CMV without regard for the DC side's midpoint voltage fluctuation [35]:

$$V_{cmv} = (V_{ao} + V_{bo} + V_{co})/3 \quad (6)$$

where V_{ao} (V_{bo} and V_{co}) is the voltage between the phase-A (phase-B and phase-C) output of the inverter and the DC neutral point. Table 2 summarizes the CMV induced by the switching combinations. CMV has four values, $\pm V_{dc}/2$ and $\pm V_{dc}/6$, where the two of the zero voltage vectors have the highest peak CMV.

Table 2. Common-mode voltage of the space vectors.

Voltage Vectors	V_{cmv}	Voltage Vectors	V_{cmv}
$V_0(0,0,0)$	$-V_{dc}/2$	$V_4(0,1,1)$	$V_{dc}/6$
$V_1(1,0,0)$	$-V_{dc}/6$	$V_5(0,0,1)$	$-V_{dc}/6$
$V_2(1,1,0)$	$V_{dc}/6$	$V_6(1,0,1)$	$V_{dc}/6$
$V_3(0,1,0)$	$-V_{dc}/6$	$V_7(1,1,1)$	$V_{dc}/2$

2.4. Conventional Modulation Method

In the conventional SVPWM, six non-zero vectors naturally divide into six equilateral triangular sectors $S_1 \sim S_6$ in the $\alpha\beta$ -plane, which is shown in Figure 2a. Using the first sector as an example, Figure 2b illustrates how a voltage vector can be synthesized from the actual voltage vectors.

Figure 2. Conventional SVPWM.

Under the sector S_1 , the action times of each vector can be calculated according to the volt-second principle, as in Equation (7) [35]:

$$\begin{cases} T_{PWM} V_{ref} = T_1 V_1 + T_2 V_2 + T_0 V_0 + T_7 V_7 \\ T_{PWM} = T_1 + T_2 + T_0 + T_7 \end{cases} \quad (7)$$

where T_{PWM} is the sampling time of one control/PWM cycle, V_{ref} is the reference voltage vector, V_0 , V_1 , V_2 , and V_7 are the voltage vectors selected for synthesis, and T_0 , T_1 , T_2 and T_7 are the corresponding action time periods. T_0 and T_7 are typically equal.

In Table 2, the highest CMV is $V_{dc}/2$ because SVPWM employs zero voltage vectors. In what follows, we introduce AZSPWM [2], NSPWM [14], and RSPWM [16]—these PWM techniques share the common feature of suppressing the CMV amplitude and toggling frequency. Figure 3 illustrates an example of synthesized switching waveforms for each of the aforementioned modulation techniques and the associated CMV.

Figure 3. Cont.

Figure 3. Synthesis and the corresponding CMV.

3. Proposed CMRSVPWM Methods for VSI

3.1. Sectors of CMRSVPWM

In order to reduce the amplitude and toggling frequency of CMV and increase the DC-bus utilization, CMRSVPWM is proposed in this work.

It begins with subdividing the basic six sectors, then divides each basic sector into three parts. The two sections vertex at the origin have the same modulation index range, so they are combined into the first component of CMRSVPWM (CMRSVPWM I), which forms the hexagonal star shape. The remaining six triangular areas are the second portion of CMRSVPWM (CMRSVPWM II). Modulation index determines which of the regions should be used. Note that since each of the six sub-regions of CMRSVPWM I contains two basic sectors, it is important to determine the precise location of the reference voltage vector. Figure 4 shows that the angle between two sector boundaries that can be used to decide whether odd or even voltage vectors are used in the synthesis process.

Figure 4. Sectors of CMRSVPWM.

SVPWM that uses only odd or even vectors for synthesis will result in a very-low DC-bus utilization rate. Figure 5a shows that the DC-bus utilization rate, which is essentially equal to the radius r_1 ($= V_{dc}/3$) of the inner tangent circle of the middle-side triangle.

CMRSVPWM I in this work intends to improve this aspect. Figure 5b shows the maximum linear output voltage is now increased to radius $r_2 (= 2\sqrt{3}V_{dc}/9)$, which is the inner tangent circle of the hexagonal star shape. The DC-bus utilization of CMRSVPWM I is increased by 15.47%, as compared to the scheme with either odd or even vectors, while continuing to suppress the CMV peak amplitude.

Figure 5. DC-bus utilization.

3.2. CMRSVPWM I

The action times of voltage vector can be solved using the volt-second principle. Modulation index M_i is introduced in Equation (8) [35]:

$$M_i = \frac{\pi V_{ref}}{2V_{dc}} \quad (8)$$

The action times corresponding to the voltage vector $V_1 \sim V_6$ are $T_1 \sim T_6$. The general equations that solve for the action times are shown in Equation (9).

$$\begin{cases} T_1 = (1/3 + 2M_i \cos\theta / \pi) T_{PWM} \\ T_3 = (1/3 - M_i \cos\theta / \pi + \sqrt{3}M_i \sin\theta / \pi) T_{PWM} \\ T_5 = (1/3 - M_i \cos\theta / \pi - \sqrt{3}M_i \sin\theta / \pi) T_{PWM} \\ T_2 = (1/3 + M_i \cos\theta / \pi + \sqrt{3}M_i \sin\theta / \pi) T_{PWM} \\ T_4 = (1/3 - 2M_i \cos\theta / \pi) T_{PWM} \\ T_6 = (1/3 + M_i \cos\theta / \pi - \sqrt{3}M_i \sin\theta / \pi) T_{PWM} \end{cases} \quad (9)$$

Table 3 summarizes the switching sequences in each sector (clockwise direction is assumed).

Table 3. Voltage vector action sequences under CMRSVPWM I.

Sectors		Sequences	Sectors		Sequences
S1	S1-1	$V_1 V_5 V_3 V_5 V_1$	S4	S4-1	$V_4 V_2 V_6 V_2 V_4$
	S1-2	$V_3 V_1 V_5 V_1 V_3$		S4-2	$V_6 V_4 V_2 V_4 V_6$
S2	S2-1	$V_2 V_6 V_4 V_6 V_2$	S5	S5-1	$V_5 V_3 V_1 V_3 V_5$
	S2-2	$V_4 V_2 V_6 V_2 V_4$		S5-2	$V_1 V_5 V_3 V_5 V_1$
S3	S3-1	$V_3 V_1 V_5 V_1 V_3$	S6	S6-1	$V_6 V_4 V_2 V_4 V_6$
	S3-2	$V_5 V_3 V_1 V_3 V_5$		S6-2	$V_2 V_6 V_4 V_6 V_2$

3.3. CMRSVPWM II

Another main contribution of this work is to propose on the use of both CMRSVPWM I and CMRSVPWM II modes to address the problem of limited usable modulation index range in CMRSVPWM I alone, therefore improving the DC-bus utilization. This scheme that combines CMRSVPWM I and CMRSVPWM II into suppressing CMV is known as CMRSVPWM in what follows. With CMRSVPWM II mode, the DC-bus utilization is further increased from $2\sqrt{3}V_{dc}/9$ (in CMRSVPWM I) to $2V_{dc}/3$ as Figure 6 shows. The modulation index M_i decides on which modes, I or II, to be used. Odd-even vectors mixing modulation is used to synthesize the reference voltage vector in CMRSVPWM II. Table 4 details the switch action sequences for each sector in the CMRSVPWM II.

Figure 6. DC-bus utilization.

Table 4. Voltage vector action sequences under CMRSVPWM II.

Sectors	Sequences	Sectors	Sequences
S1	$V_1 V_2 V_4 V_2 V_1$	S4	$V_4 V_5 V_1 V_5 V_4$
S2	$V_2 V_3 V_5 V_3 V_2$	S5	$V_5 V_6 V_2 V_6 V_5$
S3	$V_3 V_4 V_6 V_4 V_3$	S6	$V_6 V_1 V_3 V_1 V_6$

Again, using the first sector for illustration, Figure 7 shows the synthesis of the both CMRSVPWM modes and the corresponding CMV. In theory, CMRSVPWM I has no CMV fluctuation, i.e., zero voltage toggling frequency, within a modulation cycle. CMRSVPWM II, on the other hand, manifests twice voltage change/toggling. Note that the CMV peak voltages in both modes are $V_{dc}/6$.

Figure 7. Synthesis of CMRSVPWM and the corresponding CMV.

4. Experimental Result and Discussion

The proposed MPC and CMRSVPWM methods are investigated using Matlab-Simulink. Figure 8 depicts the control loop. A 380 V 50 Hz AC grid is assumed. The DC-bus voltage is chosen to be 750 V, but it is noted that single-stage voltage source inverter typically have higher varying DC voltage, e.g., in the range of 750 V to 1500 V.

Figure 8. Overall structure of simulation.

4.1. Virtual-Vector MPC

To fully utilize the entire voltage vector space, virtual vector MPC is used in this work. First, a range of selection of virtual vectors is investigated. Virtual voltage vectors are chosen at the angular phase angle intervals of 30, 45, and 60 degrees within the modulation limit. Then, each selected voltage vector is divided into 1, 2, 5, 10, and 20 sub-voltage vectors based on the magnitude length. The resulted THDs of these combinations are summarized in Figure 9.

Figure 9. Model of the grid connected PV system.

When the interval angle is the same, selecting more sub-voltage vectors results in a lower THD value. When the same number of sub-voltage vectors (in each phase angle value) is used, the THD value decreases as the angle interval decreases. As shown in Figure 9, there is only a small different of 0.01% for the selections of 10 and 20 sub-voltage vectors. With the consideration of computational burden, the virtual voltage vectors with a

30-degree angle interval (around the hexagonal voltage vector space, as show in Figure 10) and ten sub-voltage vectors (equal, for each phase angle) are used in this work.

Figure 10. Hexagonal voltage space with 120 sub-vectors(points)—used by the virtual vector model predictive control.

4.2. CMV Simulation

Table 5 describes the parameters used by the simulation model, and the inverter control part adopts the standard two-step ahead MPC method.

Table 5. Simulation Parameters.

Parameters	Values	Parameters	Values
DC side voltage V_{dc}	750 V	DC side capacitance C	$5 \times 10^3 \mu\text{F}$
Current reference I_{ref}	10 A	Switching frequency f_s	5 kHz
Filter inductance L	4 mH	MPC sampling time T_s	2×10^{-4} s
Filter resistance R	0.01Ω	Modulated sampling time T_{PWM}	2×10^{-4} s
Grid voltage e	380 V	Predictive horizon (first step to overcome digital delay)	2
Grid frequency f_g	50 Hz	Control horizon	1

The comparison in Figure 11a,b shows that the simulation results are consistent with the theoretical analysis. The peak and valley values of CMV in conventional SVPWM are $\pm 375\text{V} (\pm V_{dc}/2)$, while the peak and valley values of CMRSVPWM are $\pm 125\text{V} (\pm V_{dc}/6)$, representing a decrease of 66.67%. Notably, CMRSVPWM has fewer CMV frequency jumps per fundamental cycle.

Figure 11. CMV under different strategies.

Phase-A current and its THD values for SVPWM and CMRSVPWM are shown in Figure 12a,b. Both have a period of 0.02 s and an amplitude of 9.994 A. Next, phase-A output voltages are compared in Figure 13a,b. The amplitudes of 311.4 V of the phase-A voltages are comparable for both.

Figure 12. Outputs current of inverter.

Figure 13. Outputs phase-A voltage of inverter.

Characteristics of several PWM techniques targeting CMV improvement, and that of the proposed CMRSVPWM I and CMRSVPWM II, are listed in Table 6. All techniques with improved CMV property can reduce the peak CMV to $V_{dc}/6$. The proposed CMRSVPWM has the best combination of DC-bus utilization and CMV frequency (which is either 0 or 2, due to the two modes). For current THD (where only that for SVPWM, AZSPWM, NSPWM and CMRSVPWM are measured; all four modulation schemes have the same DC-bus

utilization), and they have practically the same value, agreeing with theoretical expectation.

Table 6. Characteristic of different PWM modulation techniques targeting CMV improvement.

	SVPWM	AZSPWM	NSPWM	RSPWM	CMRSVPWM I	CMRSVPWM (I and II)
Peak CMV	$V_{dc}/2$	$V_{dc}/6$	$V_{dc}/6$	$V_{dc}/6$	$V_{dc}/6$	$V_{dc}/6$
CMV frequency	6	6	4	0	2	0 or 2
CMV frequency at changing sectors	0	1	1	0	1	1
DC bus utilization	$2V_{dc}/3$	$2V_{dc}/3$	$2V_{dc}/3$	$V_{dc}/3$	$2\sqrt{3}V_{dc}/9$	$2V_{dc}/3$
Phase-A current THD	0.61%	0.74%	0.64%			0.75%

5. Conclusions

Space vector modulation is enhanced to reduce the property of the single-stage voltage source inverter. The following results are taken from the simulation experiment:

- (1) In comparison to the SVPWM, the enhanced CMRSVPWM strategy decreases the CMV amplitude from $V_{dc}/2$ to $V_{dc}/6$, a reduction of 66.67%. The CMV toggling frequency is reduced to either 0 or 2.
- (2) In comparison with the PWM techniques with either three odd or three even vectors, the proposed CMRSVPWM I will increase the utilization rate of the DC bus by 15.47%, reaching $2\sqrt{3}V_{dc}/9$. The utilization rate is increased further through CMRSVPWM II, up to the maximum available rate as that of SVPWM.
- (3) Through virtual-vector MPC with 120 sub-vectors, the entire range of CMRSVPWM can be utilized to output switching harmonic performance.

6. Deficiencies and Prospects

In actual implementation, a dead zone will manifest itself during the modulation phase. However, since the focus of this article is on the use of the proposed CMRSVPWM in conjunction with virtual-vector MPC, the dead zone is not considered. Future work will explore this issue in greater detail.

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Appendix A

Table A1. Definition of acronym in paper.

VSI	Voltage Source Inverter	SVPWM	Space Vector Pulse Width Modulation
MPC	Model Predictive Control	AZSPWM	Zero-State Switch Pulse Width Modulation
CMV	Common-Mode Voltage	NSPWM	Near-State Pulse Width Modulation
PWM	Pulse Width Modulation	RSPWM	Remote-State Pulse Width Modulation
THD	Total Harmonic Distortion	CMRSVPWM	Common-Mode Reduction Space Vector Pulse Width Modulation

Table A2. Definition of notations in paper.

V_{dc}	Output voltage of PV	$i_{\alpha\beta}(k+2)$	Currents in $(k+2)T_s$
V_{abc}	Inverter output voltages	$i_{\alpha\beta}^*$	Reference current values on $\alpha\beta$ axis
i_{abc}	Inverter output currents	T_s	Sampling time
e_{abc}	Grid voltages	L	Filter value
$i_{\alpha\beta}$	Output currents on $\alpha\beta$ coordinate system	R	Filter's internal resistance
$V_i(i = 0, 1 \dots 7)$	Output voltage from different switching states	V_{cmv}	Common-mode voltage value
a	Phase difference of 120°	V_{ao}	Voltage between the phase-A output of the inverter and the DC neutral point
S_{abc}	States of switch	T_{PWM}	Sampling time of one cycle
$i_{\alpha\beta}(k)$	Feedback values of $\alpha\beta$ axis currents at the current time	$T_i(i = 0, 1 \dots 7)$	Corresponding action times of voltage vectors
$e_{\alpha\beta}(k)$	Grid voltage values of $\alpha\beta$ axis at the current moment	M_i	Modulation index
$i_{\alpha\beta}(k+1)$	Predicted values of $\alpha\beta$ axis currents at the next moment		

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