

Article

Short-Term to Long-Term Plasticity Transition Behavior of Memristive Devices with Low Power Consumption via Facilitating Ionic Drift of Implanted Lithium

Young Pyo Jeon [†], Yongbin Bang [†], Hak Ji Lee, Eun Jung Lee, Young Joon Yoo ^{*} and Sang Yoon Park ^{*}

Center for Applied Electromagnetic Research for Advanced Institute of Convergence Technology, Seoul National University, Gyeonggi-do, Suwon 16229, Korea; jyp83e@snu.ac.kr (Y.P.J.); yongbin@snu.ac.kr (Y.B.); lhj6115@snu.ac.kr (H.J.L.); lee13@snu.ac.kr (E.J.L.)

^{*} Correspondence: youngjoonyoo@snu.ac.kr (Y.J.Y.); yoonpark77@snu.ac.kr (S.Y.P.)

[†] These authors contributed equally to this work.

Abstract: Recent innovations in information technology have encouraged extensive research into the development of future generation memory and computing technologies. Memristive devices based on resistance switching are not only attractive because of their multi-level information storage, but they also display fascinating neuromorphic behaviors. We investigated the basic human brain's learning and memory algorithm for "memorizing" as a feature for memristive devices based on Li-implanted structures with low power consumption. A topographical and surface chemical functionality analysis of an Li:ITO substrate was conducted to observe its characterization. In addition, a switching mechanism of a memristive device was theoretically studied and associated with ion migrations into a polymeric insulating layer. Biological short-term and long-term memory properties were imitated with the memristive device using low power consumption.

Keywords: memristive device; short-term memory; long-term memory; lithium; plasticity



Citation: Jeon, Y.P.; Bang, Y.; Lee, H.J.; Lee, E.J.; Yoo, Y.J.; Park, S.Y. Short-Term to Long-Term Plasticity Transition Behavior of Memristive Devices with Low Power Consumption via Facilitating Ionic Drift of Implanted Lithium. *Electronics* **2021**, *10*, 2564. <https://doi.org/10.3390/electronics10212564>

Academic Editor: Zhaoyang Fan

Received: 10 September 2021

Accepted: 17 October 2021

Published: 20 October 2021

Publisher's Note: MDPI stays neutral with regard to jurisdictional claims in published maps and institutional affiliations.



Copyright: © 2021 by the authors. Licensee MDPI, Basel, Switzerland. This article is an open access article distributed under the terms and conditions of the Creative Commons Attribution (CC BY) license (<https://creativecommons.org/licenses/by/4.0/>).

1. Introduction

The demand for data processing in computing systems is significantly increasing, as data processing has become more complicated due to the diversity of information types, and since new developments in technology, such as big data, deep learning artificial intelligence (AI), and the internet of things (IoT), are enabling us to access an enormous amount of information in real time. The von Neumann architecture, which is a modern computing system consisting of a control, arithmetic/logic, registers, and memory units, has critical disadvantages for managing massive data processing such as the inability to conduct parallel implementation, the Von Neumann bottleneck, and has high-power consumption due to the fact of sequential instruction processing [1–8].

Neuromorphic computing, which imitates the human brain's information processing, has been proposed as an alternative computing architecture to sequential data processing [9–13]. The major idea behind the proposed neuromorphic computing concept is collocating memory and processing units involving parallel data processing that separate parts of a complex task into smaller and independent parts to efficiently handle larger amounts of data. However, neuronal circuitry based on conventional silicon complementary metal oxide semiconductors (CMOS) is disappointing due to the low learning and non-volatile synaptic behavior. Thus, the fulfillment of scalable and high-performance neuromorphic hardware requires a new concept of devices serving synapse mimicking phenomena such as short-term and long-term plasticity.

Recently, novel designed devices have shown promise for realizing the synaptic dynamics in the learning process through various mechanisms of ferroelectric effects [14,15], spintronic effect [16], phase transitions [17,18], and ionic transfer [19,20]. Among these,

research on memristive devices employing the connection phenomenon of ion filaments or oxygen vacancy has been conducted by storing information with their conductance states and exhibiting conductivity modulation based on the programming electric field [21–23]. Rapid diffusive ions, such as Ag^+ and Cu^{2+} , or oxygen vacancy migrate into the insulating medium materials to form a filamentary structure, and silicone-based compounds are also implemented as a conductive bridge to effectively devise short-term memory (STM) and long-term memory (LTM) [24–27]. The key issue involved in the low power consumption of the memristive devices performing STM and LTM is that the switching materials can be easily ionized and aid in high filamentary connectivity by the applied electric stimulus.

In this study, the basic human brain's learning and memory algorithms for STM and LTM and their transition behaviors with memristive devices were observed. The structure of the memristive device consisted of a metal/(polymeric) insulator/metal (MIM) containing Li that was mainly a resistive switching material for ionic drift and filamentary formation. For effective resistive switching, the Li was implanted in an ITO using the thermal evaporation method, because Li has very low ionization energy; therefore, it was easily ionized and effortlessly immigrated by an applied electric field for the development of ionic filament between the top and bottom electrodes. The implanted Li was determined by X-ray photoelectron microscopy (XPS) analysis, and the origin of the electrical characteristics of the Li-implanted memristive device was investigated through surface analyses via scanning electron microscopy (SEM) and atomic force microscopy (AFM). The memristive device with an Li-implanted ITO performed hysteresis behavior with a voltage sweep from -2 to 2 V and a 10^2 on/off ratio as a resistive switching device, which we evaluated as the digital data storage capability. Furthermore, the memristive devices achieved the brain mimicking behavior of STM and LTM conductance dynamics with an exceptionally low power of 70 pJ per programming. Eventually, we investigated whether our device was able to operate analog data processing based on the frequency domain to mimic the human nervous system.

2. Experimental Details

2.1. Memristive Devices' Fabrication

ITO-coated glass substrates were serially cleaned with acetone, methanol, and deionized water using an ultra-sonication cleaning bath for 20 min. The cleaned substrates were dried using high-purity N_2 (99.9%) gas before the substrates were processed using an optical treatment with an ultraviolet ozone cleaner for 20 min to smooth and modify the surface of ITO. The Li granular (high-grade sodium, Sigma–Aldrich) was a 99% metal basis with a 4–10 mesh particle size and contained 0.5% of sodium. The Li was implanted onto the ITO by vacuum evaporation under a pressure of 1×10^{-6} Torr. The quantity of implanted Li was controlled by quartz crystal microbalance embedded in the vacuum evaporation system and monitored at 1 A/s for 50 s. After the vacuum evaporation of Li onto the ITO to contribute their doping profile, the Li:ITO/substrate was annealed at 200 °C for 2 h in a vacuum chamber. Polyvinylpyrrolidone (PVP) powder (100 mg) was dissolved in 5 mL of ethanol solvent for 30 min with magnetic stirring. The PVP solution was deposited on the Li-implanted ITO/glass as a polymeric insulating layer. The polymer thin film was spin-coated at 2000 rpm for 30 s and then annealed on a hot plate at 145 °C for 30 min to remove the residual solvent. After the baking process, an Ag electrode was deposited to a thickness of 100 nm using vacuum evaporation under a pressure of 1×10^{-6} Torr. The Ag electrode and the ITO substrate corresponded to the top electrode (TE) and the bottom electrode (BE), respectively.

2.2. Characterization and Device Performance Measurement

XPS was performed using a Theta Probe Base System (Thermo Fisher Scientific Co.) with monochromic Al $K\alpha$ radiation at an energy of 25 W after the Li-implanted ITO/glass was prepared. Morphological analyses of the Li-implanted ITO were carried out using field emission scanning electron microscopy (FE-SEM, JSM-7100F, JEOL Ltd.) and AFM

measurement (Park Systems, XE-100). The electrical properties of the Li-implanted memristive device were measured using a Keithley 4200-SCS semiconductor parameter analyzer coupled with a Keithley 4225-PMU pulse measurement unit. The currents were simultaneously measured while applying bias voltages in both the sweeping and pulse modes. Due to the limited resolution during measurement with the pulse operation system, the current output under $1 \mu\text{A}$ was modified to $0.05 \mu\text{A}$, collectively. The conductance was calculated by using the current–voltage (I–V). The presented data are the best case in a trial to explain and to represent the device’s performance.

3. Results and Discussion

Schematic diagrams for the implantation process of Li onto an ITO and the fabrication of the memristive devices, including deposition of the polymeric insulating layer and the top electrode, are given in Figure 1a. Figure 1b shows a cross-sectional SEM image of the PVP/Li:ITO/glass with a defining thickness of 179 nm of PVP on an Li:ITO/substrate. From the AFM image of $5 \times 5 \mu\text{m}$, the average surface roughness of the Li:ITO was 97.2 nm as shown in Figure 1c, and the particles were confirmed to be Li, which was supported by XPS analysis, because Li was partially implanted on the surface of the ITO originating from a very low growth rate in thermal evaporation process [28]. In order to characterize the Li:ITO, the XPS peaks of the Li:ITO over annealing periods of 200°C were studied as shown in Figure 1d,e. Generally, the corresponding peak of Li 1s was originally centered at 55 eV, and the Li 1s’ corresponding peak of the annealed Li:ITO/substrate appeared at 55.04 eV, which shows that the Li was effectively deposited onto ITO as shown Figure 1d [29,30]. In addition, the atomic proportion for Li s1 of the Li:ITO with a thermal treatment of 30.65% was quantitatively higher than that without the thermal treatment of 29.78%.

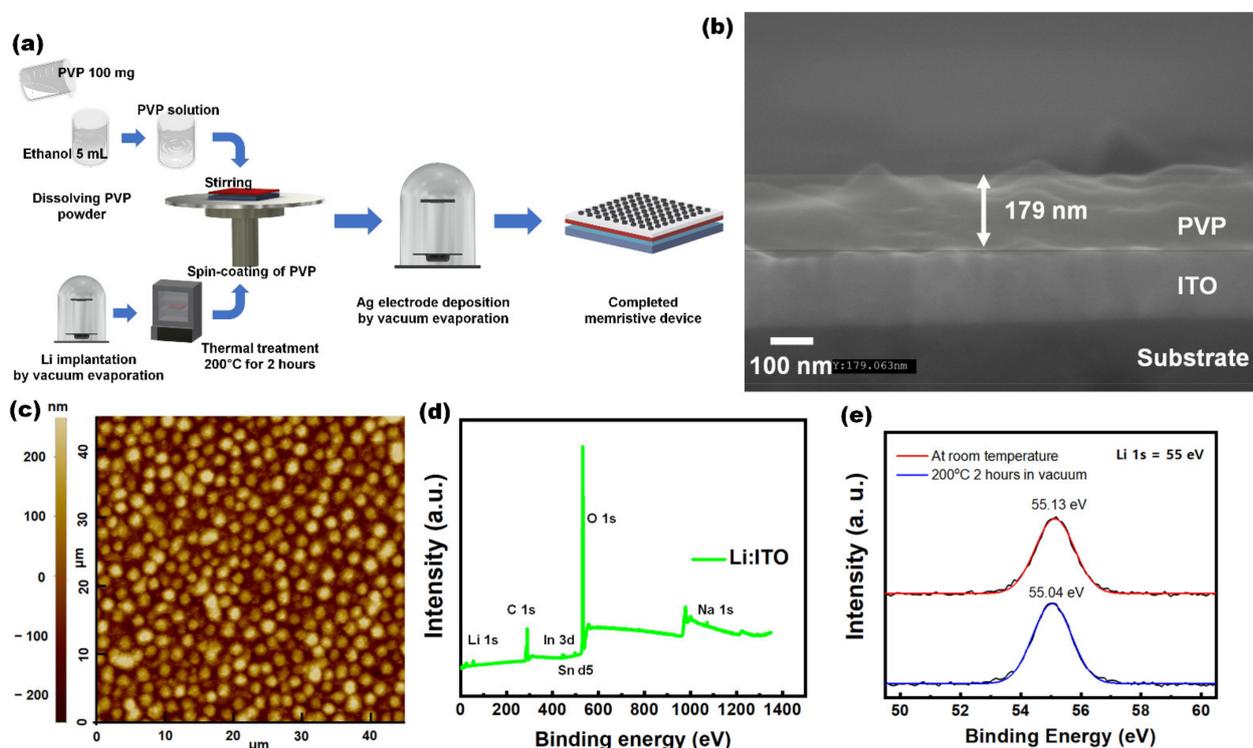


Figure 1. (a) Schematic flow chart of the fabrication process of the memristive devices implanting Li onto indium tin oxide (ITO). (b) A cross-sectional scanning electron microscopy image of polyvinylpyrrolidone (PVP, polymeric insulator) layer (highlighted) onto Li-implanted ITO. (c) Atomic force microscopy image of the Li:ITO’s surface. (d) X-ray photoelectron spectroscopy (XPS) spectra of Li-implanted ITO after that was annealed at 200°C for 2 h and the corresponding regions over the binding energy were marked. (e) The XPS peak corresponding to Li 1s of an Li-implanted ITO sample compared to that without a vacuum thermal treatment (reference peak of Li 1s: 55 eV).

The hysteresis loop of the memristive device based on a MIM structure with Li-implantation was clearly observed over a sweeping voltage from -2 V to 2 V, otherwise the hysteresis loop of the memristive devices without the Li-implantation process collapsed as shown in Figure 2a and its insert. The endurance of the memristive devices for 50 cycles was obtained to present their stability, but the on/off window slightly decreased during the cyclic operation, which infers that the current of the memristive device slightly improved due to the ionic drift by the Li element as the voltage was applied during the cycle. After that, the I–V sweep measurements were conducted (i.e., -1 V \rightarrow 0 V \rightarrow $+1.0$ V \rightarrow 0 V \rightarrow -1.0 V \rightarrow 0 V), and the memristive device showed a typical asymmetric resistance-switching behavior as shown in Figure 2b. From the initial voltage -1 to 1 V, the current gradually decreased and increased following the applied voltages, respectively. When the applied voltage reached approximately 1 V, the current suddenly increased from the HRS to a low-resistive state (LRS), which is called the SET process. The stable resistive-switching operation was possible with a large R_{ON}/R_{OFF} ratio of 4.61×10^3 . In the I–V sweep in the negative voltage, the current gradually increased when the voltage reached -1 V and decreased to 0 V, which is a typical property for “write once read many” (WORM) devices. WORM devices can be explained as data storage devices memorizing information in a set process and which are not removed during operations; they nearly match the functionality of human LTM behavior. However, the device with a SET state during a I–V sweep between -1 V and 1 V could possibly switch to the RESET state according to the bipolar I–V characteristics with a sweep mode from -2 to 2 V.

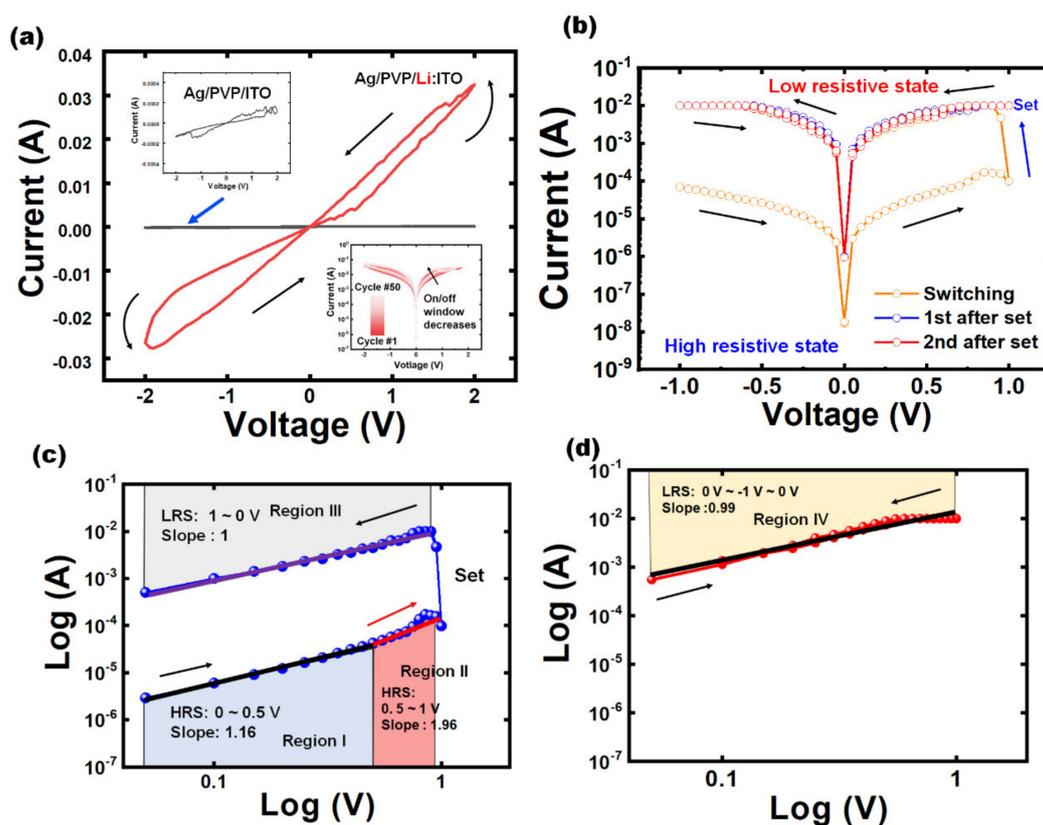


Figure 2. (a) The bipolar current–voltage (I–V) characteristics when a sweep mode bias is applied voltage from -2 to 2 V of an Ag/PVP/Li:ITO memristive device. The endurance of bipolar I–V for 50 cycles is presented in the insert. (b) I–V characteristics when a sweep mode bias is applied as voltage in the range from -1 to 1 V of an Ag/PVP/Li:ITO memristive device. I–V fitting curves on a log–log scale to illustrate the carrier transport mechanisms for a high-resistive state (HRS) with a set process and low-resistive state (LRS) (c) in the positive voltages and (d) the negative voltages (ohmic: $J \propto V$ and SCLC: $I \propto V^{1.96}$).

The I–V fitting data of the conduction mechanisms for the electron transportation models were plotted in log–log scales in Figure 2c,d. Briefly, four regions (i.e., I, II, III, and IV) were identified as the ohmic conduction (OC) and the Mott Gurney law (space charge limited current, SCLC) as follows:

$$J_{OC} = qn\mu\varepsilon \frac{V}{d} \quad (1)$$

$$J_{SCLC} = \frac{9}{8} \varepsilon \mu \frac{V^2}{d^3} \quad (2)$$

where q , μ , ε , n , d , and V represent the electronic charge, carrier mobility, permittivity of the active layer, density of carrier, distance separating the cathode and the anode, and voltages, respectively. As for region I, from 0 to 0.5 V, I–V was mainly fitted by Equation (1) as the current data on a natural log scale to a new linear relation $J \propto V^{1.16}$. When the forward bias was applied to the device, the components of the Li and Ag atoms were ionized into Li^+ and Ag^+ ions at the electrodes and stored on the ITO that supplied electrons due to the current flow. Subsequently, the ions accumulated to form a CF, and the electrons were limited by the incomplete CF (region II), which presented $J \propto V^{1.96}$ indicating that SCLC model of Equation (2) in the 0.5–1 V range. When the applied voltage reached the SET voltage in the positive voltage region, the CF was completely formed between the two electrodes following the ideal OC of $J \propto V$ (region III). Equally, when a reverse bias was applied, the CF was already formed by the enriched ions of Li^+ and Ag^+ , and the resistance state maintained the LRS in which the current was proportional to the OC model as $I \propto V^{0.99}$.

Figure 3a,b show the I–V curves and the variation in the conductance of the memristive device during seven consecutive positive and negative dual sweeps ($0 \text{ V} \rightarrow +1 \text{ V} \rightarrow -1 \text{ V} \rightarrow 0 \text{ V}$) and with a compliance current of 0.01 A, respectively. At the beginning of the cyclic voltage sweeping, the resistive state of the memristive device was in HRS and that resistive state was switched after three consecutive dual sweeps as conductive filament had formed (HRS \rightarrow LRS). The conductance of the memristive device dramatically increased from 0.00017 S to 0.012 S; therefore, the conductance continually improved following a voltage sweep (0.012 S \rightarrow 0.0153 S). In Figure 3c, an HRS to LRS transition was also observed in the retention test with a readout voltage of 0.05 V after 100 s from the beginning under HRS. No significant changes after the transition from HRS to LRS was seen over 3500 s (an hour). Our device had an excellent retention time in the LRS, but the HRS was unstable. In particular, a gradual increment in the conductance after the set process (LRS) was observed, because the CF was influenced to expand by the Li^+ and Ag^+ (Figure 3d). As the current value was evaluated in Figure 2a, only Ag^+ was impractical for construction of the conductive filament with the low potential stimulus, but Li^+ strongly changed the conductive path in the PVP polymeric matrix. For brain mimicking devices, these electrical characteristics are considerable because of the similarity of the methods expressing the conductance of the synapse, which is the delivery mechanism underlying synaptic plasticity related to learning and memory.

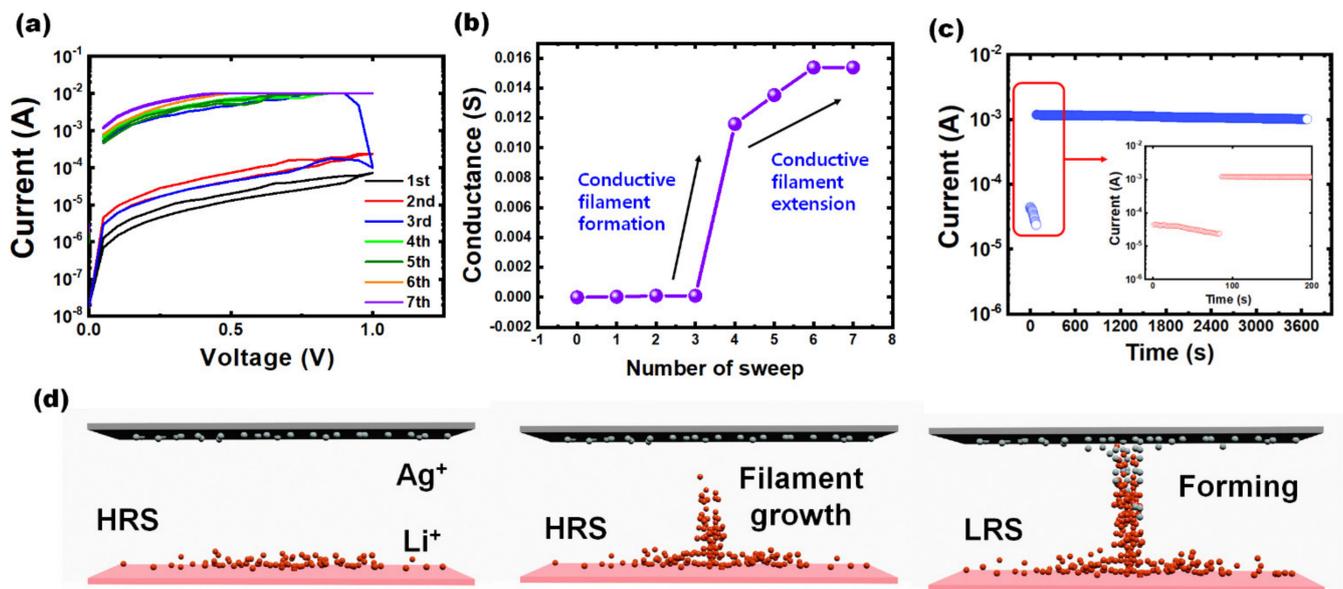


Figure 3. (a) Current–voltage (I – V) curves of the device during seven consecutive positive and negative dual sweeps ($0\text{ V} \rightarrow +1\text{ V} \rightarrow -1\text{ V} \rightarrow 0\text{ V}$) with a compliance current of 0.01 A . (b) The conductance I – V curves following seven consecutive positive and negative dual sweeps ($0\text{ V} \rightarrow +1\text{ V} \rightarrow -1\text{ V} \rightarrow 0\text{ V}$). (c) The retention time for an hour with an interval time of 1 s with a readout voltage of 0.05 V . (d) Schematic diagram of the resistive switching process.

In the conscious system of a human, the brain reacts to external stimuli through “learning or training” and reconstructs them through “remembering or memorizing”. The process in the brain establishes memory, which is divided into two types: STM and LTM as shown in Figure 4a. Basically, STM is periodically from memory lasting a few seconds, otherwise LTM is for several hours or longer. For realization of a human brain’s learning and memory algorithm, we demonstrated a transition from STM to LTM of the memristive device based on a pulse operating as shown Figure 4b,d. A programming pulse of 1 V at $1\text{ }\mu\text{s}$, including 10 read pulses of 0.01 V at $1\text{ }\mu\text{s}$, was applied. The current steadily increased after a pulse was applied, and then the current rapidly decreased as the CF spontaneously ruptured, and the current level of the memristive device remained mimicking STM. However, according to the repeatedly applied pulse voltage, the duration time of the memristive device gradually decreased as shown in Figure 4c. The reduced duration time could suggest that Li^+ and Ag^+ are progressively forming the conductive filament. Consequently, the current dramatically increased and nearly reached $10\text{ }\mu\text{A}$ after the seven pulses were applied, which were strong enough to generate numerous Li^+ and Ag^+ ions and expanded filaments to restrain the spontaneous rupture of the filaments. The STM-to-LTM transition occurred at 70 pJ with very low power consumption during an event, which was calculated by $P/\Delta t$, $P = V \cdot I$, and $\Delta t =$ period of seven pulses [31,32]. The programming power consumption is remarkable in comparison to recent research results on memristive devices based on MIM [33,34], polymer [27,35,36], and two-dimensional materials [37,38]. After the transition from STM to LTM, the current level consistently remained at half the value of the input pulse’s frequency (from 12 to 6 MHz). Under strong stimulus conditions, in Figure 4d, the current directly increased to $10\text{ }\mu\text{A}$ after 3 V was applied, and then the state steadily remained. The performance of our memristive devices were inconstant when the memristive devices operated under short periodic pulses. However, the result implies a new opportunity for the memristive device as a future neuromorphic processor that can operate with low programming power and high frequency.

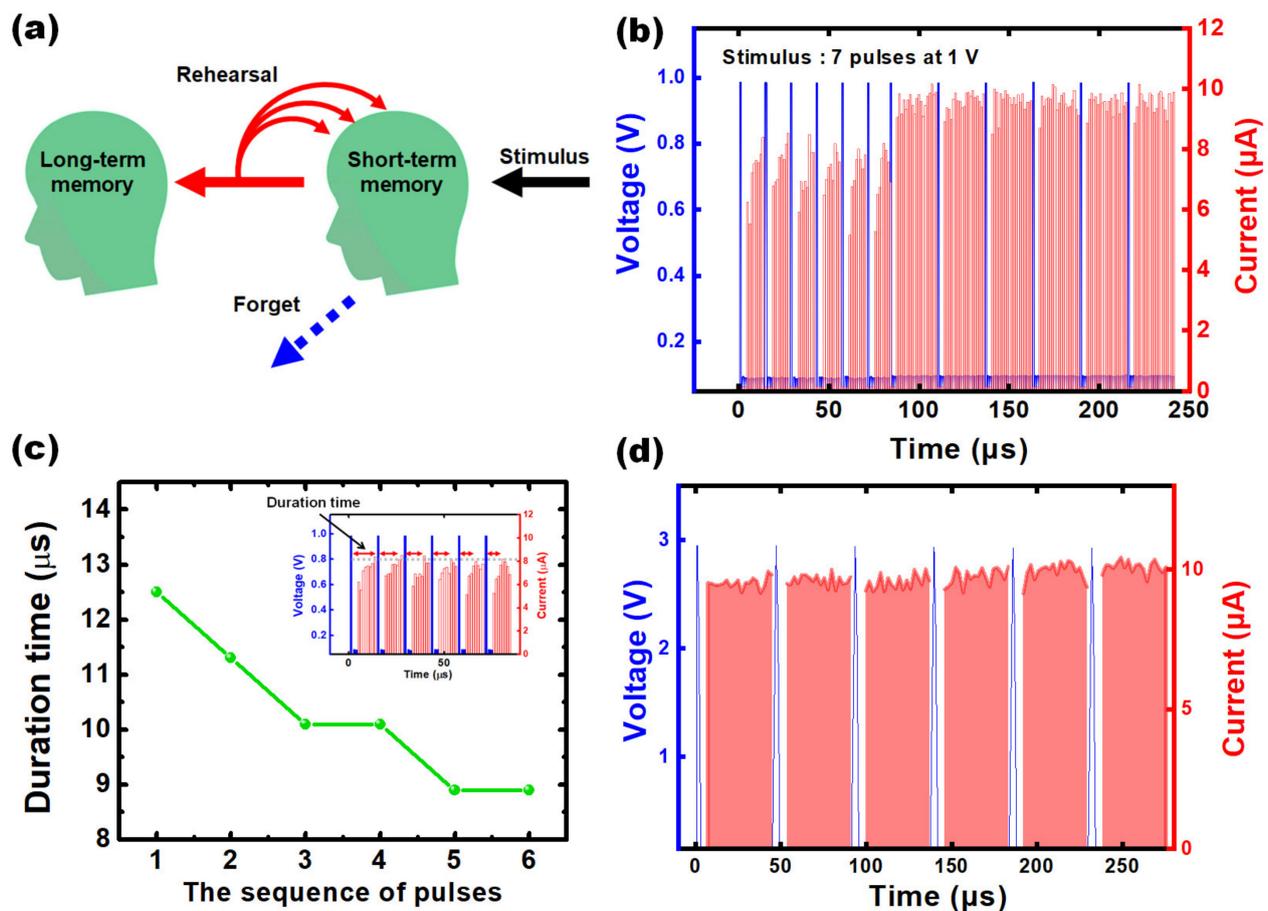


Figure 4. (a) Schematic diagram for the short-term (STM) and long-term memory (LTM) transition process through the rehearsal learning process. (b) Characteristics of the STM-to-LTM transition under an input of 7 pulses of 1 V for 1 μ s with 10 read pulses of 0.01 V for 1 μ s before the LTM transition and 1 V at 1 μ s with 20 read pulses of 0.01 V for 1 μ s after the LTM transition. (c) Duration time indicating the period that the current increased to approximately 8 μ A over the sequence number of pulses and the I–V characteristic with the input stimulus during an interval of 12 μ s (insert). (d) The property of the direct transition to LTM by a strong stimulus of 3 V for 1 μ s.

4. Conclusions

In summary, we performed human brain mimicking using memristive devices controlling STM and LTM with a low programming power consumption of 70 pJ per event. The implanted Li was defined by surface analysis based on a photoelectric effect. Since Li with low ionization energy and high ion mobility were employed, the memristive devices were able to operate only with a voltage of 1 V and a time of 1 μ s. Thus, the resistive switching mechanism of the memristive device based on Li was initially demonstrated based on the ion migrations into the polymeric insulating layer. The WORM properties of the memristive devices were studied for their I–V characteristics over the dual sweeping voltage, and the conductance changes were also observed. Furthermore, we showed that the low power memristive devices exhibited the fundamentals of next generation neuromorphic systems, i.e., learning and memory. We believe that these results are of vital importance for further research.

Author Contributions: Conceptualization, Y.P.J., Y.B., Y.J.Y. and S.Y.P.; methodology, Y.P.J., Y.B., H.J.L., Y.J.Y. and S.Y.P.; software, Y.P.J.; validation, S.Y.P.; formal analysis, Y.P.J., Y.B., H.J.L. and E.J.L.; investigation, Y.P.J.; resources, Y.J.Y. and S.Y.P.; data curation, Y.P.J.; writing—original draft preparation, Y.P.J. and Y.B.; writing—review and editing, Y.P.J., Y.B., Y.J.Y., E.J.L. and S.Y.P.; visualization, Y.P.J., H.J.L. and E.J.L.; supervision, Y.J.Y. and S.Y.P.; project administration, S.Y.P.; funding acquisition, S.Y.P. All authors have read and agreed to the published version of the manuscript.

Funding: This research received no external funding.

Data Availability Statement: The data that support the findings of this study are available from the corresponding author upon reasonable request.

Acknowledgments: This research was supported by the National Research Foundation of Korea (NRF) with a grant funded by the Ministry of Science and ICT (MSIT, No. 2018M3A7B4070990 and 2020R1A2C2103137) and by the Basic Science Research Program through the NRF with a grant funded by the Ministry of Education (No. 2020R1F1A1076359).

Conflicts of Interest: The authors declare no conflict of interest.

References

1. Von Neumann, J. *The Computer and the Brain*; Yale University: New Haven, CT, USA, 2012.
2. Jaiswal, A.; Charkraborty, I.; Agrawal, A.; Roy, K. 8T SRAM cell as a multibit dot-product engine for beyond Von Neumann computing. *IEEE Tran. VLSI Syst.* **2019**, *27*, 2556–2567. [[CrossRef](#)]
3. Zanotti, T.; Puglisi, F.M.; Pavan, P. Smart logic-in-memory architecture for low-power non-von neumann computing. *IEEE J. Electron Devices Soc.* **2020**, *8*, 757–764. [[CrossRef](#)]
4. Yao, P.; Wu, H.; Gao, B.; Tang, J.; Zhang, Q.; Zhang, W.; Yang, J.J.; Qian, H. Fully hardware-implemented memristor convolutional neural network. *Nature* **2020**, *577*, 641–646. [[CrossRef](#)] [[PubMed](#)]
5. Li, C.; Hu, M.; Li, Y.; Jiang, H.; Ge, N.; Montgomery, E.; Zhang, J.; Song, W.; Dávila, N.; Graves, C.E.; et al. Analogue signal and image processing with large memristor crossbars. *Nat. Electron.* **2018**, *1*, 52–59. [[CrossRef](#)]
6. Li, P.; Li, C.; Wang, Z.; Li, Y.; Juian, H.; Song, W.; Rao, M.; Zhuo, Y.; Upadhyay, N.K.; Barnell, M.; et al. Three-dimensional memristor circuits as complex neural networks. *Nat. Electron.* **2020**, *3*, 225–232. [[CrossRef](#)] [[PubMed](#)]
7. Yoon, J.H.; Wang, Z.; Kim, K.M.; Wu, H.; Ravichandran, V.; Xia, Q.; Hwang, C.S.; Yang, J.J. An artificial nociceptor based on a diffusive memristor. *Nat. Commun.* **2018**, *9*, 417. [[CrossRef](#)] [[PubMed](#)]
8. Pérez, E.; Pérez-Ávila, A.J.; Romero-Zalaz, R.; Mahadevaiah, M.K.; Quesada, E.P.B.; Roldán, J.B.; Molinos, F.J.; Wenger, C. Optimization of Multi-Level Operation in RRAM Arrays for In-Memory Computing. *Electronics* **2021**, *10*, 1084. [[CrossRef](#)]
9. Roy, K.; Jaiswal, A.; Panda, P. Towards spike-based machine intelligence with neuromorphic computing. *Nature* **2019**, *575*, 607–617. [[CrossRef](#)] [[PubMed](#)]
10. Shastri, B.J.; Tait, A.N.; Ferreira de Lima, T.; Pernice, W.H.; Bhaskaran, H.; Wright, C.D.; Prucnal, P.R. Photonics for artificial intelligence and neuromorphic computing. *Nat. Photonics* **2021**, *15*, 102–114. [[CrossRef](#)]
11. van De Burgt, Y.; Melianas, A.; Keene, S.T.; Malliaras, G.; Salleo, A. Organic electronics for neuromorphic computing. *Nat. Electron.* **2018**, *1*, 386–397. [[CrossRef](#)]
12. Anzueto-Ríos, Á.; Gómez-Castañeda, F.; Flores-Nava, L.M.; Moreno-Cadenas, J.A. Approaching Optimal Nonlinear Dimensionality Reduction by a Spiking Neural Network. *Electronics* **2021**, *10*, 1679. [[CrossRef](#)]
13. Lv, Z.; Wang, Y.; Chen, J.; Wang, J.; Zhou, Y.; Han, S.T. Semiconductor quantum dots for memories and neuromorphic computing systems. *Chem. Rev.* **2020**, *120*, 3941–4006. [[CrossRef](#)]
14. Wang, H.; Zhao, Q.; Ni, Z.; Li, Q.; Liu, H.; Yang, Y.; Wang, L.; Ran, Y.; Guo, Y.; Hu, W.; et al. A ferroelectric/electrochemical modulated organic synapse for ultraflexible, artificial visual-perception system. *Adv. Mater.* **2018**, *30*, 1803961. [[CrossRef](#)]
15. Kwon, K.C.; Zhang, Y.; Wang, L.; Yu, W.; Wang, X.; Park, I.H.; Choi, H.S.; Ma, T.; Zhu, Z.; Tian, B.; et al. In-plane ferroelectric tin monosulfide and its application in a ferroelectric analog synaptic device. *ACS Nano* **2020**, *14*, 7628–7638. [[CrossRef](#)] [[PubMed](#)]
16. Fukami, S.; Ohno, H. Perspective: Spintronic synapse for artificial neural network. *J. Appl. Phys.* **2018**, *124*, 151904. [[CrossRef](#)]
17. Copley, R.A.; Hayat, H.; Wright, C.D. A self-resetting spiking phase-change neuron. *Nanotechnology* **2018**, *29*, 195202. [[CrossRef](#)]
18. La Barbera, S.; Ly, D.R.; Navarro, G.; Castellani, N.; Cueto, O.; Bourgeois, G.; De Salvo, B.; Nowak, E.; Queriloz, D.; Vianello, E. Narrow Heater Bottom Electrode-Based Phase Change Memory as a Bidirectional Artificial Synapse. *Adv. Electron. Mater.* **2018**, *4*, 1800223. [[CrossRef](#)]
19. Zhao, Y.Y.; Sun, W.J.; Wang, J.; He, J.H.; Li, H.; Xu, Q.F.; Li, N.J.; Chen, D.Y.; Lu, J.M. All-Inorganic Ionic Polymer-Based Memristor for High-Performance and Flexible Artificial Synapse. *Adv. Func. Mater.* **2020**, *30*, 2004245. [[CrossRef](#)]
20. Kim, D.; Lee, J.S. Designing artificial sodium ion reservoirs to emulate biological synapses. *NPG Asia Mater.* **2020**, *12*, 62. [[CrossRef](#)]
21. Bae, J.; Kobayashi, N.P. Resistive switching device with highly-asymmetric current voltage characteristics: Its error analysis and new design parameter. *Semicond. Sci. Technol.* **2019**, *34*, 025007. [[CrossRef](#)]
22. Khan, M.U.; Hassan, G.; Bae, J. Non-volatile resistive switching based on zirconium dioxide:poly(4-vinylphenol) nano-composite. *Appl. Phys. A* **2019**, *125*, 378. [[CrossRef](#)]
23. Sun, W.; Gao, B.; Chi, M.; Xia, Q.; Yang, J.J.; Qian, H.; Wu, H. Understanding memristive switching via in situ characterization and device modeling. *Nat. Commun.* **2019**, *10*, 3453. [[CrossRef](#)]
24. Yan, X.; Zhao, Q.; Chen, A.P.; Zhao, J.; Zhou, Z.; Wang, J.; Wang, H.; Zhang, L.; Li, X.; Xiao, Z.; et al. Vacancy-Induced Synaptic Behavior in 2D WS₂ Nanosheet-Based Memristor for Low-Power Neuromorphic Computing. *Small* **2019**, *15*, 1901423. [[CrossRef](#)]

25. Yang, Y.; Zhang, X.; Qin, L.; Zeng, Q.; Qiu, X.; Huang, R. Probing nanoscale oxygen ion motion in memristive systems. *Nat. Commun.* **2017**, *8*, 15173. [[CrossRef](#)]
26. Lee, G.; Baek, J.-H.; Ren, F.; Pearton, S.J.; Lee, G.-H.; Kim, J. Artificial neuron and synapse devices based on 2D materials. *Small* **2021**, *17*, 2100640. [[CrossRef](#)]
27. Kim, M.K.; Lee, J.S. Short-term plasticity and long-term potentiation in artificial biosynapses with diffusive dynamics. *ACS Nano* **2018**, *12*, 1680–1687. [[CrossRef](#)] [[PubMed](#)]
28. Chang, Y.C.; Lu, Y.C.; Hung, Y.J. Controlling the nanoscale gaps on silver Island film for efficient surface-enhanced Raman spectroscopy. *Nanomaterials* **2019**, *9*, 470. [[CrossRef](#)] [[PubMed](#)]
29. Yao, K.P.; Kwabi, D.G.; Quinlan, R.A.; Mansour, A.N.; Grimaud, A.; Lee, Y.L.; Lu, Y.C.; Shao-Horn, Y. Thermal stability of Li₂O₂ and Li₂O for Li-air batteries: In situ XRD and XPS studies. *J. Electrochem. Soc.* **2013**, *160*, A824. [[CrossRef](#)]
30. Wood, K.N.; Teeter, G. XPS on Li-battery-related compounds: Analysis of inorganic SEI phases and a methodology for charge correction. *ACS Appl. Energy Mater.* **2018**, *1*, 4493–4504. [[CrossRef](#)]
31. Wang, K.; Li, L.; Zhao, R.; Zhao, J.; Zhou, Z.; Wang, J.; Wang, H.; Tang, B.; Lu, C.; Lou, J.; et al. A Pure 2H-MoS₂ Nanosheet-Based Memristor with Low Power Consumption and Linear Multilevel Storage for Artificial Synapse Emulator. *Adv. Electron. Mater.* **2020**, *6*, 1901342. [[CrossRef](#)]
32. Wu, C.; Kim, T.W.; Choi, H.Y.; Strukov, D.B.; Yang, J.J. Flexible three-dimensional artificial synapse networks with correlated learning and trainable memory capability. *Nat. Commun.* **2017**, *8*, 752. [[CrossRef](#)] [[PubMed](#)]
33. Lin, C.Y.; Chen, J.; Chen, P.H.; Chang, T.C.; Wu, Y.; Eshraghian, J.K.; John, M.; Yoo, S.M.; Wang, Y.-H.; Chen, W.-C.; et al. Adaptive synaptic memory via lithium ion modulation in RRAM devices. *Small* **2020**, *16*, 2003964. [[CrossRef](#)] [[PubMed](#)]
34. Lian, X.; Shen, X.; Fu, J.; Gao, Z.; Wan, X.; Liu, X.; Hu, E.; Xu, J.; Tong, Y. Electrical Properties and Biological Synaptic Simulation of Ag/MXene/SiO₂/Pt RRAM Devices. *Electronics* **2020**, *9*, 2098. [[CrossRef](#)]
35. Jeon, Y.J.; An, H.; Kim, Y.J.; Jeon, Y.P.; Kim, T.W. Highly reliable memristive devices with synaptic behavior via facilitating ion transport of the zeolitic imidazolate framework-8 embedded into a polyvinylpyrrolidone polymer matrix. *Appl. Sur. Sci.* **2021**, *567*, 150748. [[CrossRef](#)]
36. Chen, Y.; Liu, G.; Wang, C.; Zhang, W.; Li, R.-W.; Wang, L. Polymer memristor for information storage and neuromorphic applications. *Mater. Horiz.* **2014**, *1*, 489–506. [[CrossRef](#)]
37. Mostafa, H.; Khat, A.; Serb, A.; Mayr, C.G.; Indiveri, G.; Prodromakis, T. Implementation of a spike-based perceptron learning rule using TiO₂-x memristors. *Front. Neurosci.* **2015**, *9*, 357. [[CrossRef](#)] [[PubMed](#)]
38. Yan, X.; Qin, C.; Lu, C.; Zhao, J.; Zhao, R.; Ren, D.; Li, H. Robust Ag/ZrO₂/WS₂/Pt memristor for neuromorphic computing. *ACS Appl. Mater. Interfaces* **2019**, *11*, 48029–48038. [[CrossRef](#)]