

Article

A Novel Fundamental Frequency Switching Operation for Conventional VSI to Enable Single-Stage High-Gain Boost Inversion with ANN Tuned QWS Controller

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Abstract: Single-stage high-gain inverters have recently gained much research focus as interfaces for inherent low voltage DC sources such as fuel cells, storage batteries, and solar panels. Many impedance-assisted inverters with different input stage configurations have been presented. To decrease passive component sizes, these inverters operate at high-frequency switching. The high-frequency switching optimizes the passive component sizes but introduces many challenges in the form of high-frequency inductor design, control complexity, high-frequency gate driver requirements, high semiconductor losses, and electromagnetic interferences. This article proposes a novel fundamental frequency switching operation for the conventional voltage source inverters (VSI) to operate as a single-stage high-gain inverter. As the novel operational strategy changes the behavior of conventional VSI from buck inverter to a boost inverter, it is hereafter termed as a novel inverter. By virtue of the operation strategy, switches withstand peak inverse voltage (PIV) equal to DC link voltage, unlike other impedance assisted boost inverters where PIV across switches is the amplified DC voltage. The proposed inverter can invert low-level DC voltage to high voltage AC with low total harmonic distortion (THD) in a single stage without the help of any external filter. A novel quarter-wave symmetric phase-shift controller is proposed for variable voltage and frequency control of proposed inverters tuned by a back-propagation thin-plate-spline neural network (BPTPSNN). Mathematical analysis with experimental validation is presented. Experimentation is carried out on a prototype of 2 kW for single-phase resistive load, induction motor, and non-linear loads.

Keywords: boost inverter; Class-D amplifier; peak inverse voltage; resonant power conversion; zero-current switching

1. Introduction

The limited availability of fossil fuels and increasing pollution can never fulfill the ever-increasing energy demand. It increased the thrust for renewable energy sources and allied technology to the forefront of the research arena [1]. Solar energy enjoys the prime focus among the available renewable energy sources because of its abundance and immense installation potential. The solar energy harvested by the photovoltaic (PV) panels inherently produce low voltage DC [2]. However, most electrical appliances demand AC at higher voltage levels. For this reason, inverters that convert DC to AC are essential for interfacing such renewable energy-based generators to the grid [3]. The conventional voltage source inverters (VSI) are of buck type, i.e., they produce an AC voltage level less than or equal to the available input DC link voltage. These VSIs usually employ either a step-up transformer

or a back-ended boost converter to increase the voltage levels. However, these methods increase the system's cost and complexity and compromise efficiency [4–6].

Further, current source inverters (CSIs) that are boost-type inverters have been employed with PV panels [7,8]. However, CSIs employ a high-value inductor at the DC link side, increasing overall system cost and weight. Moreover, control of such systems tends to be complicated as constant output voltage must be maintained.

An inverter mitigating the above issues with buck-boost capabilities termed impedance source inverters (ZSIs) has been proposed in [9], possessing the advantages of both VSI and CSI. Many improvised, enhanced, and modified topologies of ZSIs are presented in state-of-the-art [10–16]. However, the basic ZSI and the modified and enhanced structures provide boosted DC voltage at the interim inverting stage at the cost of passive components. This increases the component count, size, weight, and above all, the control complexity.

The passive components have been reduced by replacing the ZSI with multi-level inverters (MLIs) [17–22]. Further, a few state-of-the-art structures employ switched-capacitor inverters to boost low-level DC to high voltage AC in a single stage [22–25]. However, these inverters provide boosting, proportional to the number of semiconductors employed, i.e., more switches are employed to generate a higher level of AC voltage. This increases the semiconductor losses, thereby decreasing the efficiency, and the more the number of semiconductor switches employed, the system's reliability decreases inversely. Moreover, the control of too many switches increases the control complexity.

Several single-stage boost inverters have been proposed [23–26]. The boost inverter proposed in [18] and further detailed in [19] delivers low total harmonic distortion (THD) double boosted output voltage. However, the two synchronously operating boost converters should operate with a phase shift of 180° to provide doubly boosted sinusoidal output to the differentially connected load. The boost inverter discussed in [25] uses coupled inductors for boosting the voltage levels. However, this employs many inductors, which increases the size and cost of the converter. Another boost inverter with common ground for PV applications has been detailed in [26], which employs an extra capacitor for boosting purposes. This reduces the reliability and efficiency of the system. As evident from literature, many inverter topologies have been investigated for a practical high-gain DC-AC conversion with allied pros and cons.

However, the real-time application of solar panels can involve single-stage or two-stage power conversion system. The PV power conversion system's task is twofold, i.e., the first is to extract maximum power from PV, and the second is to deliver to the application side with required power quality. Two-stage systems have these two controls decoupled i.e., maximum power tracking and AC side requirements, therefore, they are simple to implement but are bulky and costly. In contrast, single-stage conversion systems have complex control to address PV and AC side demands [27,28]. The focus of the article is a single-stage inversion system with high gain and simple control.

Class-D amplifiers with double pole filters (shown in Figure 1) have ruled the arena of high-efficiency audio and power amplifiers with a simple design, effortless control, high power, and reliable operation [29,30]. Its theoretical efficiency of 100% is often transformed into practical efficiencies of 95% and above in applications. Many controllers have been designed and developed for Class-D amplifiers to enhance intrinsic low THD and noise at output levels [31,32].

Its working has been based on sinusoidal pulse width modulation (SPWM) inverters. Many series and parallel resonant power converters have been investigated for heating purposes [33]. Nevertheless, high-frequency switching is used in all applications, raising electromagnetic interference (EMI) and electromagnetic compliance (EMC) issues. In the present work, the authors propose a new fundamental frequency switched single-stage high-gain quasi-resonant inverter. The topology of the proposed inverter mimics the Class-D amplifiers for single-phase applications.

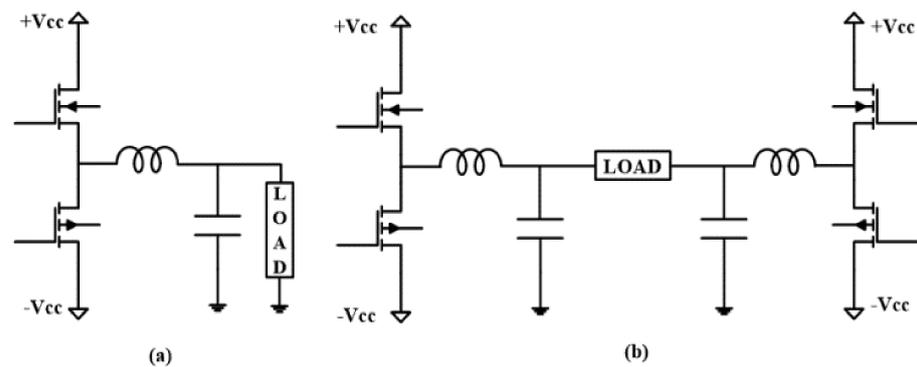


Figure 1. (a) Half-bridge and (b) full-bridge Class-D amplifier with double-pole filter.

Although the conventional H-Bridge VSI and proposed inverter structure are the same, operation-wise, it is different [34]. Conventional VSI is a buck type of inverter. However, the proposed inverter is a high-gain boost inverter. Moreover, the L and C in the conventional VSI act as a filter, but they act as voltage boosters in the proposed inverter. The proposed inverter is switched at the fundamental frequency and employs coupled resonant LC-pair to boost DC input to AC voltage with theoretically pure sinusoidal waveforms at the output. Fundamental frequency switching and lack of interim DC-link give the proposed inverter the following unique characteristics:

- Low PIV across switches;
- Low total blocking voltage (TBV) of converter, signifying minimal semiconductor loss;
- Filter-free low THD output waveform;
- Fundamental-frequency switching eliminates switching losses;
- Supports resistive, inductive as well as non-linear loads;
- Low passive component requirement.

2. Circuit Operation

The proposed circuit consists of four switches and an LC pair, tuned around the fundamental frequency of operation, and the load is connected across the capacitor, as shown in Figure 2.

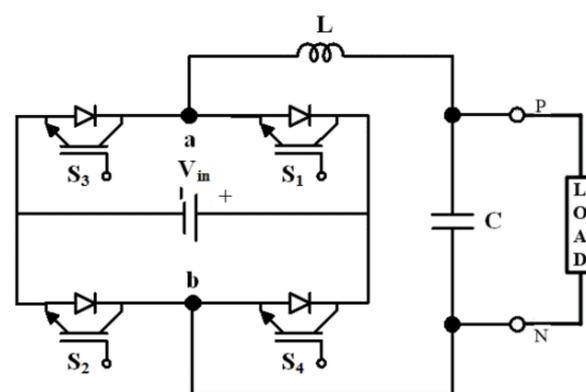


Figure 2. Circuit of proposed inverter.

Switches are operated at the fundamental frequency in a complementary fashion, i.e., while S1 and S2 are ON, S3 and S4 remain OFF and vice-versa. As the input DC source is parallel to the legs, the operation is symmetrical. Operation modes are shown in Figure 3.

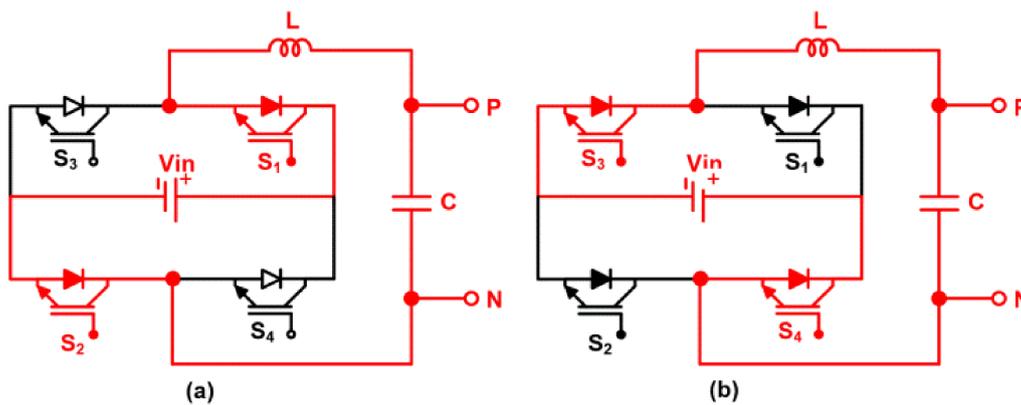


Figure 3. Modes of operation (a) S_1, S_2 in ON state and (b) S_3, S_4 in ON state.

2.1. Steady-State and Dynamic Operation

To explain the operation simply and without any loss of generality, the duty cycle is fixed at fifty percent. In its simplest form, the circuit behaves as a two-pole low pass filter during both modes of operation, as shown in Figure 4.

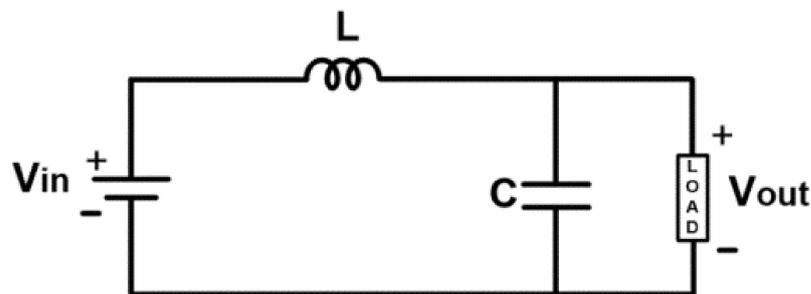


Figure 4. Equivalent circuit in its simplest form.

The transfer function for the circuit is given by:

$$G(s) = \frac{Vo(s)}{Vin(s)} = \frac{1}{1 + sL/R + s^2LC} \tag{1}$$

where L is inductance, R is load resistance, and C is the capacitance of the circuit. The resonant frequency of the system (ω_r) is:

$$\omega_r = \frac{1}{\sqrt{LC}} \tag{2}$$

Rephrasing Equation (1) in a standard second-order system by substituting ω_r from Equation (2), we obtain:

$$G(s) = \frac{Vo(s)}{Vin(s)} = \frac{\omega_r^2}{s^2 + \alpha s\omega_r + \omega_r^2} \tag{3}$$

where $\alpha = \frac{1}{R} \sqrt{\frac{L}{C}}$

Now by replacing s by $j\omega$, (3) results in the following Equation:

$$G(j\omega) = \frac{\omega_r^2}{(j\omega)^2 + (j\omega)\alpha\omega_r + \omega_r^2} \tag{4}$$

The gain of the system is given by:

$$|G(j\omega)| = \frac{1}{\sqrt{\left\{1 - \left(\frac{\omega}{\omega_r}\right)^2\right\}^2 + \alpha^2 \left(\frac{\omega}{\omega_r}\right)^2}} \quad (5)$$

At the resonant frequency, i.e., $\omega = \omega_r$ Equation (5) gives the value of gain to be $1/\alpha$, i.e.;

$$|G(j\omega)| = \frac{1}{\alpha} = R\sqrt{\frac{C}{L}} \quad (6)$$

Equation (6) provides the system's steady-state gain when the duty cycle is fixed at 0.5. The output voltage across the load is sinusoidal by tuned resonance operation across L and C . The output voltage equation across the load is given by:

$$V_o = \frac{V_{DC}}{\alpha} \text{Sin}(\omega t) \quad (7)$$

However, V_{DC} is a function of input voltage V_{in} and duty cycle " d " and is given as $V_{DC} = d \times V_{in}$, which resembles a buck converter's output voltage, which is evident from the circuit, so that Equation (7) can be rephrased in the form of (8).

$$V_o = \frac{dV_{in}}{\alpha} \text{Sin}(\omega t) \quad (8)$$

Equation (8) is the dynamic equation of the converter. Considering loss-less components, the power balance of the converter can be given by (9).

$$|V_{in} \times I_{in}| = |V_o \times I_o| \quad (9)$$

where V_{in} , I_{in} is the input voltage and current, and V_o , I_o is the output voltage and current, respectively. By substituting V_o , from Equation (8), considering maximum value of $\text{Sin}(\omega t)$ as one, relation between input and output current can be shown as:

$$|I_{in}| = |dI_o/\alpha| \quad (10)$$

Based on system equations, operational waveforms of circuit operation can be drawn, as shown in Figure 5. The maximum gain of the converter under symmetric operation is achieved at 0.5 duty cycle. For practical quadruple gain of the circuit at 1 kW load, d/α is equal to 4, i.e., $d = 0.5$ and $\alpha = 0.125$. The gain for variable load and the variable duty cycle is calculated and plotted in Figure 6.

2.2. Loss and Efficiency Calculation

From the operational waveform (see Figure 5), zero current switching of the switches can be observed; the proposed converter has no switching loss associated with it. The conduction loss of the switch (P_{SWc}) with on-time resistance (R_{CE}) is given by:

$$P_{SWc} = I_{SW}^2 R_{CE} \quad (11)$$

where I_{SW} is the collector current. As seen from Figure 5, the switch current is half sinusoid; thus, its root mean square (RMS) value is given by:

$$I_{SW} = dI_o/2\alpha \quad (12)$$

Substituting the value of switch current from Equation (12) in Equation (11), switch conduction loss is given by:

$$P_{SWc} = (dI_o/2\alpha)^2 R_{CE} \quad (13)$$

The current stress on the inductor is a sinusoidal variation with a peak value of dI_o/α . Thus, current through inductor responsible for inductor loss is given by (14), i.e.,

$$I_L = dI_o/\alpha\sqrt{2} \tag{14}$$

From (14), inductor loss (P_L) is calculated as:

$$P_L = \left(\frac{dI_o}{\alpha\sqrt{2}}\right)^2 R_L \tag{15}$$

where R_L is the DC resistance of the inductor. Another component where the loss occurs in the capacitor due to its equivalent series resistance (ESR). Current through the capacitor is given by:

$$I_C = I_L - I_O \tag{16}$$

Power loss in the capacitor (P_C), with an equivalent series resistance (ESR) is given by:

$$P_C = (I_C)^2 ESR \tag{17}$$

The efficiency of the converter is given by:

$$\eta = \frac{P_O}{P_O + Losses} = \frac{P_O}{P_O + P_C + P_L + P_{SW}} \tag{18}$$

where P_O is output power and P_C, P_L and P_{SW} are capacitor, inductor, and switch losses (as ZCS occurs, switch loss only has conduction loss component).

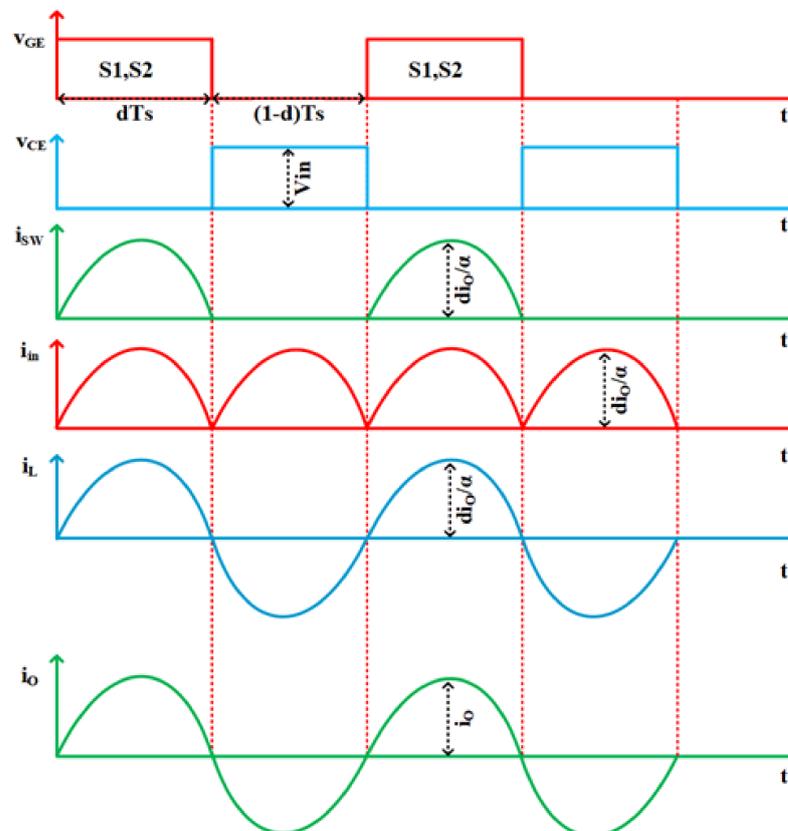


Figure 5. Operational waveforms of the proposed inverter.

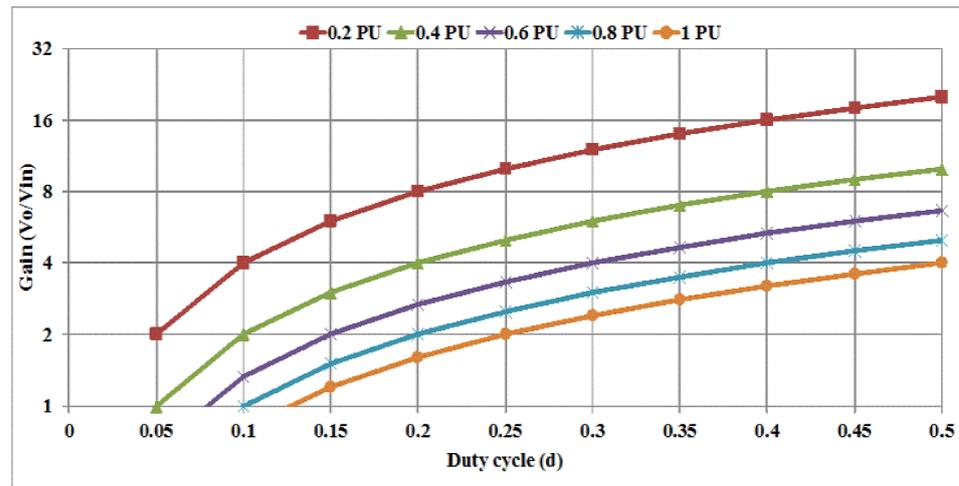


Figure 6. Gain variation with the duty cycle for fixed DC link voltage and on different loads.

Based on circuit equations, voltage and current stress across each component can be tabulated as shown in Table 1.

Table 1. Voltage and current stress.

| Component | Voltage Stress | Current Stress |
|-----------|----------------|-----------------------------|
| Switch | dV_{in} | $dI_o/2\alpha$ |
| Inductor | - | $dI_o/2\alpha$ |
| Capacitor | V_o | $I_o - dI_o/\sqrt{2\alpha}$ |

A thermal model of the proposed converter is constructed using PLECS software to verify the calculation efficiency further. The datasheet-assisted thermal model of the switch is shown in Figure 7.

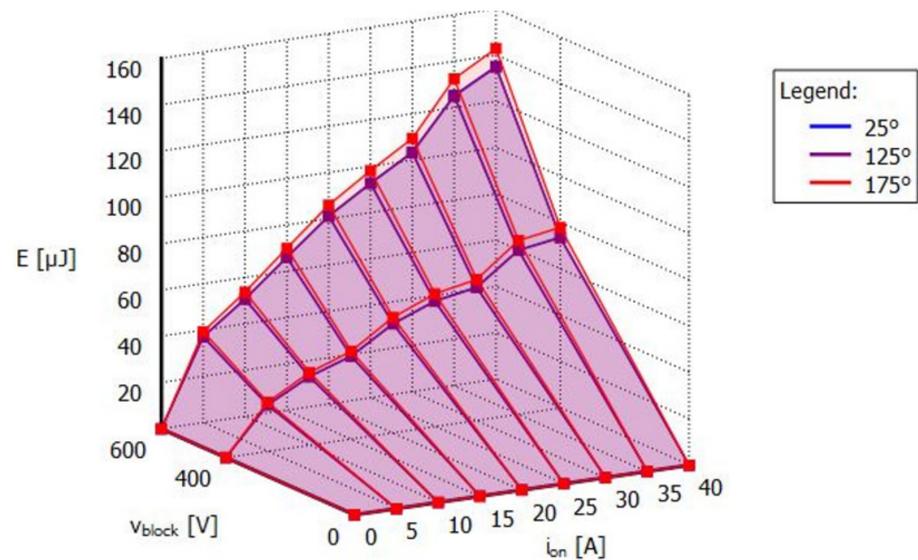


Figure 7. Cont.

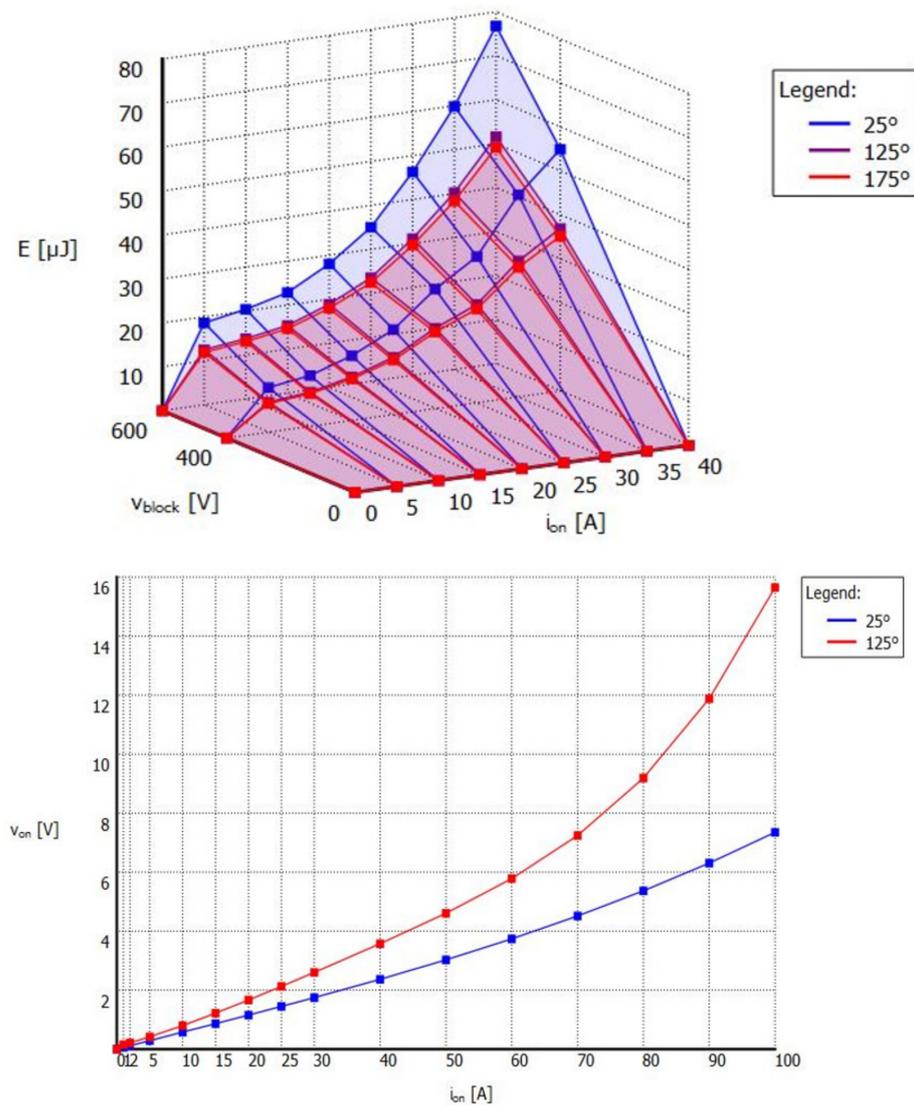


Figure 7. Turn-on energy, turn-off energy, and conduction loss variation (from top to bottom, respectively).

3. Variable Voltage Variable Frequency Controller

Single-stage single-phase boost inverters have the symmetric operation as two converters are working in tandem, so for a proper sinusoidal output waveform generation, the two converters need to be in perfect synchronism.; such converters tend to destabilize above the duty cycle of 0.5, so they are operated in the duty cycle range of 0 to 0.5 [24].

Boost inverters generally employ a sliding mode or close loop waveform controller for symmetric operation at all operation points. The sliding mode controller works only when the sliding surface and tracking equations are accurately defined. In the case of un-optimized functions, chattering is a dominant problem. Finding out the sliding surface and control law equations is a painstaking task and involves two different loops, i.e., inductor current control and capacitor voltage control [35,36] for proper wave-shape tracking, which is sinusoidal in the case of boost inverter.

A new quarter-wave symmetric (QWS) controller has been designed for variable voltage and variable frequency output control. This QWS controller is a Sin cascaded controller in which the frequency of sine wave is changed for variable fundamental frequency operation, and quarter symmetric pulse turn-on time is controlled for variable voltage gain operation. Equation (8) shows that the inverter is capable of variable gain boost factor and variable frequency operation by changing the duty cycle and switching frequency,

respectively. The block diagram of the controller is shown in Figure 8. The subsequent pulse generation is also highlighted in Figure 9.

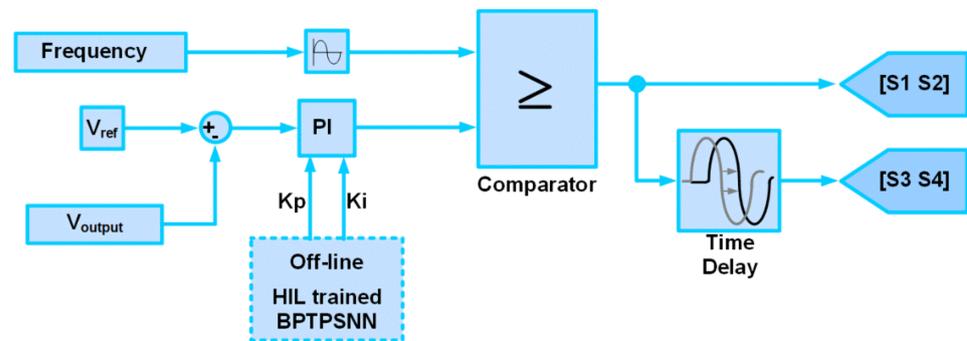


Figure 8. Functional diagram of the QWS controller.

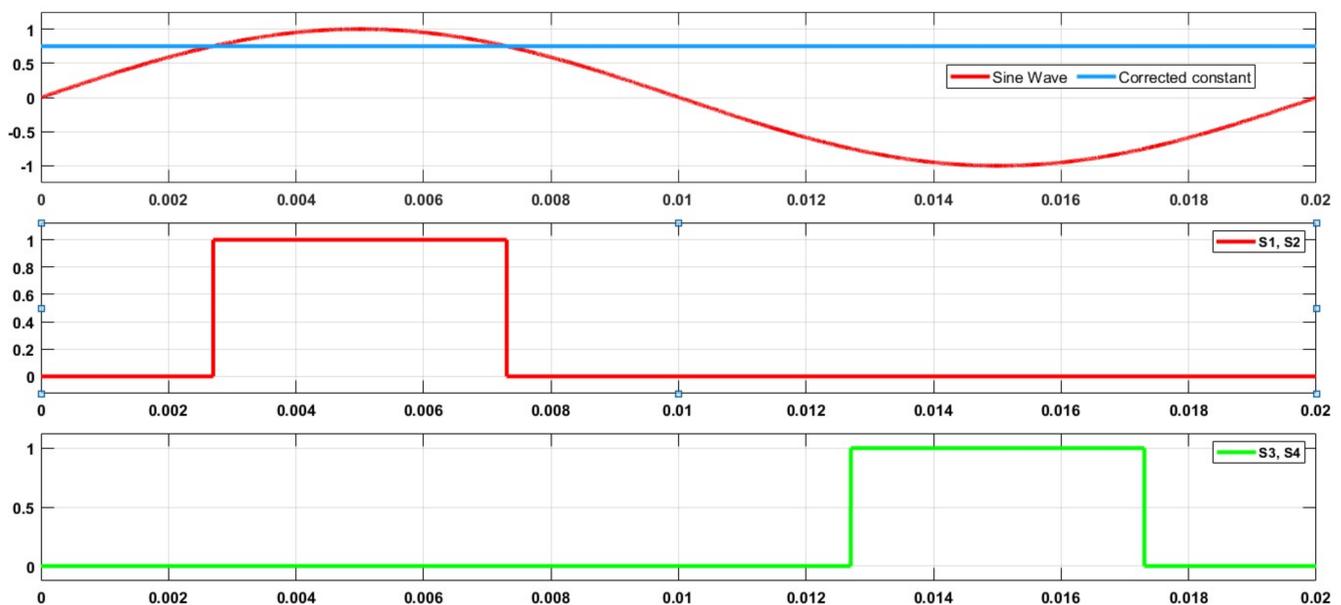


Figure 9. Phase-shifted pulse generation from the QWS controller.

QWS controller produces switching pulses, which vary in frequency and pulse width. Sine cascaded design is applied so as even when the duty cycle varies from 0 to 0.5, they are symmetric at the quarter-wave time. The governing equation for QWS is given by solution from the following simultaneous equations.

$$y_1 = \mathcal{E}(K_p + K_i/s) \tag{19}$$

$$y_2 = \sin(\omega t) \tag{20}$$

where \mathcal{E} is the error between V_{ref} and V_{output} , K_p and K_i are PI controller gains, and ω is frequency.

For realizing the PI controllers, an online-supervised learning-based artificial neural network is used. A back-propagation thin-plate-spline neural network (BTPSNN) is utilized using MATLAB *Deep Learning Toolbox*. For training the network, data are extracted by hardware in the loop setup using OP5130 OPAL-RT. Using the HIL setup, V_{output} is recorded for an input voltage sweep, input duty cycle sweep, input modulation sweeps, and input frequency sweep. Therefore, for training the network, known V_{output} is available for input frequency, voltage, and duty cycle variation.

BPTPSNN is a feed-forward back-propagation supervised learning neural network based on a thin-plate-spline transfer function [37,38]. The thin-plate-spline function in its simplest form is referred to as radial basis function represented in mathematical form as

$$y_i(n) = \sum_{j=1}^H W_{ij} f_j(u, c, \sigma) \quad (21)$$

where y_i is the output of i th neuron in the hidden layer, u is input, c is the central value, and σ is variance. W_{ij} is the weighted connection between two different layers. The control signal from the PI controller is expressed in discrete regression terms by:

$$U(k) = K_p e(k) + K_i T_i \sum_{i=1}^n e(i) \quad (22)$$

where e is the error signal, and T_i is the tunable parameters correlated to the weights and bias of the weighted connection in layers. Back-propagation is used for supervised learning as it first adjusts the weighted functions based on the neuron's activity level, and then back pass is computed based on acquired slope, which reiterates the learning rate. As shown in Figure 10, the input layer is taking the frequency sweep, input voltage sweeps, and duty-cycle perturbation data. This layer computes the maxima and minima range of K_p and K_i values, and the hidden layer optimizes the K_p and K_i values based on readjusted weights and bias, which is transferred to the output layer as optimized gain parameters [38,39]. These PI gain values K_p and K_i are used in real-time implementation of the QWS controller. The K_p and K_i values are saved in the internal registers of the TMS320F28379D for performing the control operation based on voltage feedback and reference requirements.

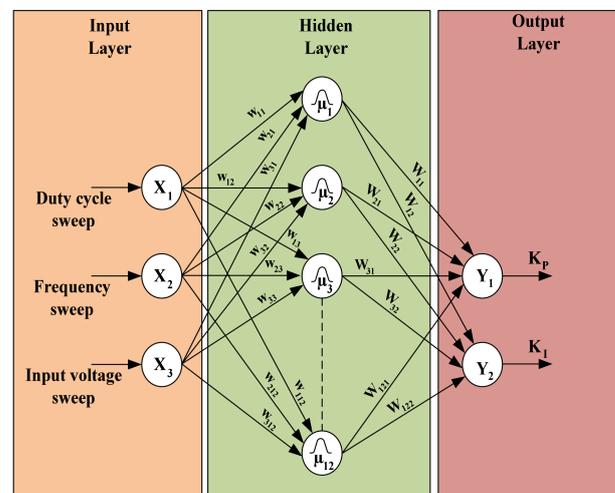


Figure 10. Layers and weighted connection of proposed BPTPSNN.

4. Experimental Validation

Experimentation was performed with 2 kW load capability on Semikron open-source inverter module with in-built gate driver and protection circuitry to demonstrate the control system's effectiveness and the circuit's capability. LEM DVL-1500 voltage sensor is used for feedback, and the DSP TI TMS320F28379D is used for pulse generation. The experimental setup is shown in Figure 11.

The data recorded in a Chauvin Arnoux power quality analyzer are shown in Figure 12. It can be seen that without any external filter, the inverter can be seamlessly switched from 50 Hz to 60 Hz operation and vice-versa. Unity power factor is maintained as expected from a resistive load in both the operation modes. The voltage and current harmonics for UPF load variation from 200 to 2000 watts is shown in Figure 13. It can be seen that the harmonics at all load levels are well below prescribed THD limits of 5% by IEEE STD-519 [40].

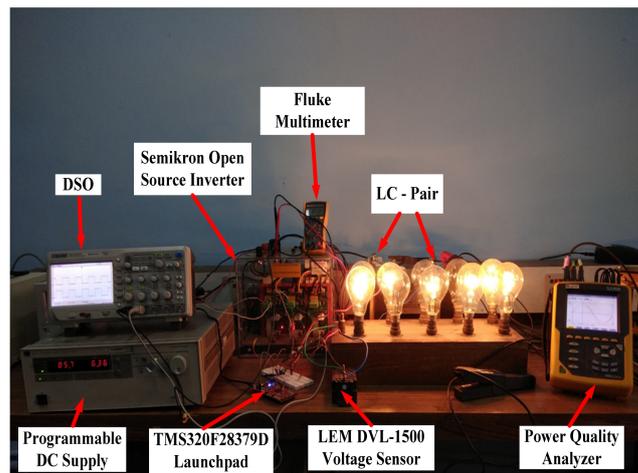


Figure 11. Experimental setup.

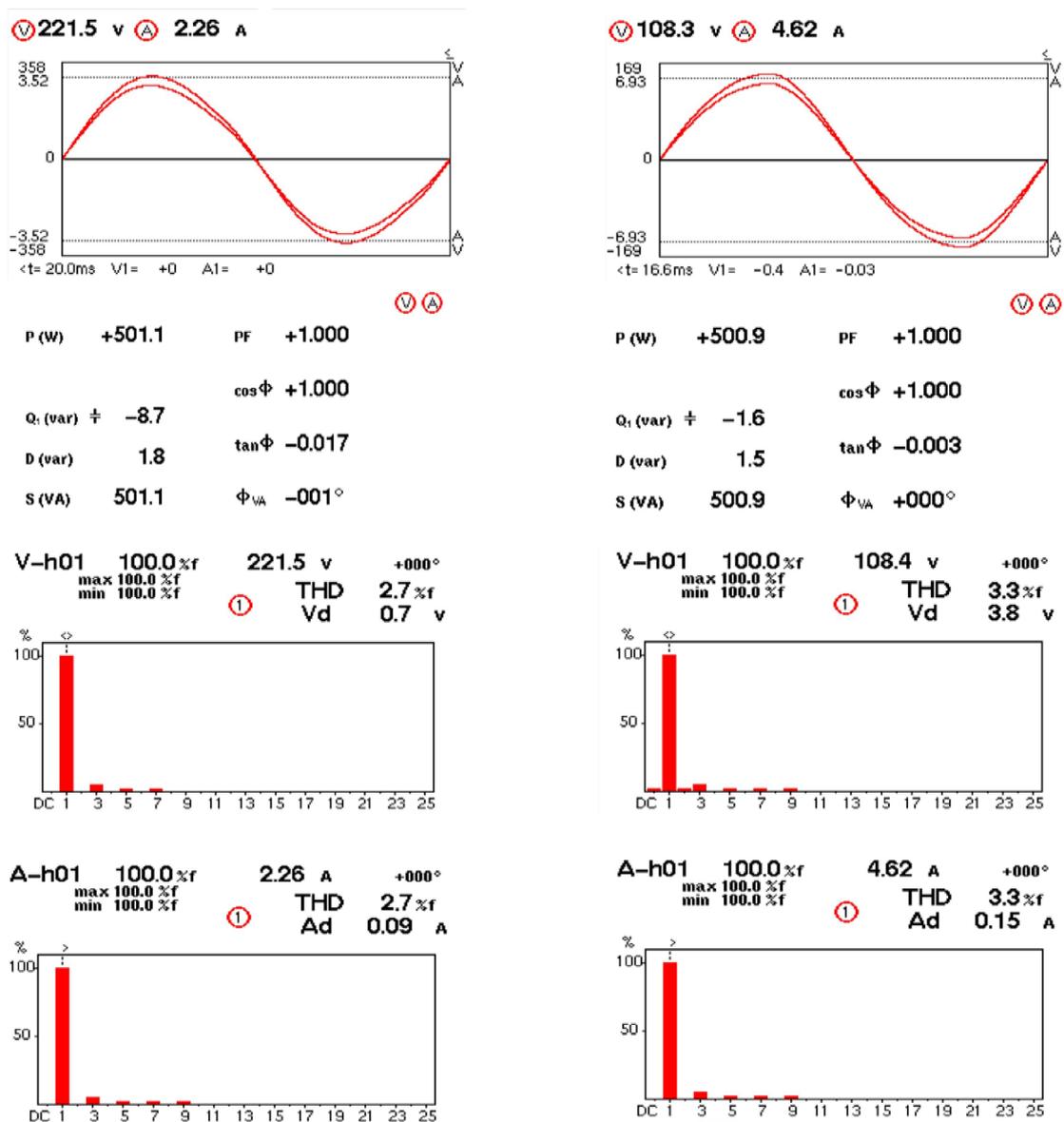


Figure 12. (Top to bottom) output voltage and current waveform, power and PF, voltage THD, and current THD, respectively. Left for 50Hz operation, right for 60 Hz operation.

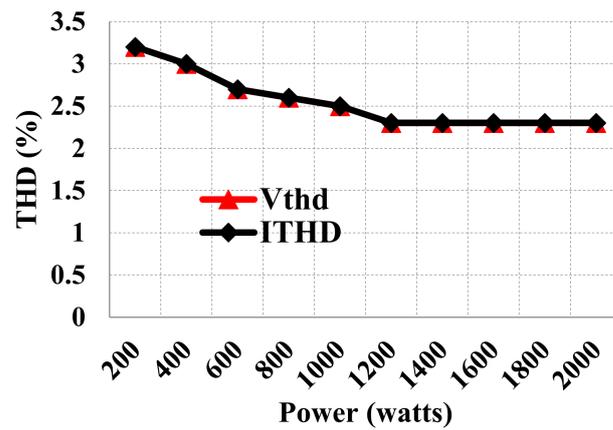


Figure 13. THD at various UPF load levels.

Harmonics present in output voltage and current for different RL loads are reported in Figure 14. These results also conform to the standard requirement of THD limits from a DC/AC inversion system.

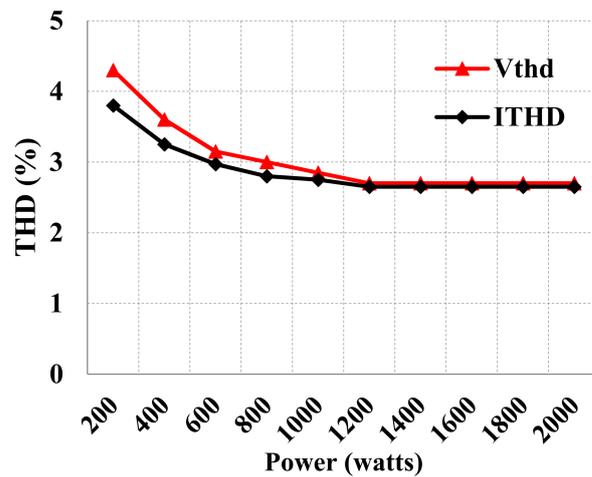


Figure 14. Voltage and current harmonics at various RL load.

The efficiency of the proposed inverter for both resistive and inductive loads is reported in Figure 15. The efficiency of the proposed converter is low at lower loads and increases to an effective value of 97% near full load.

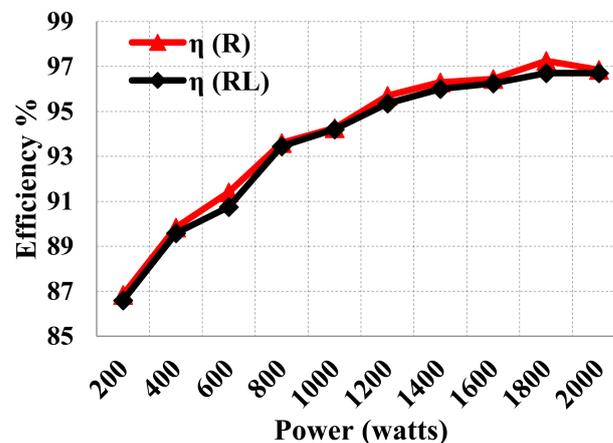


Figure 15. Experimental power conversion efficacy of inverter.

To validate the controller operation, a pulsed reference is applied as V_{ref} , which changes from 230 V to 150 V and then to 230 V, as shown in Figure 16a; it can be seen that V_{rms} follows V_{ref} faithfully with settling times less than three cycles. The quarter-wave symmetric controller operation for variable voltage and frequency control is validated by switching the output voltage and frequency from 230 V@50 Hz operation to 110 V@60 Hz operation, as shown in Figure 16b. This step-change is introduced with the DC input voltage of 85 volts, showing the controller's ability to effectively change the output voltage, frequency, and associated gains. For 230 V@50 Hz operation at 85 V, DC input gain is 3.82, while for the 110 V@60 Hz operation, the gain is 1.83. It can be observed that the steady-state has been achieved after step change has been applied within two cycles. Further, the proposed inverter is subjected to a step load of 1 kW from no-load and is illustrated in Figure 16c.

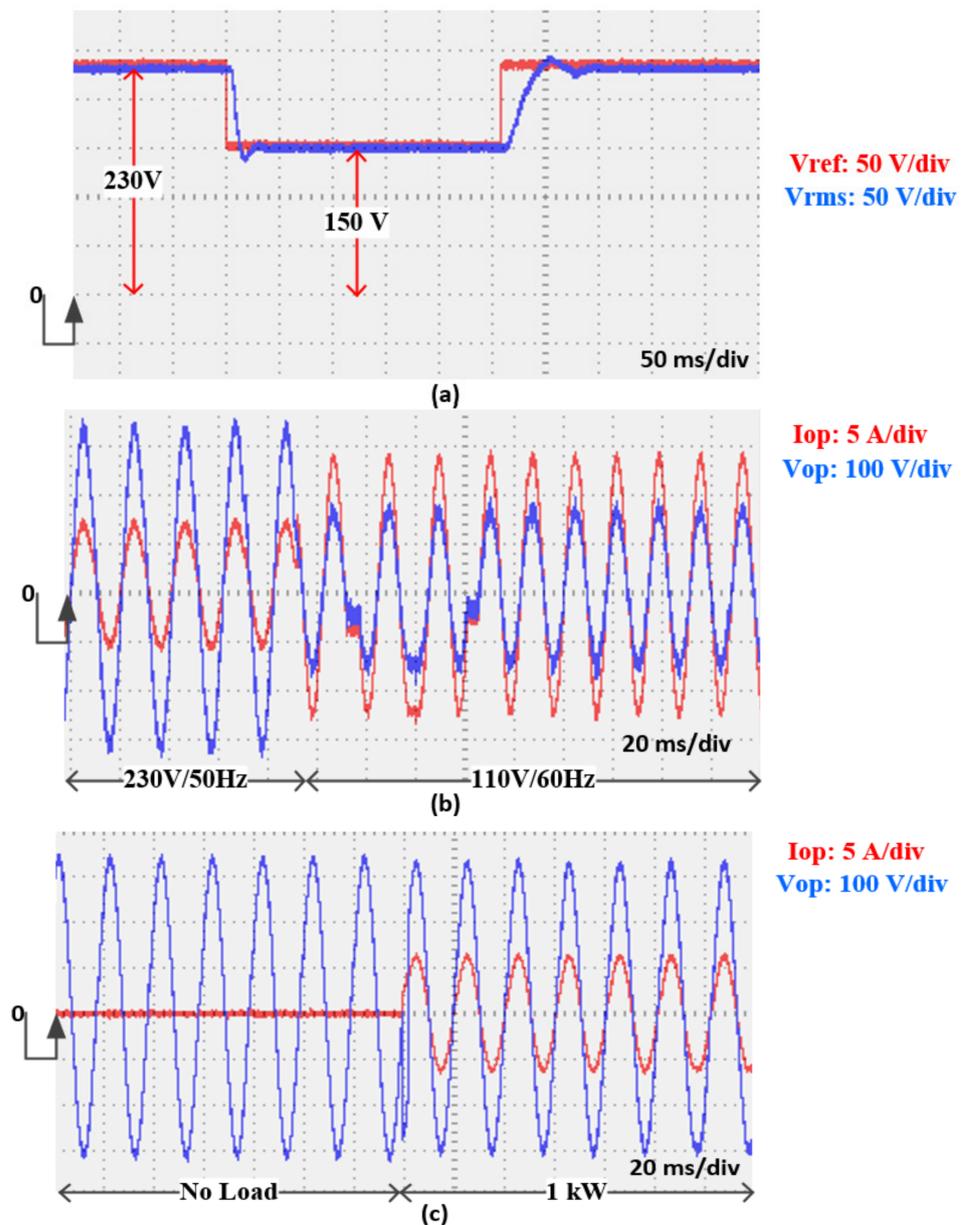


Figure 16. (a) Pulse voltage change response of the controller. (b) Fixed load voltage and frequency control response. (c) No-load to half rated load step change response.

The total blocking voltage (TBV) [41] of the converter is given by:

$$TBV = \left(\sum_{i=1}^n PIV_i \right) / V_{out_{pk}} \quad (23)$$

where PIV is the peak inverse voltage experienced by each semiconductor device, $V_{out_{pk}}$ is the peak output voltage, and n denotes the number of semiconductor devices. For the proposed inverter, the PIV of each switch is 85 volts, i.e., equal to DC link voltage, as shown in Figure 17.

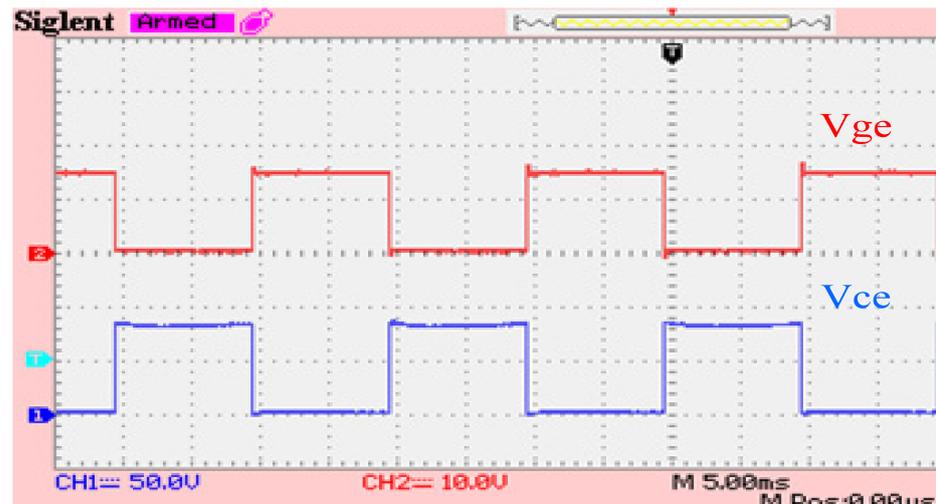


Figure 17. Gating signal $V_{GE} = 15$ Volts and switch voltage $V_{CE} = 85$ volts.

The total number of switches is equal to four, and the peak output voltage is 324.7 volts; therefore, TBV of the proposed converter can be given by:

$$TBV_{LTQGBI} = 4 \times 85 / 324.7 = 1.05 \quad (24)$$

This low value of TBV signifies lower semiconductor costs as well as loss. A detailed comparative evaluation based on different parameters is shown in Table 2.

Table 2. Comparative evaluation.

| Topology | N_s | N_D | N_L | N_C | Filter | Power Level |
|----------|-------|-------|-------|-------|--------|-------------|
| [5] | 6 | 2 | 2 | 2 | Yes | 500 W |
| [7] | 4 | 4 | 2 | 2 | Yes | 250 W |
| [14] | 2 | 0 | 2 | 2 | Yes | 40 W |
| [17] | 29 | 0 | 0 | 8 | NO | 265 W |
| [26] | 5 | 4 | 1 | 2 | Yes | 343 W |
| Proposed | 4 | 0 | 1 | 1 | NO | 2000 W |

When compared with the available designs available in the literature, the superiority of the proposed topology becomes evident. As shown in Table 2, the proposed topology requires fewer components and does not require any filter. This reduces the cost and the losses, is simple, and eases production. Furthermore, this topology achieves more with less as the power level is 4 to 50 times higher than other comparable designs. Finally, operating at kW levels makes this inverter available for different uses, such as battery chargers or electric vehicle domains.

5. Conclusions

The article utilized the conventional H-Bridge-based VSI structure to convert it into a high gain fundamental frequency switched boost inverter capable of converting low voltage DC to required AC voltage in a single stage was proposed in this paper. The proposed converter can have a wide range of applications in renewable energy systems, especially solar-based applications. Further, a variable voltage variable frequency controller was proposed to regulate the load voltage. The proposed controller was effective in regulating the load voltage under disturbances on the source and load intermittencies. The converter was found to have 97% efficiency under full load. A 2-kW laboratory prototype of the proposed converter was developed and found to have the THD levels within the IEEE standards.

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