

Article

HTNURL: Design of a High-Performance Low-Cost Triple-Node Upset Self-Recoverable Latch

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Abstract: A high-performance and low power consumption triple-node upset self-recoverable latch (HTNURL) is proposed. It can effectively tolerate single-node upset (SNU), double-node upset (DNU), and triple-node upset (TNU). This latch uses the C-element to construct a feedback loop, which reduces the delay and power consumption by fast path and clock gating techniques. Compared with the TNU-recoverable latches, HTNURL has a lower delay, reduced power consumption, and full self-recoverability. The delay, power consumption, area overhead, and area-power-delay product (APDP) of the HTNURL is reduced by 33.87%, 63.34%, 21.13%, and 81.71% on average.

Keywords: soft errors; triple-node upsets; self-recoverable; C-element; clock gating; fast path



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1. Introduction

With the semiconductor technology scaling down continuously, higher integration and lower power integrated circuits (ICs) have been successfully developed. However, modern ICs are growing vulnerable to radiation strike gradually [1,2]. Soft errors are mainly brought by the strike of particles, such as protons, neutrons, alpha particles, heavy ions, and electrons [3]. When a particle hits a circuit-sensitive node, the value stored in the node may be changed, resulting in a single-node upset (SNU). However, in the high-density ICs, owing to charge sharing, high-energy particle strike may alter the logic values of double/triple nodes at the same time, resulting in a double-node upset (DNU) or even a triple-node upset (TNU) [4].

The existing radiation-hardened latch designs may achieve TNU tolerance [2–9], but only two of them can be fully TNU self-recoverable [4,9]. A fully self-recoverable latch can restore back to the original correct value(s) after the node(s) has been flipped by particle-striking, avoiding a floated state that can be easily altered by leakage current when the clock interval is long. Although the latches presented in [4,9] are fully TNU-recoverable, their delay and power consumption are large. Therefore, they are not suitable for aerospace applications.

Because of latches' problems mentioned above, we designed a high-performance and low-power latch which is TNU self-recoverable. This latch comprises four series of C-element modules, each consisting of four two-input C-elements. Each C-element fans out to the two C-elements in the next module. Furthermore, fast path and clock gating (CG) techniques are taken to reduce delay and power consumption. Compared with the typical TNU-recoverable latches, the HTNURL proposed in this paper decreases the delay by 69.54%, the power consumption by 30.90%, the area overhead by 3.60%, and the APDP by 88.60%. In addition, process, voltage, and temperature (PVT) estimation indicates it is less sensitive to PVT variations than that of up-to-date latches.

This paper is structured as follows. Section 2 provides some radiation-hardened cell reviews. In Section 3, the working principle, implementation, and reliability verification

of the proposed latch is described. Section 4 compares the latches. In Section 5, we draw conclusions from this paper and show our plan for future work.

2. Typical Radiation Hardened Designs

The C-element and the dual interlocked storage cell (DICE) are the most extensively used in the design of radiation-hardened latches. The 2-input and 3-input C-elements are shown in Figure 1a,c.

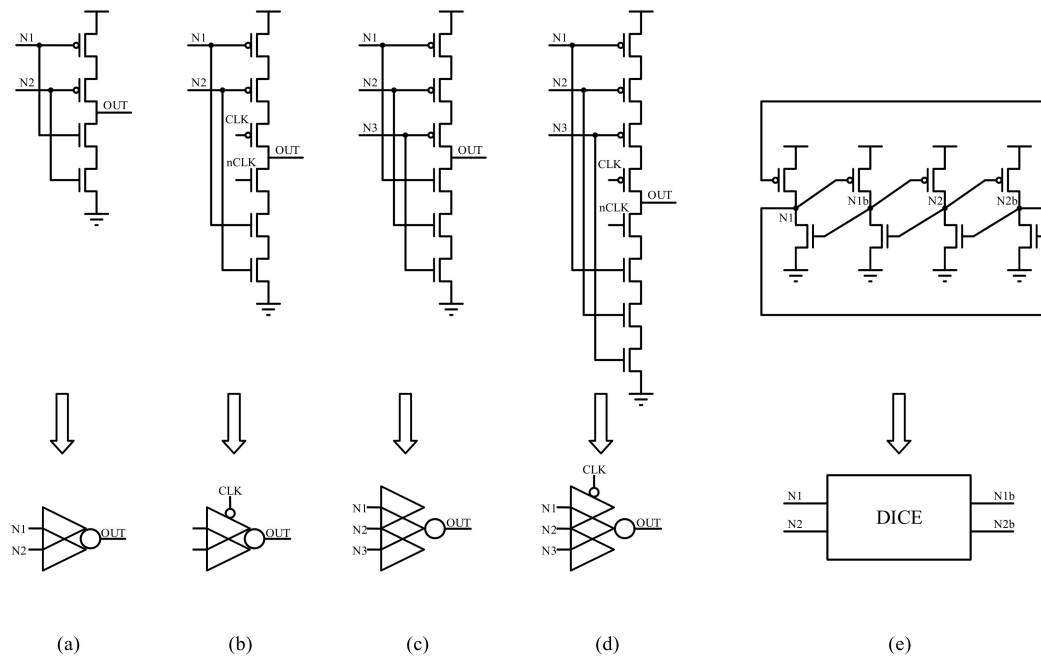


Figure 1. C-elements and DICE: (a) 2-input C-element; (b) CG-based 2-input C-element; (c) 3-input C-element; (d) CG-based 3-input C-element; (e) DICE.

If the inputs of the C-element are the same, the function of the C-element is similar to an inverter. If the inputs of the C-element are different, the C-element outputs a high-impedance state (HIS) and keeps the original value. Figure 1b,d show the CG-based two-input C-element and CG-based three-input C-element that can be controlled by the system clock and the negative system clock signals. Figure 1e is the DICE, which consists of four PMOS transistors and four NMOS transistors. The DICE has four sensitive nodes (N1, N2, N1b, and N2b). Here, a sensitive node is defined as a node in a circuit whose electrical potential can be modified by internal injection or collection of electrical charges [10]. The DICE can self-recover when any nodes are flipped by an SNU, but this structure cannot self-recover from DNU [11].

2.1. LCHRNAN

The low-cost and highly reliable hardened latch design for nanoscale CMOS technology (LCHRNAN) [12] is shown in Figure 2. It tolerates a SNU through the C-elements. Suppose node N5 is struck by a SNU, node nq enters a HIS and keeps the original value, so node Q outputs the correct value. However, the incorrect value of node N5 reaches nodes N1 and N2 through the inverters, causing node N5 to keep the incorrect value and it cannot be recovered until the next clock cycle. Suppose node pair (N5, N6) is struck by a particle and causes a DNU, the value of node nq is flipped, while N5 and N6 keep the incorrect value. Therefore, this latch can only tolerate SNU, but cannot self-recover.

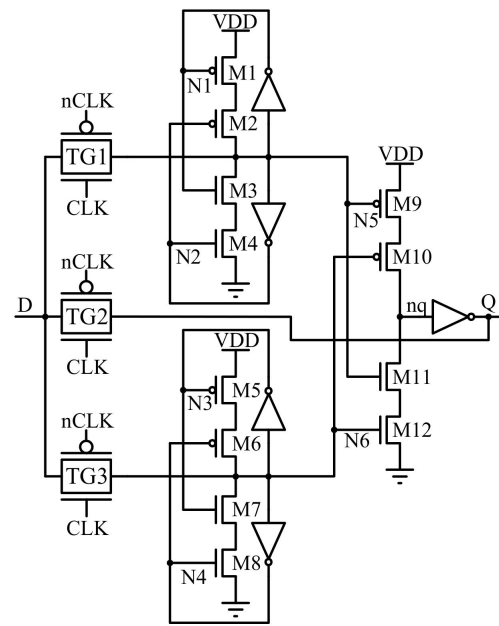


Figure 2. Schematic of LCHRNAN latch.

2.2. HRPV

The highly reliable and high-performance SEU-hardened latch (HRPV) [13] is shown in Figure 3. The latch uses four C-elements to construct a feedback loop. When N2 is struck by a particle causing a SNU, node Q is affected immediately, so N1 and Q enter the HIS and keep their original values. The incorrect value of node N2 is updated by N1. Q keeps the correct value, so the HRPV latch is SNU-recoverable. Suppose node pair (N2, N3) is struck by a particle causing a DNU, the value of nodes Q and N1 are flipped, and thus this latch cannot tolerate DNUs.

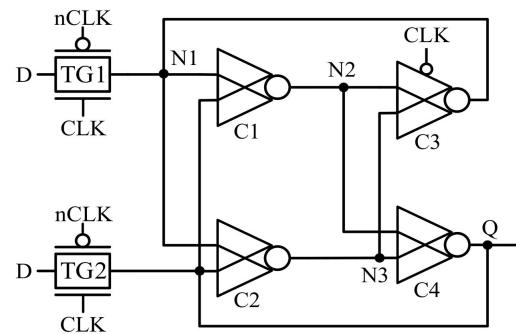


Figure 3. Schematic of HRPV latch.

2.3. DNCS

The double-node charge-sharing SEU-tolerant latch (DNCS) [14] is shown in Figure 4. This latch uses six two-input C-elements to construct a feedback loop to store values and one three-input C-element as a voter at the output. Suppose node pair (N1, N3) is struck and it causes a DNU, the three-input C-element will enter the HIS and keep the original value, so node Q will not be affected. This latch can tolerate DNU but is not self-recoverable.

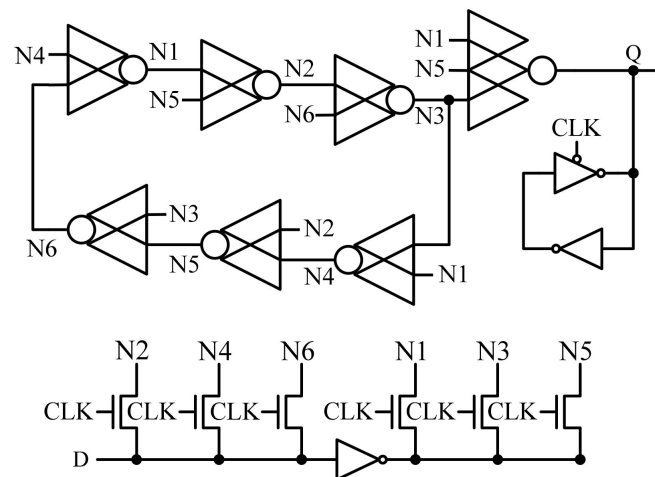


Figure 4. Schematic of DNCS latch.

2.4. Delta DICE

The delta dual interlocked storage cell (Delta DICE) [15] latch is demonstrated in Figure 5. It is composed of three interlocked DICEs. Any two DICEs are connected through a shared node. Suppose node pair (N1, N3) is struck, causing a DNU in DICE A. DICE A cannot self-recover in this case. Since node N1 is the shared node of DICE A and DICE B, it can be recovered by DICE B. Similarly, node N3 can be recovered by DICE C. This latch cannot keep the correct value if all of the shared nodes N1, N3, and N5 are flipped. Therefore, the Delta DICE latch can only be DNU-recoverable and cannot tolerate TNUs. At the same time, many current loops exist in the transparent mode, which causes a lot of power consumption.

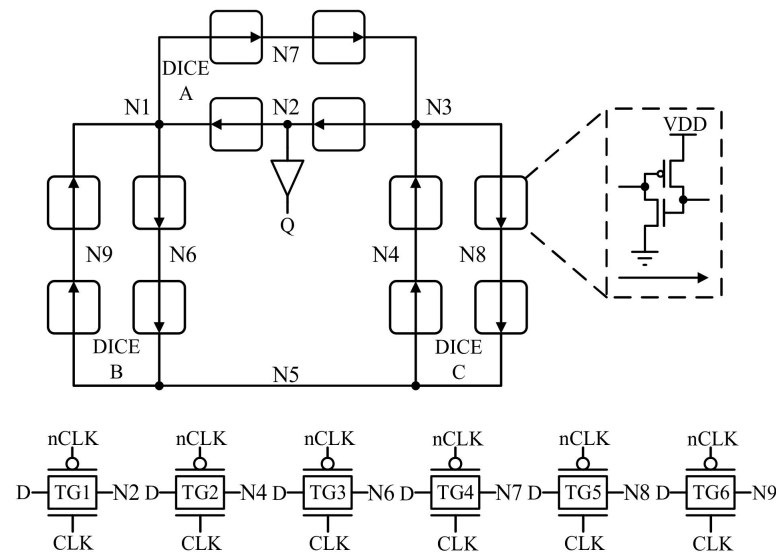


Figure 5. Schematic of Delta DICE latch.

2.5. TNUHL

The TNU-hardened latch (TNUHL) [8] is shown in Figure 6. The latch takes five interlocked four-input C-elements to construct a feedback loop and combines two three-input C-elements and one two-input C-element to filter soft errors. Suppose node set (N1b, N2b, N5b) is struck and it causes a TNU, node N6 is flipped through the three-input C-element. Node N7 enters the HIS and keeps the original value because nodes N3b and N4b are not affected. Similarly, node Q is not affected and maintains the correct value. Therefore, the TNUHL latch can tolerate TNU but cannot self-recover. Besides, the delay of the latch is large.

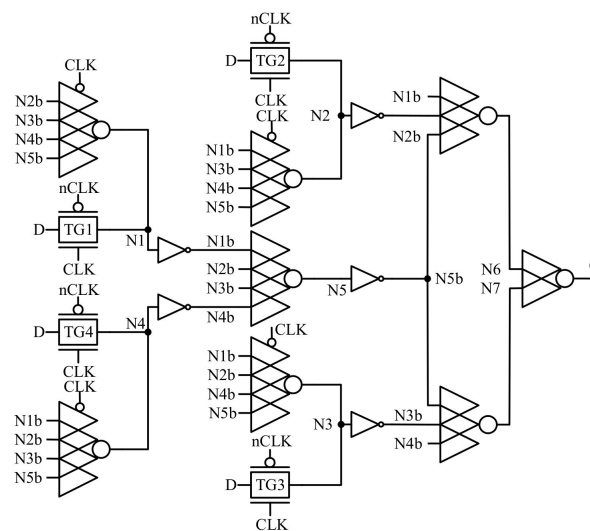


Figure 6. Schematic of TNUHL latch.

2.6. LCTNURL

The low-cost and TNU self-recoverable latch (LCTNURL) [9] is shown in Figure 7. It mainly constructs a feedback loop through twelve circularly linked three-input C-elements (C1–C12). Suppose node set (N1, N7, N11) is struck and it causes a TNU. Since nodes N4, N6, and Q keep their original values, node N1 can be recovered by C1. Similarly, nodes N7 and N11 can be recovered by C7 and C11, respectively. Since the output of any C-element in the latch is connected to the input of the three specified downstream C-elements, the latch can tolerate the TNU and is self-recoverable. However, there are many current paths in the latch, generating a large power consumption.

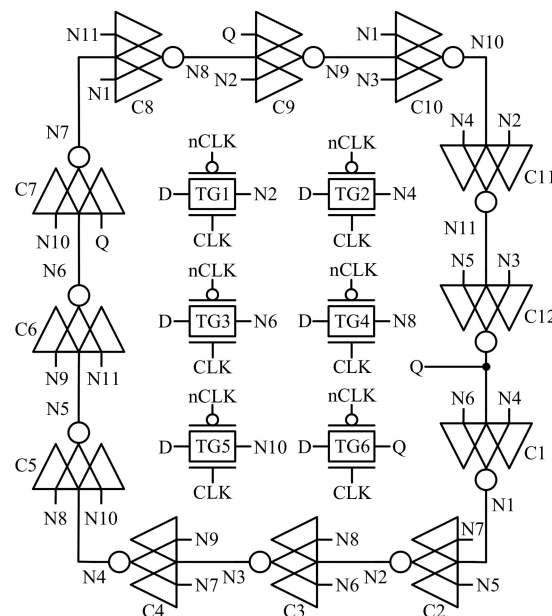


Figure 7. Schematic of LCTNURL latch.

2.7. TNURL

The TNU self-recoverable latch (TNURL) [4] is shown in Figure 8. It is mainly constructed from seven mutually feeding back soft-error-interceptive modules (SIMs), any of which consists of two three-input C-elements and one two-input C-element. Suppose node set (I1, I2, I3) is struck and it causes a TNU. For SIM2, since nodes I4, I5, I6, and Q are not affected, nodes t3 and t4 keep their original values, node I1 can be recovered by nodes

t3 and t4 through the two-input C-element. Similarly, nodes I2 and I3 can be recovered by SIM3 and SIM4, respectively. Due to the mutual feedback mechanism of SIMs and the dual-level soft-error interception of each SIM, the latch can self-recover from any possible TNU. However, the TNU recovery is achieved at the price of an increased area overhead and power consumption penalties.

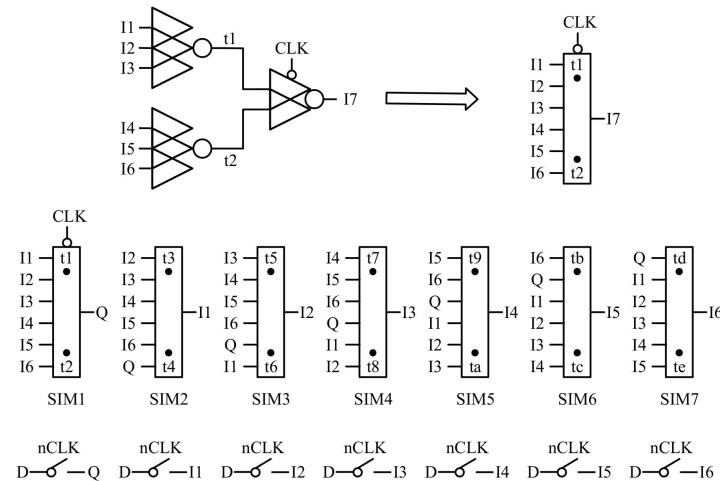


Figure 8. Schematic of TNURL latch.

3. Proposed Hardened Latch Design

3.1. Circuit Design and Behavior

The HTNURL latch is proposed and demonstrated in Figure 9. CLK and nCLK represent the system clock and negative system clock, respectively; TG1–TG4 represent four transmission gates (TGs); N1–N15 represent the data nodes inside the latch; C1–C16 represent 2-input C-elements. It should be noted that C13, C14, C15, and C16 represent CG-based 2-input C-elements. The sensitive nodes in this latch are N1–N14 and Q. The latch is mainly composed of 4 stage C-element modules, and each module is composed of four 2-input C-elements. Each 2-input C-element flows to the input of the two C-elements in the next stage, and each input of the 2-input C-element comes from the 2-input C-element in the previous stage, thus forming a feedback loop.

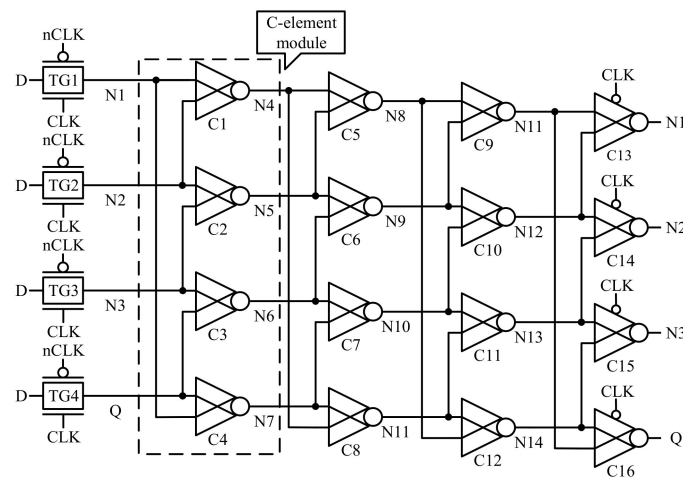


Figure 9. Proposed HTNURL latch design.

When CLK is high and nCLK is low, the HTNURL latch works in transparent mode. At this time, TG1–TG4 are ON, and C13–C16 are OFF. The data of input D are transmitted to nodes N1, N2, N3, and Q through TG1, TG2, TG3, and TG4, and then transmitted to

other nodes (N4–N15) in the following stages through C-elements (C1–C12). Because node Q is connected to node D via TG4, the D–Q delay is reduced.

When CLK is low and nCLK is high, the HTNURL latch works in the latching mode. In this mode, TG1–TG4 are OFF, and C13–C16 are ON. The data are stored in the latch through the feedback loop formed by four C-element modules and outputted through the node Q. The simulation waveform of each node in the transparent mode and latching mode is shown in Figure 10.

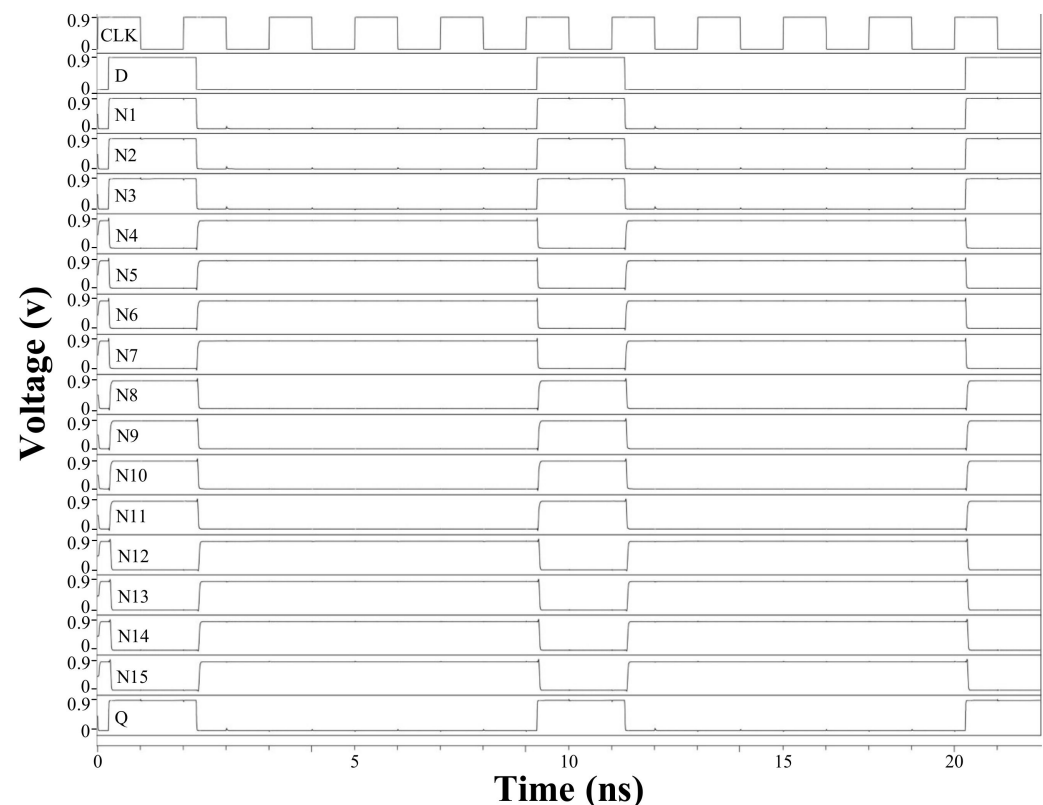


Figure 10. Simulation waveform of HTNURL latch.

SNU-recovery feature: For SNU, because the structure of the latch is symmetric, the impact of a SNU on the latch is the same for any node. Considering N1, when N1 causes a SNU, the logic value of N1 is flipped, and the incorrect value is transmitted to one of the inputs of C1 and C4, but N2 and Q still keep the correct values. According to the transmission characteristics of the C-element, the output nodes N4 of C1 and N7 of C4 keep their original values. Nodes N12 and N13 also keep the correct values and recover node N1 through C13 from the incorrect value. Therefore, the HTNURL latch is SNU-recoverable.

DNU-recovery feature: For DNU, because the structure of the latch is symmetric, the HTNURL latch can be affected by a DNU in three cases.

CASE D1: Two modules are affected.

Taking the node pair (N1, N2) as an example, because each internal node of the HTNURL latch is the shared node of the two modules, the affected modules must be adjacent.

Suppose node pair (N1, N2) is struck by a particle and it causes a DNU, the two input nodes of C1 are both flipped, so the output node N4 of C1 is also flipped. At this time, nodes N3 and Q are kept at the correct values, so nodes N5, N6, and N7 keep their original correct values. Though the value of node N4 is incorrect, due to the correct values of N5 and N7, N8 and N11 keep their original correct values. Hence, the soft error in the HTNURL latch has been completely blocked and will not be transmitted to the next module. Because nodes N12, N13, and N14 keep the correct values, the incorrect values of nodes N1 and N2 can be restored via C13 and C14.

CASE D2: Three modules are affected.

Taking the node pair (N1, N4) as an example, when (N1, N4) is struck by a particle and it causes a DNU, because Q is not affected, the output node N7 of C4 keeps the original value. Though the value of node N4 is incorrect, due to the correct values of N5 and N7, nodes N8 and N11 keep their original values. Because N12 and N13 are not affected, the incorrect value of node N1 can be recovered through C13. At this time, N1 and N2 have correct values, and the incorrect value of node N4 is recovered through C1.

CASE D3: Four modules are affected.

Taking the node pair (N1, N8) as an example, when the node pair (N1, N8) is struck by a particle and it causes a DNU, since nodes N2, Q, N9, and N11 are not affected, nodes N4, N7, N12, and N15 keep their original values. At this time, nodes N12, N13, N4, and N5 have correct values, thus the incorrect N1 and N8 can be restored through C13 and C5.

Therefore, the HTNURL latch is DNU-recoverable.

TNU-recovery feature: For TNU, there are three cases since the latch is symmetric.

CASE T1: Two modules are affected.

Taking the node set (N1, N2, N3) as an example, when (N1, N2, N3) is struck by a particle and it causes a TNU, since the values of both inputs of C1 and C2 are flipped, N4 and N5 are inverted as well. The value of node Q is not affected, so nodes N6 and N7 keep their original values. The values of inputs of C5 are both flipped and the value of node N8 is also flipped. Nodes N9 and N11 still keep their correct values, so nodes N12 and N15 keep their original values. Because all of the nodes N12, N13, N14, and N15 output correct values, the incorrect values of nodes N1, N2, and N3 can be recovered through C13, C14, and C15.

CASE T2: Three modules are affected.

Taking the node set (N1, N2, N5) as an example, when (N1, N2, N5) is struck by a particle and it causes a TNU, N4 is inverted as both inputs of C1 have been flipped. The nodes N3 and Q are not affected, so node N5 keeps the incorrect value, but N6 and N7 keep their original correct values. Because the values of N4 and N5 are flipped, the value of node N8 is also flipped. N6 and N7 are not affected at this time, so nodes N9, N10, and N11 keep their original values. N8 is inverted, and nodes N9 and N11 keep their original correct values, so nodes N12 and N15 keep their original values. Because nodes N13 and N14 keep their correct values, the incorrect values of nodes N1 and N2 are recovered through C13 and C14, and then the incorrect value of node N5 is recovered through C2.

CASE T3: Four modules are affected.

Taking the node set (N1, N4, N8) as an example, when (N1, N4, N8) is struck by a particle and it causes a TNU, since N2 and Q are not affected, the output node N4 of C1 keeps the incorrect value, and the output node N7 of C4 keeps the original value. Because the value of node N5 is not affected, node N8 keeps the incorrect value, and nodes N9 and N11 keep their original values. The output nodes N12 and N15 keep their original values. Nodes N12 and N13 keep correct values, so the incorrect value of N1 is recovered through C13. Nodes N1 and N2 have correct values, so the incorrect value of N4 is restored through C1. Nodes N4 and N5 have correct values, then the incorrect value of N8 is restored through C5.

Therefore, the HTNURL latch is TNU-recoverable.

3.2. Verification Results

The charge deposition mechanism for upsets is direct ionization and indirect ionization. Direct ionization is caused by the incident particle, while indirect ionization is caused by secondary particles created by nuclear reactions between the particle and the device. The charge generated by indirect ionization is significantly different from that generated by direct ionization [16]. An aerospace application may work in both situations. Therefore, we inject enough charges to the latches to flip the nodes indiscriminately in the simulations.

To verify the function of the HTNURL latch design, simulations were performed by Synopsys HSPICE using the 32 nm PTM [17]. The temperature was set to 27 °C, the supply

voltage was set to 0.9 V, and the clock frequency was set to 500 MHz. For TG1–TG4, the PMOS transistors had the ratio W/L as 4 and the NMOS transistors had the ratio W/L as 1. For the rest transistors, the PMOS transistors had the ratio W/L as 2 and the NMOS transistors had the ratio W/L as 1. We used a double-exponential current source model to inject charges in the simulation as in [18]. The equation of the model is shown in (1):

$$I_{inj}(t) = \frac{Q_{inj}}{\tau_1 - \tau_2} \left(e^{\frac{-t}{\tau_1}} - e^{\frac{-t}{\tau_2}} \right) \quad (1)$$

Q_{inj} denotes the amounts of induced charge at time t . τ_1 and τ_2 are the material dependent time constants, and they do not change in the same material (e.g., silicon). Basically, the critical charge is only related to the location of the node in a latch and does not change.

Figure 11 demonstrates the simulation results for SNU injections of the proposed HTNURL latch. When the value of a single node is flipped, none of the other nodes is affected. The incorrect value is restored quickly.

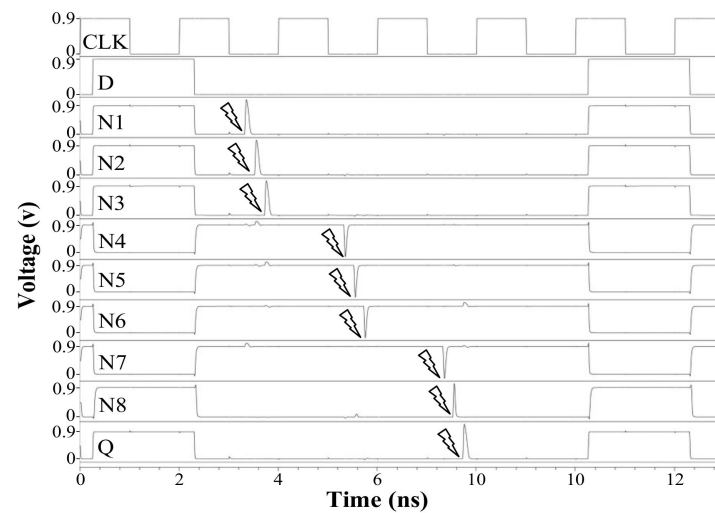


Figure 11. Simulation for SNU injections of HTNURL latch.

Figure 12 demonstrates the simulation for DNU injections of the proposed HTNURL latch. Current was injected into (N1, N2), (N1, N4), and (N1, N8) in turn. After the current injection into the node pair (N1, N2), it can be found that the value of node N4 is instantly flipped, and then all the other flipped nodes are recovered to their correct values.

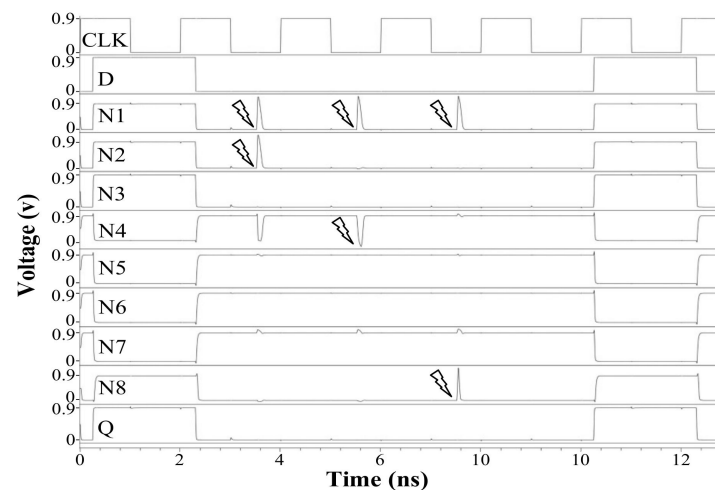


Figure 12. Simulation for DNU injections of HTNURL latch.

Figure 13 demonstrates the simulation for TNU injections of the proposed HTNURL latch. Current was injected into (N1, N2, N3), (N1, N2, N2), and (N1, N4, N8) in turn. After current injection into the node set (N1, N2, N3), it can be found that N4, N5, and N8 are flipped instantly, and then all the affected nodes are recovered to their correct values.

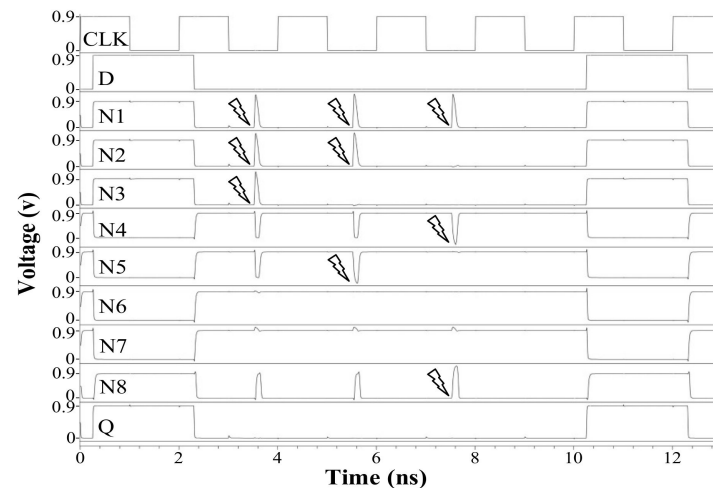


Figure 13. Simulation for TNU injections of HTNURL latch.

In summary, the HTNURL latch is SNU-, DNU- and TNU-tolerant, and self-recoverable. Scaling down the voltage to the sub-threshold/near-threshold regime increases the energy efficiency of the circuits. This technique is widely used in electronics circuits. As shown in Figure 14, the proposed latch works well with the supply voltage ranging from 0.5 V through 0.7 V with a step of 0.04 V. It means if we scale down the supply voltage into the sub-threshold/near-threshold regime, the latch can provide not only good robustness but also a lower power consumption.

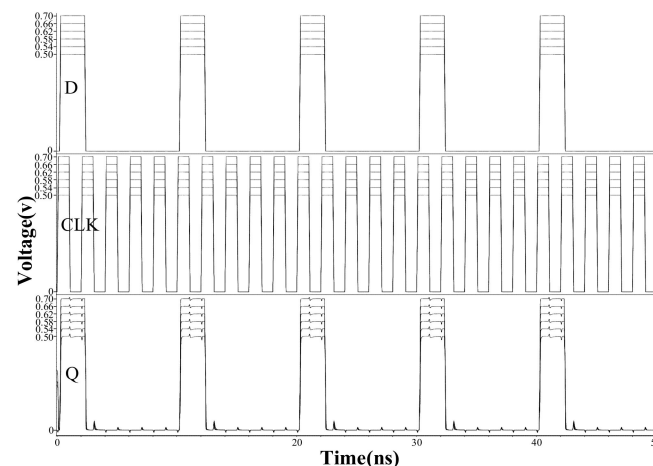


Figure 14. Simulation waveform with supply voltage in sub-threshold/near-threshold regime of the proposed HTNURL latch.

4. Comparisons and Evaluation

4.1. Performance Evaluation

To evaluate and compare the latches fairly, the HTNURL latch design and typical radiation-hardened latches introduced in Section 2 were implemented under the same simulation conditions. All simulations were performed by Synopsys HSPICE tool, using a 32 nm PTM. The temperature was set to 27 °C, the supply voltage was set to 0.9 V, and the clock frequency was set to 500 MHz. The designs were compared regarding the reliability, area, delay, and power consumption. Linear energy transfer (LET) is often used to describe

the sensitivity of a process technology to a particle strike, which is directly proportional to the charge deposited at the particle-struck node [19], so the critical charge about the latches is compared in the following HSPICE simulations.

Table 1 demonstrates the robustness comparisons among the SNU-, DNU-, and TNU-hardened latches. The LCHRNAN latch is only SNU-tolerant instead of SNU self-recoverable, and the DNCS latch is only DNU-tolerant instead of DNU self-recoverable. The Delta DICE latch provides DNU self-recoverability, but it is not reliable when it is affected by a TNU. The TNUHL latch is only TNU-tolerant but not self-recoverable. The LCTNURL, TNURL, and HTNURL provide self-recoverability from SNU, DNU and TNU, while our proposed HTNURL latch has a lower overhead as shown in Table 2.

Table 1. Robustness comparisons among the typical radiation-hardened latches and HTNURL latch.

Latch	SNU Tolerant	SNU Recoverable	DNU Tolerant	DNU Recoverable	TNU Tolerant	TNU Recoverable
LCHRNAN	YES	NO	NO	NO	NO	NO
HRPU	YES	YES	NO	NO	NO	NO
DNCS	YES	YES	YES	NO	NO	NO
Delta DICE	YES	YES	YES	YES	NO	NO
TNUHL	YES	YES	YES	YES	YES	NO
LCTNURL	YES	YES	YES	YES	YES	YES
TNURL	YES	YES	YES	YES	YES	YES
HTNURL	YES	YES	YES	YES	YES	YES

Table 2. Overhead and critical charge comparisons among the typical radiation-hardened latches and HTNURL latch.

Latch	Q_{crit}/fC	Delay/ps	Power/ μW	Area (USTs)	$10^{-3} \times APDP$
LCHRNAN	0.51	37.28	0.53	28	0.56
HRPU	0.75	36.91	0.48	14	0.24
DNCS	0.84	101.6	0.72	50	3.66
Delta DICE	0.99	48.63	1.73	36	3.03
TNUHL	0.47	136.3	0.42	82	4.93
LCTNURL	0.59	33.14	0.90	84	2.51
TNURL	1.33	22.51	1.30	128	3.75
HTNURL	0.70	17.73	0.39	80	0.55

In Table 2, “ Q_{crit} ” is critical charge. “Delay” is D to Q delay, i.e., the average of the rise and fall delays of D to Q. “Power” is the average of static and dynamic power consumption [3]. “Area” is silicon area measured in equivalent USTs as in [7]. “APDP” is the area-power-delay product to comprehensively evaluate overheads of these latches [20]. Though the latch with higher critical charges means it is less sensitive to particle strike, our HTNURL is the most robust because the latch can self-recover after suffering a strike even if a node is flipped. Compared with other TNU-recoverable latches, the HTNURL latch had the lowest area. It achieved a low power consumption and delay without being less robust. The delay of HTNURL is the smallest.

To make quantitative comparisons, we have calculated the relative overhead in terms of delay ($\Delta Delay$), power ($\Delta Power$), area ($\Delta Area$) and APDP ($\Delta APDP$) of the TNU-recoverable latches by Equation (2), as shown in Table 3.

$$\Delta = (Proposed\ latch - Compared\ latch) / Compared\ latch \times 100\% \quad (2)$$

Table 3. Comparisons among TNU-recoverable latches.

Latch	Δ Delay	Δ Power	Δ Area	Δ APDP
LCTNURL	−46.50%	−56.67%	−4.76%	−78.09%
TNURL	−21.24%	−70.00%	−37.50%	−85.33%
Average	−33.87%	−63.34%	−21.13%	−81.71%

As shown in Table 3, we can see that for all the parameters of the latches the percentages are negative, reflecting that all the parameters of the HTNURL latch are the lowest. Compared with the other TNU-recoverable latches, the HTNURL latch reduced the transmission delay by 33.87%, the power consumption by 63.34%, the area overhead by 21.13%, and the APDP by 81.71%. The overhead of the proposed latch is the lowest.

4.2. Effect of PVT Variations on Latches

As the process size is scaled down, the latch becomes more sensitive to the PVT variations [2]. In order to compare the circuit working in different situations, simulations were performed by the HSPICE tool with the 32 nm PTM. PVT variations on the performance of each latch is analyzed, as shown in Figure 15.

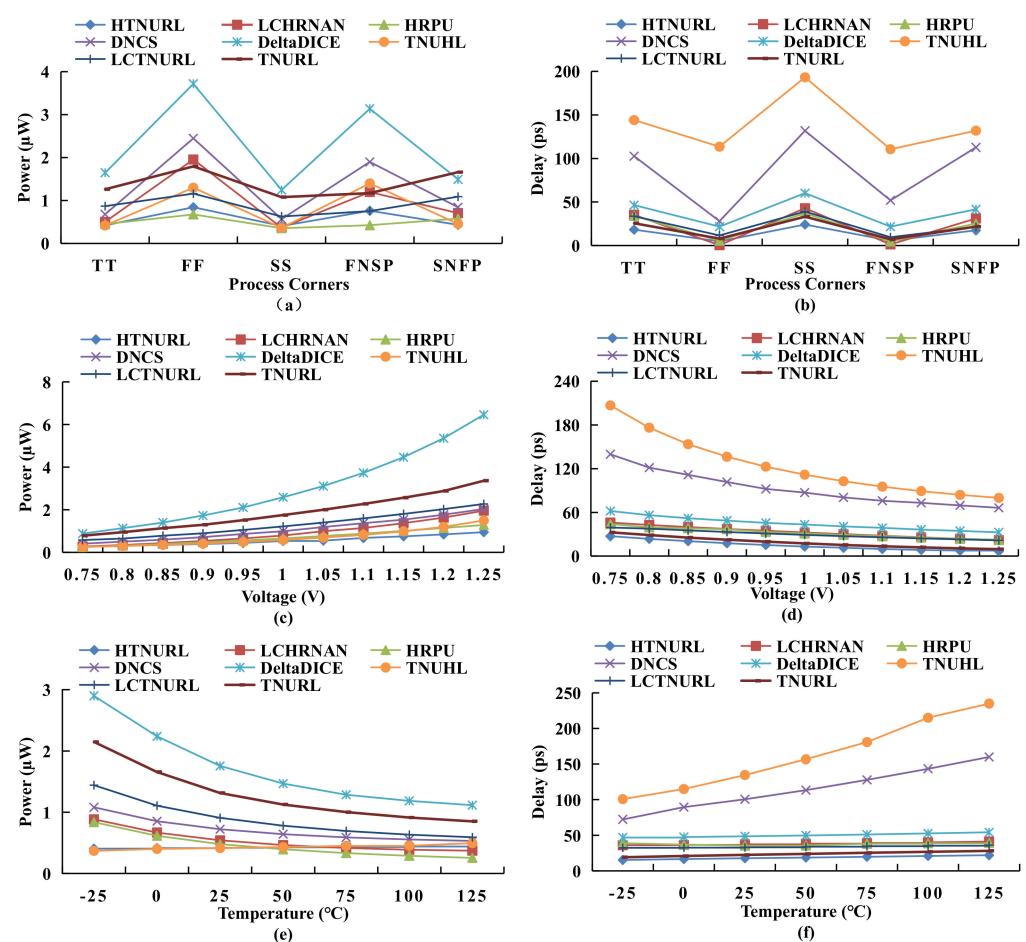


Figure 15. Assessment results of the PVT variations effect on the latches' performances: (a) process corners vs. power; (b) process corners vs. delay; (c) supply voltage vs. power; (d) supply voltage vs. delay; (e) temperature vs. power; (f) temperature vs. delay.

There are five process corners: TT, FF, SS, FNFP, and SNFP [21]. The supply voltage was varied from 0.75 V to 1.25 V, and the temperature was varied from −25 °C to 125 °C.

As shown in Figure 15a,b, the power consumption and delay of the latch vary with the change of process corner. The power consumption of the HTNURL latch is minimal at the SS process corner, the delay of the HTNURL latch is minimal at the process corner of the FF, while it is maximal at the process corner of the SS. The power consumption and delay variations of our latch under different process corners are smaller than those of typical TNU-tolerant/recoverable latches.

As shown in Figure 15c, the power consumption of the latch increases with increasing supply voltage, because the power consumption is proportional to the square of the supply voltage [22]. Meanwhile, as shown in Figure 15d, the latch delay decreases with increasing of the supply voltage, because the higher conducted current on the devices is taken by the higher supply voltage, then the delay decreases [23]. In addition, the power consumption and delay of the HTNURL latch are least affected by the supply voltage changes compared to the other latches.

As shown in Figure 15e,f, the latch delay increases with the temperature increasing, because the carrier mobility decreases when the temperature increases [22]. The delay and power consumption of the HTNURL latch are less effected when temperature changes.

In summary, compared with typical latch designs, the power consumption and delay of the HTNURL latch is less sensitive to PVT variations.

5. Conclusion and Future Work

The development of process technology has caused the radiation-induced TNU to become more serious. Although typical latches can tolerate TNU, they cannot self-recover or they require a larger overhead. Therefore, a TNU-recoverable latch, HTNURL, is proposed. The latch reduces delay by adopting a fast path and uses clock gating technique to reduce power consumption. The HTNURL latch comprises four-stage C-element modules, forming a feedback loop. It can tolerate TNUs and is highly reliable and self-recoverable. The HTNURL latch is cost-effective and has lower delay (i.e., is high-performance) compared to other TNU-recoverable latches, and it has a lower sensitivity to PVT variations. Though the HTNURL latch is cost-effective, the signal scattering is an issue in this field and our next step will be proposing a lower signal-scattering latch in future research.

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References

1. Xu, H.; Zhu, J.; Lu, X.; Li, J. An advanced SEU tolerant latch based on error detection. *J. Semicond.* **2018**, *39*, 81–84. [\[CrossRef\]](#)
2. Yan, A.; Lai, C.; Zhang, Y.; Cui, J.; Huang, Z.; Song, J.; Guo, J.; Wen, X. Novel Low Cost, Double-and-Triple-Node-Upset-Tolerant Latch Designs for Nano-scale CMOS. *IEEE Trans. Emerg. Top. Comput.* **2021**, *9*, 520–533. [\[CrossRef\]](#)
3. Yan, A.; Ling, Y.; Cui, J.; Chen, Z.; Huang, Z.; Song, J.; Girard, P.; Wen, X. Quadruple Cross-Coupled Dual-Interlocked-Storage-Cells-Based Multiple-Node-Upset-Tolerant Latch Designs. *IEEE Trans. Circuits Syst. I Regul. Pap.* **2020**, *67*, 879–890. [\[CrossRef\]](#)
4. Yan, A.; Feng, X.; Hu, Y.; Lai, C.; Cui, J.; Chen, Z.; Miyase, K.; Wen, X. Design of a Triple-Node-Upset Self-Recoverable Latch for Aerospace Applications in Harsh Radiation Environments. *IEEE Trans. Aerosp. Electron. Syst.* **2020**, *56*, 1163–1171. [\[CrossRef\]](#)
5. Yan, A.; Xu, Z.; Yang, K.; Cui, J.; Huang, Z.; Girard, P.; Wen, X. A Novel Low-Cost TMR-Without-Voter Based HIS-Insensitive and MNU-Tolerant Latch Design for Aerospace Applications. *IEEE Trans. Aerosp. Electron. Syst.* **2020**, *56*, 2666–2676. [\[CrossRef\]](#)
6. Kumar, C.; Anand, B. A Highly Reliable and Energy Efficient Triple-Node-Upset Tolerant Latch Design. *IEEE Trans. Nucl. Sci.* **2019**, *66*, 2196–2206. [\[CrossRef\]](#)
7. Song, Z.; Yan, A.; Cui, J.; Chen, Z.; Li, X.; Wen, X.; Lai, C.; Huang, Z.; Liang, H. A Novel Triple-Node-Upset-Tolerant CMOS Latch Design using Single-Node-Upset-Resilient Cells. In Proceedings of the 2019 IEEE International Test Conference in Asia (ITC-Asia), Tokyo, Japan, 3–5 September 2019; pp. 139–144.

8. Watkins, A.; Tragoudas, S. Radiation Hardened Latch Designs for Double and Triple Node Upsets. *IEEE Trans. Emerg. Top. Comput.* **2020**, *8*, 616–626. [[CrossRef](#)]
9. Yan, A.; Hu, Y.; Cui, J.; Chen, Z.; Huang, Z.; Ni, T.; Girard, P.; Wen, X. Information Assurance Through Redundant Design: A Novel TNU Error-Resilient Latch for Harsh Radiation Environment. *IEEE Trans. Comput.* **2020**, *69*, 789–799. [[CrossRef](#)]
10. *Soft Errors in Modern Electronic Systems*; Nicolaidis, M. (Ed.) Springer: New York, NY, USA, 2010; Volume 41.
11. Yan, A.; He, Z.; Zhou, J.; Cui, J.; Ni, T.; Huang, Z.; Wen, X.; Girard, P. Dual-modular-redundancy and dual-level error-interception based triple-node-upset tolerant latch designs for safety-critical applications. *Microelectron. J.* **2021**, *111*, 105034. [[CrossRef](#)]
12. Nan, H.; Choi, K. Low cost and highly reliable hardened latch design for nanoscale CMOS technology. *Microelectron. Reliab.* **2012**, *52*, 1209–1214. [[CrossRef](#)]
13. Rajaei, R.; Tabandeh, M.; Fazeli, M. Single Event Multiple Upset (SEMU) Tolerant Latch Designs in Presence of Process and Temperature Variations. *J. Circuits Syst. Comput.* **2014**, *24*, 68–176. [[CrossRef](#)]
14. Katsarou, K.; Tsiatouhas, Y. Soft error interception latch: Double node charge sharing SEU tolerant design. *Electron. Lett.* **2015**, *51*, 330–332. [[CrossRef](#)]
15. Eftaxiopoulos, N.; Axelos, N.; Zervakis, G.; Tsoumanis, K.; Pekmestzi, K. Delta DICE: A Double Node Upset resilient latch. In Proceedings of the 2015 IEEE 58th International Midwest Symposium on Circuits and Systems (MWSCAS), Fort Collins, CO, USA, 2–5 August 2015; pp. 1–4.
16. Dodd, P.E.; Massengill, L.W. Basic mechanisms and modeling of single-event upset in digital microelectronics. *IEEE Trans. Nucl. Sci.* **2003**, *50*, 583–602. [[CrossRef](#)]
17. Zhao, W.; Cao, Y. Predictive Technology Model for Nano-CMOS Design Exploration. *JETC* **2007**, *3*, 1-es. [[CrossRef](#)]
18. Yamamoto, Y.; Namba, K. Construction of Latch Design with Complete Double Node Upset Tolerant Capability Using C-Element. In Proceedings of the 2018 IEEE International Symposium on Defect and Fault Tolerance in VLSI and Nanotechnology Systems (DFT), Chicago, IL, USA, 8–10 October 2018; pp. 1–6.
19. Shah, A.P.; Gupta, N.; Wlatl, M. High-performance radiation hardened NMOS only Schmitt Trigger based latch designs. *Analog Integr. Circuits Signal Process.* **2021**, 1–15. [[CrossRef](#)]
20. Yan, A.; Huang, Z.; Fang, X.; Ouyang, Y.; Deng, H. Single event double-upset fully immune and transient pulse filterable latch design for nanoscale CMOS. *Microelectron. J.* **2017**, *61*, 43–50. [[CrossRef](#)]
21. Dang, L.D.T.; Kim, J.S.; Chang, I.J. We-Quatro: Radiation-Hardened SRAM Cell With Parametric Process Variation Tolerance. *IEEE Trans. Nucl. Sci.* **2017**, *64*, 2489–2496. [[CrossRef](#)]
22. Huang, Z.; Liang, H.; Hellebrand, S. A High Performance SEU Tolerant Latch. *J. Electron. Test.* **2015**, *31*, 349–359. [[CrossRef](#)]
23. Yan, A.; Liang, H.; Huang, Z.; Jiang, C.; Ouyang, Y.; Li, X. An SEU resilient, SET filterable and cost effective latch in presence of PVT variations. *Microelectron. Reliab.* **2016**, *63*, 239–250. [[CrossRef](#)]