



# Article ESD Design and Analysis by Drain Electrode-Embedded Horizontal Schottky Elements for HV nLDMOSs

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**Abstract:** Electrostatic discharge (ESD) events can severely damage miniature components. Therefore, ESD protection is critical in integrated circuits. In this study, drain-electrode-embedded horizontal Schottky diode contact modulation and Schottky length reduction modulation were performed on a high-voltage 60-V n-channel laterally diffused metal-oxide–semiconductor transistor (nLDMOS) element. The effect of the on-voltage characteristics of cascade Schottky diodes on ESD protection was investigated. By using a transmission-line pulse tester, the trigger voltage, holding voltage, and secondary breakdown current ( $I_{t2}$ ) of the nLDMOS element were determined using the I–V characteristic. As the N<sup>+</sup> area was gradually replaced by the parasitic Schottky area at the drain electrode, an equivalent circuit of series Schottky diodes formed, which increased the on-resistance. The larger the Schottky area was the higher the  $I_{t2}$  value was. This characteristic can considerably improve the ESD immunity of nLDMOS components (highest improvement of 104%). This is a good strategy for improving ESD reliability without increasing the production steps and fabrication cost.

**Keywords:** electrostatic discharge (ESD); holding voltage ( $V_h$ ); lateral diffusion MOS (LDMOS); schottky diode; secondary breakdown current ( $I_{t2}$ ); transmission-line pulse system (TLP system)



Citation: Hong, S.-Z.; Chen, S.-L. ESD Design and Analysis by Drain Electrode-Embedded Horizontal Schottky Elements for HV nLDMOSs. *Electronics* **2021**, *10*, 178. https:// doi.org/10.3390/electronics10020178

Received: 7 December 2020 Accepted: 13 January 2021 Published: 15 January 2021

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### 1. Introduction

Although the efficiency and speed of components have improved with the evolution of semiconductor processes, component integration and cost considerations have become a concern. Generally, compact components are desired. Although the economic benefits of advanced components have increased, reliability uncertainties have also increased. Even a small defect during manufacturing can cause considerable losses to the manufacturer. Electrostatic discharge (ESD) events [1–10] for integrated circuits (ICs) are the major hazard to reliability.

Common discrete ESD protection devices are laterally diffused metal-oxidesemiconductor transistors (LDMOSs), gas discharge tube (GDTs), spark gap (SPGs), transient voltage suppressor (TVSs), and voltage-dependent resistor (VDRs). However, in this paper, a power management high-voltage integrated circuit manufactured by a verylarge-scale interaction bipolar-CMOS-DMOS (VLSI BCD) process uses LDMOS devices to form HV circuits and discusses how to protect their ESD reliability. This LDMOS ESD protection device can be used to protect the I/O port of the circuit. Therefore, LDMOSs have been effectively used in integrated circuits for power electronics, Internet of things (IoT) applications, vehicle electronics, and ESD protection components [11–25], and their importance is gradually increasing. A high-voltage LDMOS has a longer drift region and shallow trench isolation (STI) region. Then, this device has a larger depletion region and higher on-resistance (R<sub>on</sub>) allowing it to operate under high voltage. However, the operating voltage of LDMOSs is considerably high. Good reliability and the ability to withstand large currents are critical in high-current devices. Therefore, the effective discharge of large currents is essential. However, the current density of these high-voltage LDMOS devices is often concentrated between the drain and STI. Therefore, the LDMOS has lower ESD

protection capabilities and at the same time is prone to disadvantages such as latch-up effects [26–32]. Schottky diodes [33–39] typically include metals and semiconductor junctions. In this work, we combined the low turn-on voltage characteristic of Schottky diodes with nLDMOSs to form a parasitic horizontal Schottky region at the drain electrode of the nLDMOS element. Such components exhibit superior reliability and can withstand high ESD currents.

### 2. Sample Designs of the HV nLDMOS

### 2.1. HV nLDMOS Reference Device

High-voltage (HV) laterally diffused metal-oxide-semiconductor transistors (LDMOS) are often used as ESD protection components at the input/output electrodes of circuits to prevent the circuit latch-up effect, which causes the element to burn out. We designed LDMOSs with a protective ring. Typically, to withstand high voltage, a long drift region is necessary and various concentration regions of N-type and P-type doping are used to form a concentration gradient. Furthermore, the element has a high drift region resistance. Various concentration gradients are used to disperse strong electric fields and extend the length of the depletion region to increase the breakdown voltage. Figure 1a displays the cross-sectional view of the parasitic equivalent circuit of the LDMOS component, Figure 1b displays the 3-D structure view, and Figure 1c displays the layout view of the HV nLDMOS reference element. The test element used in this experiment was a nonbutted structure that was fabricated using the TSMC 0.25-µm HV 60-V bipolar-CMOS-DMOS (BCD) process. The component was developed to improve the ESD discharge current capability. The multifinger symmetrical layout design was used in these HV LDMOS transistors to reduce the layout area of elements. The total finger number is four. The channel width  $(W_f)$  of each finger of the element was 75  $\mu$ m. Therefore, the total channel width ( $W_{tot}$ ) was 300  $\mu$ m. A gate-grounded nMOSFET configuration was used in the HV ESD protection structure. The instantaneous ESD surge current was discharged through the parasitic BJT path below the nLDMOS below nLDMOS.







(b)



**Figure 1.** (a) Parasitic equivalent circuit & cross-sectional view, (b) 3-D structure view, and (c) layout diagram of the high-voltage n-channel laterally diffused metal-oxide–semiconductor transistor (HV nLDMOS) reference device.

# 2.2. HV nLDMOSs with Drain Electrode-Embedded Horizontal Schottky Elements (Contact Rows Modulation)

In this study, we removed the N<sup>+</sup> area in the nLDMOS\_ref drain electrode to form an equivalent series Schottky area structure. Figure 2a,b display the 3D structure view and layout view, respectively, of the nLDMOS with the drain electrode parasitic full Schottky diode modulation. The nLDMOS formed a Schottky diode and series parasitic BJT-NPN. Arranging Schottky diodes in series increases the on-resistance of the HV nLDMOS.





**Figure 2.** (**a**) 3D structure view and (**b**) layout diagram of the HV nLDMOS with the drain electrodeembedded full Schottky device modulation.

Figure 3a–c are the 3D structure diagram, layout view, and equivalent circuit of drain-electrode-embedded horizontal Schottky element modulation of the nLDMOS of the nLDMOS. The parasitic Schottky area was modulated by varying the row of contact of the Schottky area. The modulation method involves varying the Schottky area by symmetrically adding the contact windows laying on the top and bottom rows above the chip surface. The Schottky diode region was gradually increased to 2, 4, 8, 16, 32 and 36 rows of contact windows, and the effect of the increase in rows on ESD capability was observed. The ratio of the heavily doped N<sup>+</sup> areas to Schottky diode areas is displayed in Table 1. Equivalently, from Figure 3c, the  $R_{on}$  will be increased as an HV nLDMOS by adding series Schottky diodes in the drain side. Under this parasitic Schottky structure, the drain electrode is equivalent to a series Schottky element and a high impedance R'<sub>drain</sub>.

Furthermore, it is hoped that, through this technique, the  $I_{t2}$  can be increased to improve the ESD withstanding capability of the device.

nLDMOS	N <sup>+</sup> Area (%)	Schottky Area (%)
Ref. DUT	100	0
HorSchottky_02	94	6
HorSchottky_04	84	16
HorSchottky_08	58	42
HorSchottky_16	42	58
HorSchottky_32	16	84
HorSchottky_36	6	94
Full Schottky	0	100



(a)





**Figure 3.** (a) 3D structure view, (b) layout diagram, and (c) equivalent circuit of the HV nLDMOS with the drain electrode-embedded horizontal Schottky elements modulation.

# 2.3. HV nLDMOSs with the Drain Electrode-Embedded Horizontal Schottky Elements (Length Modulation)

Next, another Schottky modulation for the upper and lower rows of contact windows were used as the variable parameter for Schottky length modulation. The Schottky area was then gradually reduced, which effectively reduced the length of the Schottky area by 1.5  $\mu$ m on the left and right sides, 3  $\mu$ m on the left and right sides, and 4.5  $\mu$ m on the left and right sides. The effect of decreasing the ratio of the Schottky diode area and the length of the current path to the drain electrode on ESD capability was observed. Finally, the area ratio of heavily doped N<sup>+</sup> to Schottky diode is listed in Table 2. Figure 4a,b display the structure and layout diagrams of HV nLDMOSs with the drain electrode-embedded horizontal Schottky length modulation.

nLDMOS	N <sup>+</sup> Area (%)	Schottky Area (%)
Ref. DUT	100	0
DSchottky_450	98	2
DSchottky_300	97	3
DSchottky_150	96	4
DSchottky_0 (Same as HorSchottky_02)	94	6

**Table 2.** Area ratios of N<sup>+</sup> and Schottky diode regions in the drain electrode.



(a)



Drair

(b)

Figure 4. (a) 3D structure view and (b) layout diagram of the HV nLDMOS with the drain electrodeembedded horizontal Schottky length modulation.

## 3. Test Method and Test Instrument

Transmission line pulse (TLP) systems [40-42] are generally used to measure the high-voltage and high-current snapback behavior of a test device. This TLP system uses LabVIEW software to control and match the peripheral electronic instruments such as ESD pulse generators, high-frequency digital oscilloscopes, and digital power meters, thus enabling automated measurement mechanisms. This machine can provide a continuous rising square wave to track the I-V characteristic curve of the DUTs, and the short rise and fall time of this continuous square wave can be used to simulate a fast ESD surge. The TLP system is used to simulate the human body model. Thus, the voltage and current response of the element can be obtained through element measurement, and the behavior of short ESD pulses on the protection device can be simulated. Through the TLP system, we can measure I–V characteristics, such as the trigger voltage ( $V_{t1}$ ), holding voltage ( $V_h$ ), secondary breakdown current ( $I_{t2}$ ), and other physical parameters of the component.

#### 4. Experimental Test Results

# 4.1. HV nLDMOSs with Drain Electrode-Embedded Horizontal Schottky Elements (Contact Rows Modulation)

The TLP tester system was used to measure the HV nLDMOS reference device and the DUTs characteristics with drain-electrode-embedded horizontal Schottky modulation (contact rows modulation). The snapback I–V characteristic curve,  $V_{t1}/V_h$  distribution, and secondary breakdown current distribution are displayed in Figures 5–7, respectively. The number of contact window rows increased with the drain-electrode-embedded horizontal Schottky area to completely remove the heavily doped N<sup>+</sup> area. Obviously, from Figure 3c, Schottky\_Drain exhibited a higher secondary breakdown current performance than other DUTs because the drain electrode in the series Schottky diode increased the on-resistance  $(R_{on})$  of the nLDMOS parasitic BJT. Meanwhile, through the measuring test, it can be found that an nLDMOS with the parasitic horizontal Schottky diode at the drain electrode had a limited effect on the breakdown voltage of the device. This modulation of the drainelectrode-embedded horizontal Schottky did not obviously influence the DC breakdown voltage (the maximum value only by 3.95%). Finally, all the measured parameters are displayed in Table 3. The Schottky area increased with the increase in the drain side, which increased  $I_{t2}$  from 2.23 A in the nLDMOS reference device to a maximum of 4.55 A (104%) improvement). From the measured data, it is found that the area of the parasitic Schottky diode in the drain side greatly affects the ESD capability. When the area percentage of an nLDMOS drain side added the Schottky diode exceeds 50%, the ESD robustness (It2) of the device is significantly increased. Then, the ESD immunity of nLDMOS was effectively improved by using these techniques.



**Figure 5.** Snapback I-V curves and leakage currents of HV nLDMOSs with the drain electrodeembedded horizontal Schottky rows modulation.



**Figure 6.** Trigger voltage and holding voltage distribution charts of HV nLDMOSs with the drain electrode-embedded horizontal Schottky rows modulation.



**Figure 7.** Secondary breakdown-current distribution chart of HV nLDMOSs with the drain electrodeembedded horizontal Schottky rows modulation.

**Table 3.** Snapback extracted parameters of HV nLDMOSs with the drain electrode-embedded horizontal Schottky rows modulation.

nLDMOS	Schottky Area %	V <sub>t1</sub> (V)	V <sub>h</sub> (V)	I <sub>t2</sub> (A)
Ref. DUT	0	105.18	34.80	2.23
HorSchottky_02	6	105.40	34.54	2.33
HorSchottky_04	16	106.75	35.07	2.34
HorSchottky_08	42	106.45	35.41	2.35
HorSchottky_16	58	106.65	35.11	2.63
HorSchottky_32	84	105.52	35.83	2.67
HorSchottky_36	94	107.20	37.15	2.73
Full Schottky	100	106.55	36.49	4.55

# 4.2. HV nLDMOSs with the Drain Electrode-Embedded Horizontal Schottky Elements (Length Modulations)

Furthermore, the Schottky length of the nLDMOS drain electrode was reduced to achieve modulation. The components were measured using the TLP tester. The snapback I–V characteristic curve,  $V_{t1}/V_h$  distribution, and secondary breakdown current distribution are displayed in Figures 8–10, respectively. When the length of the Schottky area was decreased by reducing the length of the drain-electrode-embedded horizontal Schottky diode. The Schottky area of the drain electrode of the element gradually decreased, and the contact resistance of the drain electrode equivalent series to the Schottky diode also decreased. Similarly, through the measuring test, it can be found that an nLDMOS with the parasitic horizontal Schottky diode at the drain electrode of this modulation did not influence the DC breakdown voltage (the maximum value was only 2.51%). The secondary breakdown current of ESD immunity was reduced considerably. The measured parameters measured are displayed in Table 4. As the area of Schottky decreased to its minimum value, its  $I_{t2}$  also reached the minimum (2.13 A).



**Figure 8.** Snapback I-V curves and leakage currents of HV nLDMOSs with the drain electrodeembedded horizontal Schottky length modulation.



**Figure 9.** Trigger voltage and holding voltage distribution charts of HV nLDMOSs with the drain electrode-embedded horizontal Schottky length modulation.



Figure 10. Secondary breakdown-current distribution chart of HV nLDMOSs with the drain electrodeembedded horizontal Schottky length modulation.

**Table 4.** Snapback extracted parameters of HV nLDMOSs with the drain electrode-embedded horizontal Schottky length modulation.

nLDMOS	Schottky Area %	V <sub>t1</sub> (V)	V <sub>h</sub> (V)	I <sub>t2</sub> (A)
Ref. DUT	0	105.18	34.80	2.23
DSchottky_450	2	105.41	34.28	2.13
DSchottky_300	3	106.60	35.21	2.22
DSchottky_150	4	105.34	34.99	2.26
DSchottky_0	6	105.40	34.54	2.33

#### 4.3. Summary of HV nLDMOSs with Drain Electrode-Embedded Horizontal Schottky Elements

As described above, the ESD capability  $(I_{t2})$  value and Schottky-area percentage comparisons of HV nLDMOSs with the drain electrode-embedded horizontal Schottky elements by the row and length modulations are organized as shown in Figure 11a,b, respectively. According to the equivalent circuit diagram of Figure 3c, if the Schottky diode is parasitically embedded in the drain side of an nLDMOS, the ESD transient current under the action of an ESD will flow through the path (1) (the partial nLDMOS) and the path (2) (the parasitic Schottky diode). In the case of an HV nLDMOS with the drain electrodeembedded horizontal Schottky elements, the conduction-on resistance of this nLDMOS with a parasitic Schottky diode (path (2)) is higher than that of others nLDMOS part (path (1)). The main ESD current flows through the nLDMOS path (1). However, when the area of the Schottky diode increases, it means that the area of the drain-electrode for removing heavily doped N<sup>+</sup> increases. Due to the low-doped NWell under the drain-electrode, it has a high impedance and favor to limit the ESD current. Therefore, when the Schottky area of the component is higher, the improvement of  $I_{t2}$  is more obvious, especially as the area percentage of an nLDMOS drain side added to the Schottky diode exceeds 50%. When the area percentage of drain-side added the Schottky diode exceeds 94%, this ESD transient current cannot have more path options (it will be more uniform), the robustness  $(I_{t2})$  of the device is significantly increased. This is also the reason why the  $I_{t2}$  will be the highest value for an nLDMOS device with drain side covered 100% full parasitic Schottky diode. However, as the area ratio of the parasitic Schottky diode is small, the conduction path of the device is dominated by the nLDMOS path (1). Then, the characteristics of the parasitic series Schottky diode are not obvious. This leads to the lower It<sub>2</sub> values of these components corresponding to Figure 11b.



**Figure 11.** ESD capability ( $I_{t2}$ ) values and Schottky-area % comparison of HV nLDMOSs with the drain electrode-embedded horizontal Schottky elements by the (**a**) row modulation and (**b**) length modulation.

#### 5. Conclusions

This study described the effect of the drain-electrode of horizontal Schottky modulation on ESD protection. When the contact row modulation was performed for the drain-electrode-embedded horizontal Schottky diode, the area of the Schottky diode gradually increased. Under the parasitic Schottky structure of part or all of the drain electrode, the equivalent ON-resistance of the overall HV LDMOS device will be increased. Therefore, a higher Schottky area in the drain electrode of the element results in a higher secondary breakdown current. The component can withstand a larger ESD current. Therefore, when the area of the drain electrode Schottky diode increases, the ESD immunity will increase significantly, especially when the area percentage of the Schottky diode exceeds 50%. Especially, when the nLDMOS drain side is all covered with the parasitic Schottky diode, its ESD capability ( $I_{t2}$ ) will increase from 2.23 A in the nLDMOS Reference device to a maximum value of 4.55 A (an increase of 104%). The  $I_{t2}$  was excellent, and the ESD protection capability of the device was also satisfactory.

**Author Contributions:** Conceptualization, S.-Z.H. and S.-L.C.; data curation, S.-Z.H.; formal analysis, S.-Z.H.; investigation, S.-Z.H. and S.-L.C.; project administration, S.-L.C.; supervision, S.-L.C.; validation, S.-Z.H. and S.-L.C.; writing—original draft, S.-Z.H.; writing—review and editing, S.-L.C. All authors have read and agreed to the published version of the manuscript.

Funding: This research was no external funding.

**Data Availability Statement:** Data can be provided according to industry R&D requirements (The data used in the study may be available depending on the corresponding author).

**Acknowledgments:** In this work, the authors would like to thank the Taiwan Semiconductor Research Institute in Taiwan for providing the process information and fabrication platform of TSMC.

Conflicts of Interest: The authors declare no conflict of interest.

### Abbreviations

BCD	Bipolar-CMOS-DMOS
BJT	Bipolar transistor
ESD	Electrostatic discharge
GDT	Gas discharge tube
HV	High-voltage
I <sub>t2</sub>	Secondary breakdown current
LDMOS	Lateral diffused metal-oxide-semiconductor transistor
SPG	Spark gap
STI	Shallow trench isolation
TLP	Transmission-line Pulse
TVS	Transient voltage suppressor
VDR	Voltage-dependent resistor
V <sub>h</sub>	Holding voltage
VLSI	Very-large-scale integration
V <sub>t1</sub>	Trigger voltage

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