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# A Fast Lock All-Digital MDLL Using a Cyclic Vernier TDC for Burst-Mode Links

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**Abstract:** An all-digital multiplying delay-locked loop (MDLL)-based clock multiplier featuring a time-to-digital converter (TDC) to achieve fast power-on capability is presented. The proposed MDLL adopts a new offset-free cyclic Vernier TDC to achieve a fast lock time of 15 reference clock cycles while maintaining a wide detection range and high resolution. The proposed offset-free TDC also uses a correlated double sampling technique to remove mismatch and offset issues, resulting in low jitter characteristics. After the MDLL is quickly locked, the TDC is turned off, and it goes into delta-sigma modulator (DSM)-based sequential tracking mode to reduce power consumption and improve jitter performance. Implemented in a 65-nm 1.0-V CMOS process, the proposed MDLL occupies an active area of 0.043 mm<sup>2</sup> and generates a 2.4-GHz output clock from a 75-MHz reference clock (multiplication factor N = 32). It achieves an effective peak-to-peak jitter of 9.4 ps and consumes 3.3 mW at 2.4 GHz.

**Keywords:** multiplying delay-locked loop; MDLL; TDC; frequency multiplication; serial link



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## 1. Introduction

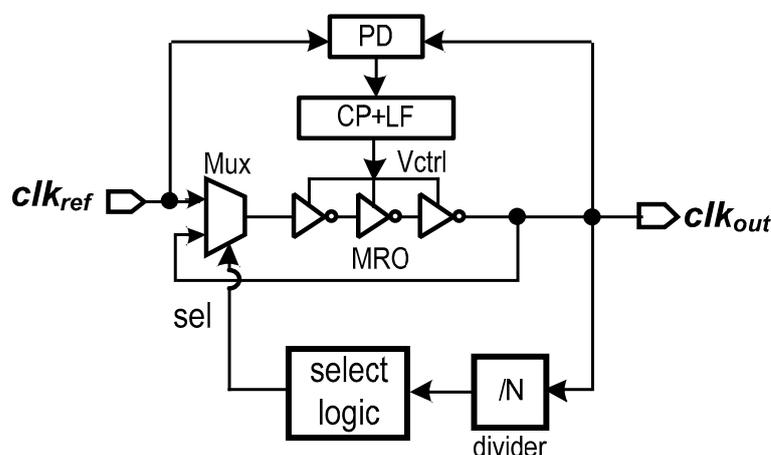
As the demand for high-speed off-chip I/O bandwidth in computing systems increases, the importance of energy efficiency of serial links is rapidly increasing. One approach to address this problem is to use burst-mode communication. Burst-mode data communication, traditionally applied to passive optical networks (PONs), has recently begun to be applied to electrical chip-to-chip serial links [1–4]. In conventional serial links, there is idle power consumed by transceivers even when the link is not in use. However, in a burst-mode-based energy proportional link [4], energy efficiency can be increased because the link and transceivers are powered-on/-off rapidly only when there is a data transmission request.

One of the most critical building blocks in this high-speed energy proportion link design is a fast power-on (or fast lock) clock multiplier for burst-mode operation. The fast power-on/-off clock multiplier should have the ability to quickly multiply the reference clock and complete the phase lock to generate a de-skewed high-frequency output clock.

In general, clock multipliers have been designed based on phase-locked loops (PLLs). However, the loop bandwidth of a typical PLL cannot be easily increased to shorten the lock time due to stability problems [5]. Various techniques have been proposed in the PLL structure to reduce the locking time. Among the PLLs showing reasonable power and performance, the digital PLL from [6] achieved a lock time of forty reference clock cycles, which is insufficient for use in burst mode serial link applications.

In this paper, instead of using a PLL, we introduce a clock multiplier technology that uses a digital multiplying delay-locked loop (MDLL) to obtain fast lock characteristics. A typical MDLL generates the output clock frequency  $f_{\text{clkout}}$  that is N times the reference clock frequency  $f_{\text{clkref}}$ , where N is the frequency multiplication factor [7–19]. Figure 1 shows the block diagram of a typical MDLL. It consists of a multiplexer (MUX), a multiplexed ring

oscillator (MRO), a phase detector (PD), a charge pump (CP) + loop filter (LF), a divider  $N$ , and a select logic. By periodically injecting a clean reference clock edge, the MDLL can achieve better jitter performance with reduced loop bandwidth limit issues. The extended loop bandwidth of the MDLL can bring fast lock characteristics, but most of the MDLLs presented so far have been mainly concerned with jitter and phase noise characteristics.



**Figure 1.** Typical multiplying delay-locked loop (MDLL) architecture.

Among the various all-digital MDLL architectures [8–19], the work from digital MDLL [14] achieved a lock time of forty clock cycles by using a successive approximation register (SAR)-based binary search algorithm. To further improve the locking time of a digital MDLL, we propose a new method of using a time-to-digital converter (TDC) [20–26] in this paper. Conventionally, the purpose of using a TDC in digital MDLL design was to generate a digital bit proportional to the phase difference between two inputs by replacing a phase detector (PD). Since the quantization error of a TDC causes a jitter increase, the main issue of conventional TDC-based MDLLs was in the design of a high-resolution TDC with low power consumption [8,13]. In these conventional digital MDLLs, low jitter and low reference spur characteristics were the main concern, and little attention was paid to fast power-on or locking time.

In this paper, we present a new all-digital MDLL that features a cyclic Vernier TDC to achieve fast power-on capability. This is the first fast lock all-digital MDLL that utilizes a cyclic Vernier architecture [20–26] to achieve a wide detection range and high resolution. The rest of this paper is organized as follows. Section 2 presents the architecture and operation of the proposed all-digital MDLL, Section 3 shows the experimental results, and Section 4 presents the conclusion.

## 2. Proposed All-Digital MDLL

### 2.1. Proposed MDLL Architecture

Figure 2 shows a conceptual diagram of the proposed MDLL detecting the initial phase error ( $=\Delta t$ ) using a TDC at the beginning of the operation, where  $T_{REF}$  is the period of the reference clock ( $clk_{ref}$ ),  $T_1$  is the period of the initial output clock ( $clk_{out}$ ), and  $T_2$  is the period of the  $clk_{out}$  after locking. Ideally,  $T_2 = T_1 + \Delta t/N$  after locking, where  $N$  is the frequency multiplication factor.

Figure 3a shows the proposed all-digital MDLL architecture, which consists of an offset-free cyclic Vernier TDC, a lock detector (LD), a digital loop filter (DLF), a bang-bang phase detector (BBPD), a second-order delta-sigma modulator (DSM), three binary-to-thermometer decoders (coarse/fine/DSM), a digitally controlled multiplexed ring oscillator (MRO), a/16 frequency divider, a/2 frequency divider, and a select logic. The MRO is a pseudo-differential inverter with three types of varactor delay cells (63 coarse delay cells, 15 fine delay cells, 3 DSM cells). As shown in Figure 3b, the proposed MDLL has two operation modes: TDC mode and sequential tracking mode. When the proposed MDLL is

enabled, the MRO starts at the maximum operating frequency. The proposed cyclic Vernier TDC measures the initial phase error ( $\Delta t$ ) between the  $N + 1$ th rising edge of  $clk_{out}$  and the rising edge of  $clk_{ref}$  (as shown in Figure 2) and converts this  $\Delta t$  value to a 10-bit digital TDC code. Then, the TDC code is filtered by the DLF. And the DLF generates the 16-bit LF [15:0] signal. The three decoders generate signals (coarse [62:0], fine [14:0], and dither [2:0]) that control the delay of the MRO.

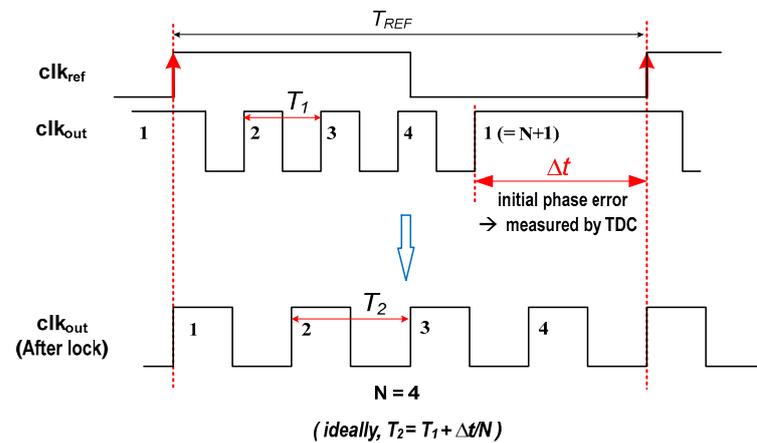


Figure 2. Initial phase error detection using a time-to-digital converter (TDC) in the proposed MDLL.

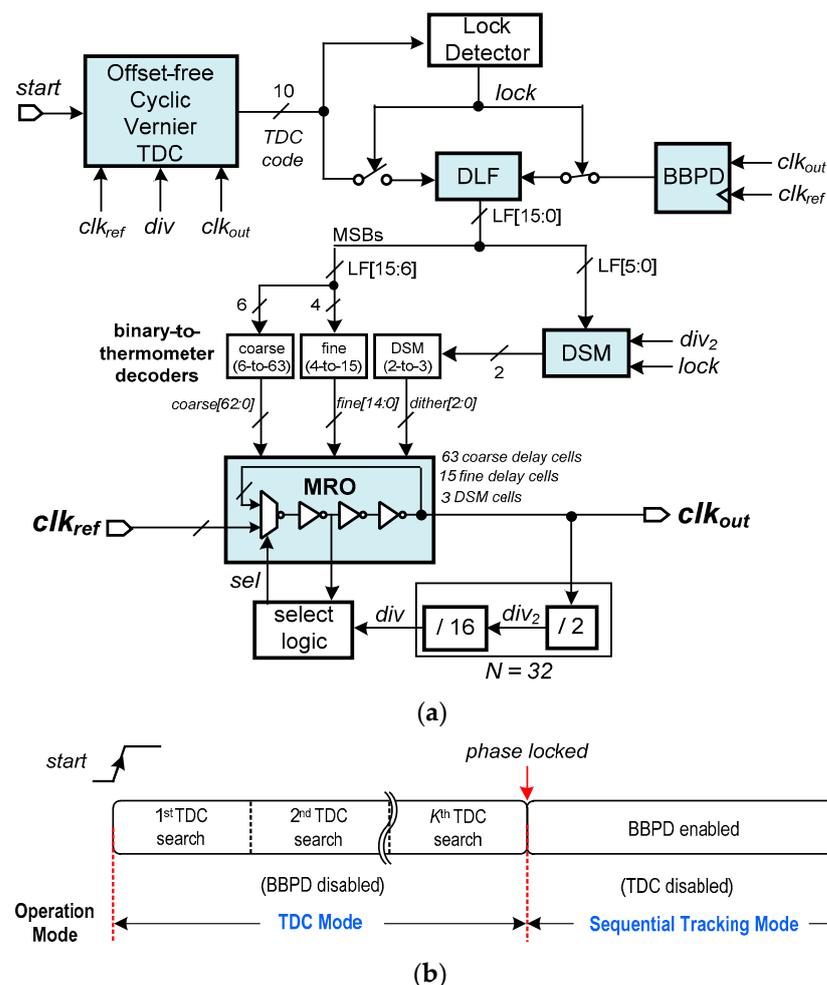


Figure 3. Proposed fast-lock all-digital MDLL, (a) architecture, (b) operation mode.

The coarse decoder utilizes the six most-significant-bits (MSBs) of the LF [15:0] to generate the thermometer code signal (coarse [62:0]) that adjusts the programmable delay value of the coarse delay cells of the MRO. Similarly, the fine decoder utilizes the LF [9:6] signal to provide the fine [14:0] signal that adjusts the fine delay cells of the MRO. The DLF’s 6-bit least-significant-bits (LSBs) are used for the DSM, and the DSM decoder generates the dither [2:0] signal that controls the DSM cells of the MRO at high speed. Here, the sum of the programmable delay of the 15 fine delay cells is equal to the delay of one coarse delay cell. The delay resolution of the DSM cell and that of the fine delay cell are the same.

As shown in Figure 3b, in the TDC mode, the TDC search can be repeatedly performed several times. Each TDC search requiring three reference clock cycles uses a correlated double sampling technique [13,27] to eliminate mismatch and offset issues. Ideally, the TDC mode can be completed with only one TDC search. However, the mismatch problem between the MRO and TDC remains unless offset calibration is used, which leads to repetitive TDC searches. A single TDC search takes three  $T_{REF}$  cycles, and the TDC mode is completed through a maximum of five TDC search iterations. Subsequently, when phase lock is completed, the LD generates the lock signal, and the MDLL enters the sequential tracking mode. In this sequential tracking mode, the TDC is turned off, and both the BBPD and the DSM are enabled. Therefore, after fast phase locking, the MDLL operates in a closed-loop and can track the process, voltage, and temperature (PVT) and environment variations while simultaneously reducing power consumption and improving jitter performance. The DSM receives 6-bit LSBs, LF [5:0], of the DLF and generates a 2-bit binary signal with a frequency 16 times higher than the BBPD operating frequency. Then, the DSM decoder generates dither [2:0] signals operating at high speed to control the DSM cells of the MRO, which effectively reduces the dithering jitter of the digital MDLL [15].

2.2. Proposed Offset-Free Cyclic Vernier TDC

Figure 4 shows the block diagram of the proposed offset-free cyclic Vernier TDC. The proposed TDC consists of an EN generator, a reset generator, a slow ring oscillator (RO), a fast RO, an edge detector, two multiplexers, and a 10-bit up/down counter. The fast RO has a period of  $T_{fast}$  that is slightly faster than  $T_{slow}$ . As shown in the lower right Figure 4, the TDC is used to measure the initial phase error ( $=\Delta t$ ) between the  $N + 1$  th rising edge of  $clk_{out}$  and the rising edge of  $clk_{ref}$ .

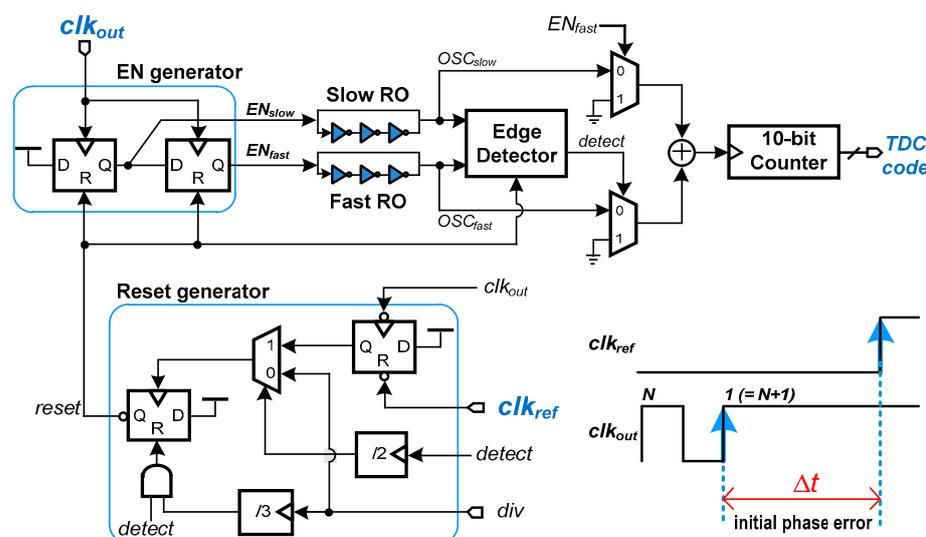


Figure 4. Proposed offset-free cyclic Vernier TDC.

Figure 5 shows the detailed operation process of the proposed TDC mode with an example of  $N = 4$ . Each TDC search process takes three reference clock cycles. When the

TDC is activated, the EN generator creates the ENslow and ENfast signals that enable the two ROs. The initial phase difference between these two signals is equal to  $t_{cyc} + \Delta t$ , where  $t_{cyc}$  is the free-running period of the  $clk_{out}$  (=output of the MRO). The 10-bit counter counts the oscillation number (=m) of the OSCslow signal during the time from the rising edge of the ENslow to the rising edge of the ENfast. Instead of using two separate counters, the 10-bit counter counts the oscillation number (=n) of the OSCfast again during the time from the rising edge of the ENfast to the rising edge of the detect signal: in this example,  $m = 3$  and  $n = 4$ . The edge detector shown in Figure 4 compares the OSCslow and OSCfast signals and generates the detect signal when the rising edge of OSCfast leads to the rising edge of OSCslow. The detect signal makes the reset signal go to logic high, making the outputs of the EN generator fall to logic low. Then, the detect signal falls to logic low again. As a result, in the first reference clock cycle,  $t_{cyc} + \Delta t$  is measured and can be determined as follows:

$$t_{cyc} + \Delta t = T_C + T_F = m \cdot T_{slow} + n \cdot (T_{slow} - T_{fast}) \tag{1}$$

where  $T_C$  is the coarse delay,  $T_F$  is the fine delay, and  $T_{slow} - T_{fast}$  is the fine resolution of the proposed TDC. Similarly, the second reference clock cycle is used to measure the  $t_{cyc}$ . By subtracting the code value of the second cycle from the code value of the first cycle, the required initial phase error  $\Delta t$  can be obtained. The third reference clock cycle is used to apply this subtracted TDC code to the DLF and the MRO, and accordingly, the delay of the MRO is changed, and the MDLL approaches the coarse phase lock state.

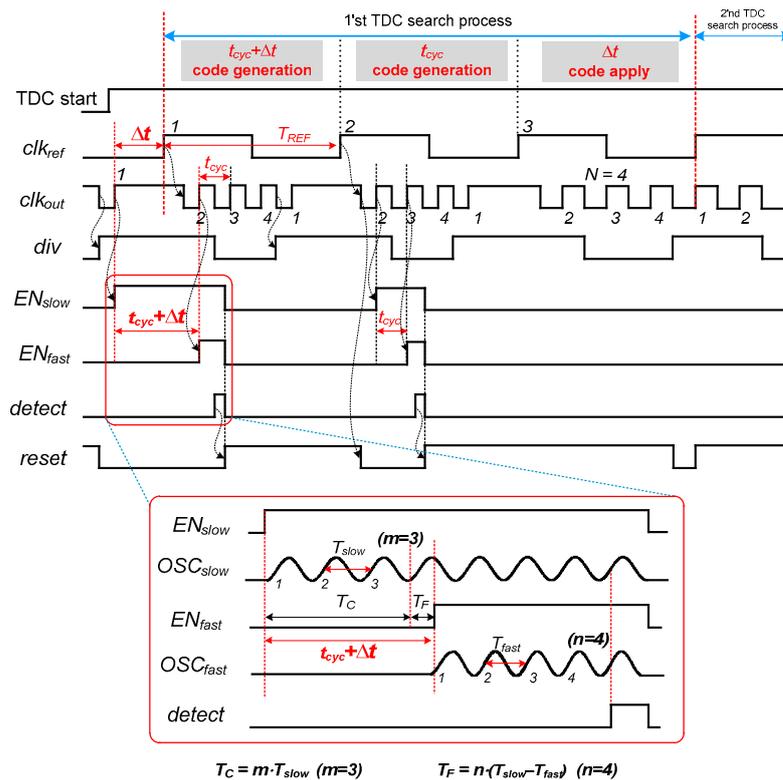


Figure 5. Operation process of the proposed TDC mode.

When the TDC measures the time difference, there can always be a time offset,  $\Delta_{offset}$ . This  $\Delta_{offset}$  is caused by analog nonidealities, such as signal path mismatch and device mismatch, and causes a problem of increasing the deterministic jitter of an MDLL. To overcome this problem, the proposed TDC mode adopts a correlated double-sampling technique [13,22] to eliminate mismatch and offset problems and improve jitter performance.

In Figure 5, what the TDC actually measures in the first sampling period is not  $t_{cyc} + \Delta t$  but  $t_{cyc} + \Delta t + \Delta_{offset}$ , which is a value including the time offset  $\Delta_{offset}$ . The value measured

in the second sampling period is not  $t_{cyc}$ , but  $t_{cyc} + \Delta_{offset}$ . Therefore, if the values of two consecutive measurement codes are subtracted from each other, the  $\Delta_{offset}$  can be removed, and the correct  $\Delta t$  can be obtained. When the  $\Delta t$  value becomes smaller than the resolution ( $=T_{slow} - T_{fast} = 6$  ps in this design) of the Vernier TDC after up to a maximum of five TDC searches are performed, the lock detector generates the lock signal, and the MDLL enters the sequential tracking mode. Then, the TDC is disabled to reduce power consumption, and both the BBPD and the DSM are enabled.

The lower six-bits, LF [5:0], of the DLF output, are used for the DSM. The DSM operates 16 times faster than the reference clock and generates a 2-bit signal for the DSM decoder. Then, the DSM decoder generates dither [2:0], which controls the three DSM cells at high frequency. This DSM-based dithering jitter reduction scheme brings the advantage of greatly improving the deterministic jitter performance of the proposed MDLL with a large N value [15].

### 3. Experimental Results

The proposed MDLL has been implemented in a 65-nm CMOS process. Figure 6 shows the layout of the proposed MDLL core, where the active area is about  $0.043 \text{ mm}^2$ . When the 75 MHz input reference clock is multiplied by  $N = 32$  to generate an output clock of 2.4 GHz, the power consumption is about 3.3 mW from a 1.0 V supply.

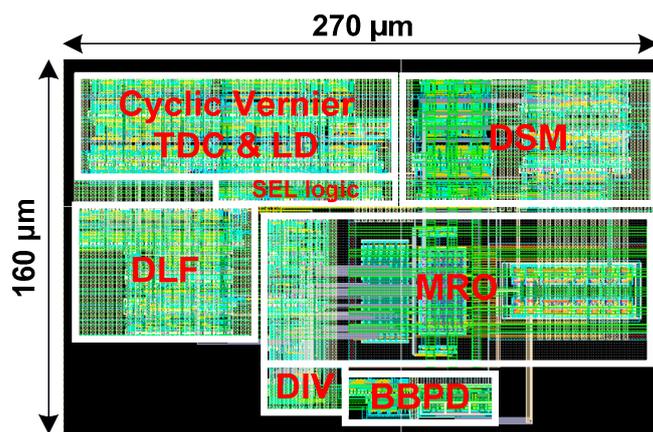


Figure 6. Layout of the proposed fast lock MDLL core block.

Figure 7 shows the simulated locking process of the proposed all-digital offset-free cyclic Vernier-based MDLL. When the MDLL is enabled and the TDC starts operating at 160 ns, the initial phase error ( $=\Delta t$ ) is about 2.9 ns. Since each TDC search process takes three reference clock cycles, the 10-bit output value of the DLF, LF [15:6], is changed at every three reference clock cycles. After five TDC search operations taking 15 reference clock cycles, the phase error becomes less than 2.3 ps, and the MDLL starts the sequential tracking mode. At this point, the MDLL is phase-locked, the TDC is turned off, and the BBPD and DSM are turned on to maintain the lock state.

Figure 8 shows the simulated jitter and reference spur performances of the proposed fast-lock all-digital MDLL at 2.4 GHz ( $N = 32$ ). It achieves a root-mean-square (RMS) jitter of 0.82 ps and a peak-to-peak (p-p) jitter of only 4.0 ps. It also achieves a reference spur of  $-38.1$  dBc. As shown in Figure 9, with an intentionally injected 8.08 ps p-p input clock jitter noise, the proposed MDLL obtains a 17.46 ps p-p (RMS jitter = 2.58 ps) output clock jitter. This means that even when input noise is injected, the effective p-p jitter is only 9.38 ps ( $=17.46 \text{ ps} - 8.08 \text{ ps}$ ). Table 1 compares the performance of the proposed MDLL with previous digital MDLLs. Among the digital MDLLs, the proposed MDLL has the fastest locking time of less than 15 reference clock cycles, which is suitable for use in energy proportional serial link applications.

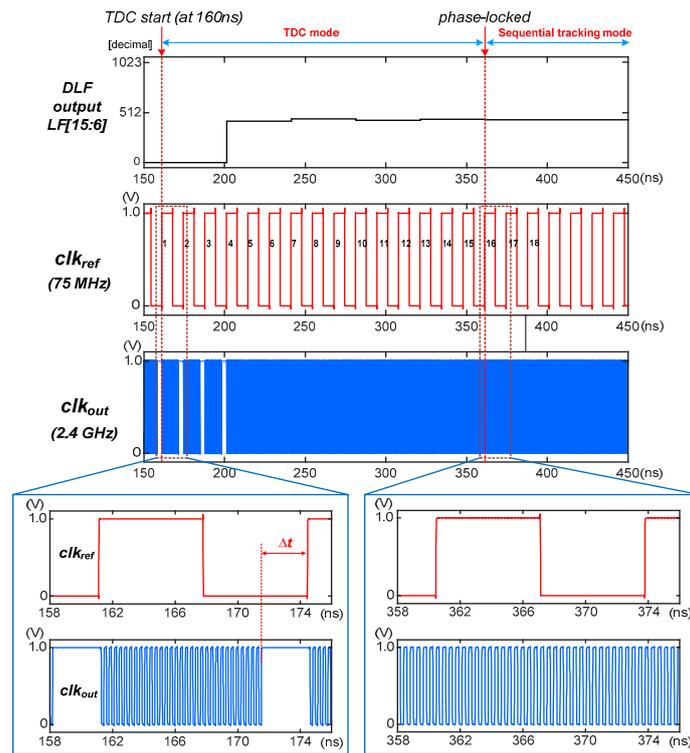


Figure 7. Simulated locking process of the proposed fast lock all-digital MDLL (@2.4 GHz, N = 32).

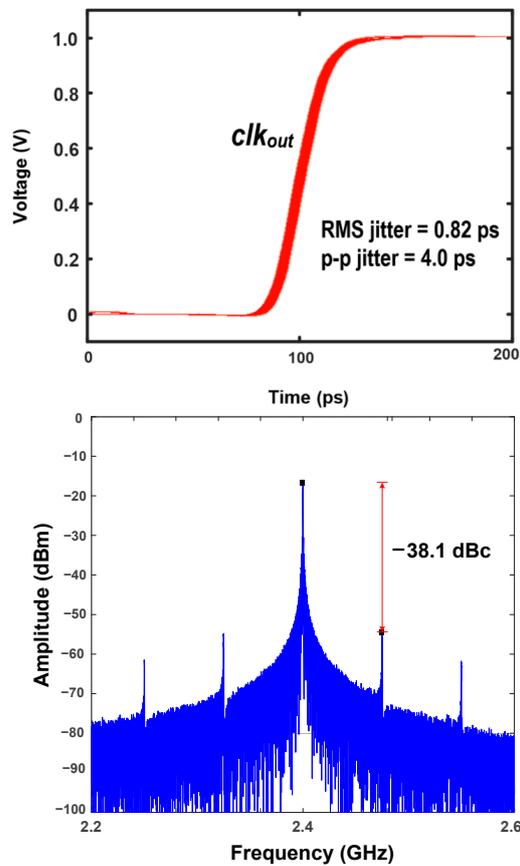


Figure 8. Simulated output clock's p-p/RMS jitter and reference spur characteristics of the proposed all-digital MDLL (@2.4 GHz, N = 32).

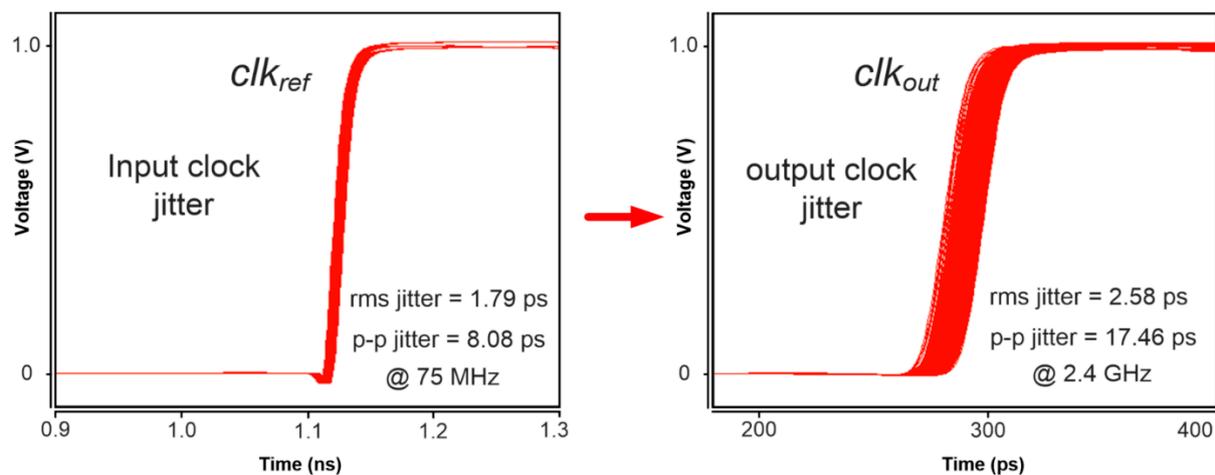


Figure 9. Simulated output clock's p-p jitter performance with an injected input clock noise (@2.4 GHz, N = 32).

Table 1. Digital MDLL performance summary and comparison.

Reference	[9]	[12]	[13]	[14]	This Work
Process and Supply	65 nm/1.2 V	28 nm/1.0 V	130 nm/1.2 V	65 nm/1.1 V	65 nm/1.0 V
Freq. range (GHz)	0.2–1.45	2.4	1.6	0.7–2.0	2.0–3.0
Output freq. (GHz)	1.4	2.4	1.6	2.0	2.4
Reference freq. (MHz)	87.5	75	50	500	75
Multiplication factor (N)	16	32	32	N/M = 8/2	32
Locking time (cycles)	N/A	>6000	N/A	40	15
p-p/RMS jitter (ps)	N/A	15.9/1.53	11.1/0.93	22/2.86	17.46/2.58
Power (mW)	8.0 @1.4 GHz	1.51 @2.4 GHz	9.2 @1.6 GHz	3.31 @1 GHz	3.3 @2.4 GHz
Active area (mm <sup>2</sup> )	0.054	0.024	0.76	0.019	0.043

#### 4. Conclusions

In this paper, we presented a new all-digital MDLL-based clock multiplier that features a cyclic Vernier TDC to achieve a fast lock capability of less than 15 reference clock cycles. This is the first fast-lock MDLL that utilizes a cyclic Vernier TDC to achieve both a wide phase detection range and high time resolution. In addition, the proposed offset-free TDC adopts a correlated double-sampling technique to improve jitter performance by eliminating mismatch and offset problems. The proposed MDLL utilizes DSM-based sequential tracking mode to achieve low output clock jitter characteristics. Implemented in a 65-nm 1.0-V CMOS process, the proposed MDLL generates a 2.4-GHz output clock with a frequency multiplication factor N of 32. The simulated peak-to-peak jitter is about 9.4 ps at 2.4 GHz, where the power consumption is only 3.3 mW (=1.375 mW/GHz). The proposed MDLL clock multiplier is suitable for use in high-speed burst mode serial link applications for chip-to-chip communications that require fast power-on/-off characteristics.

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**Conflicts of Interest:** The authors declare no conflict of interest.

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