Article

A Single Source Switched-Capacitor 13-Level Inverter with Triple Voltage Boosting and Reduced Component Count

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Abstract: A new triple voltage boosting switched-capacitor multilevel inverter (SCMLI) is presented in this paper. It can produce 13-level output voltage waveform by utilizing 12 switches, three diodes, three capacitors, and one DC source. The capacitor voltages are self-balanced as all the three capacitors present in the circuit are connected across the DC source to charge it to the desired voltage level for several instants in one fundamental cycle. A detailed comparative analysis is carried to show the advantages of the proposed topology in terms of the number of switches, number of capacitors, number of sources, total standing voltage (TSV), and boosting of the converter with the recently published 13-level topologies. The nearest level control (NLC)-based algorithm is used for generating switching signals for the IGBTs present in the circuit. The TSV of the proposed converter is 22. Experimental results are obtained for different loading conditions by using a laboratory hardware prototype to validate the simulation results. The efficiency of the proposed inverter is 97.2% for a 200 watt load.

Keywords: switched-capacitor; voltage boosting; multilevel inverter; nearest level control; modulation index

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1. Introduction

In recent times, multilevel inverters (MLIs) have been used as a potential solution for DC to AC conversion for various applications such as renewable energy conversion systems, high power drives, a high-voltage direct current (HVDC) transmission system, a distributed power generation system, etc. The main advantages of MLIs are lower dv/dt stress, higher operating voltage with lower rating devices, and near to sinusoidal output voltage, which in turn reduces total harmonic distortion (THD) and fault-tolerant capability [1–3]. Conventional MLIs such as the neutral point clamped (NPC) inverter, flying capacitor (FC) inverter, cascaded H-bridge (CHB) inverter, and modular multilevel converter (MMC) have replaced the conventional two-level inverter for medium and high voltage applications [4,5]. However, these conventional MLIs require more components and more complex control circuitry due to voltage balancing issues with an increased number of levels at the output voltage.

To overcome these issues, researchers have proposed a self-balanced switched-capacitor multilevel inverter (SCMLI), which can synthesize the desired voltage levels at the output using fewer components and reduced control complexity [6–12]. Several SCMLIs have been presented by researchers utilizing fewer components to realize the desired multilevel output voltage. A seven-level inverter is proposed in [13], which utilizes 10 switches and

one capacitor to produce 1.5 times voltage gain. Authors in [14] have used 12 switches and two capacitors to generate seven-level output voltage with increased voltage gain. Recently, several high gain SCMLIs were proposed which are capable of producing 13-level output voltage [15–21]. Four DC sources and 10 switches are used to produce 13-level output voltage in [18] with unity voltage gain. To improve the voltage gain and to reduce the number of sources, [22] uses only one DC source for producing 1.5 times voltage boosting, while [16] uses two sources to achieve dual voltage boosting with an increased number of switches. In [23] a high-voltage boosting of six is achieved, but the number of switches used in the circuit is twenty-nine with a total standing voltage (TSV) of 34. To reduce the number of switches, the authors in [19] used 19 switches for generating voltage boosting of six, but the TSV of the inverter circuit increased to 39. A detailed review on the recently published multilevel inverter topologies to find the most suitable applications with reduced device count is published in [7–12]. In the case of lower solar PV voltages, a high gain DC–DC converter along with multilevel inverter can be used to boost the PV voltage for obtaining desired output voltage for grid integration [24–26].

In this paper a triple voltage gain SCMLI topology is proposed with reduced component count and reduced TSV. The number of switches used in the proposed circuit is 12, with reduced TSV to 22. A simpler NLC based algorithm is used to generate switching pulses for IGBTs employed in the proposed circuit. The main objectives of the proposed topology are as follows;

- A 13-level output voltage is synthesized with 11 switches and one DC source.
- The proposed topology provides triple voltage boosting at the output.
- Total standing voltage (TSV) of the proposed topology has significantly reduced.
- Negative voltage levels are generated without using an H-bridge.
- All three capacitor voltages are self-balanced, hence control circuitry is simple.

The proposed circuit configuration, its working during different modes of operation, and charging–discharging states of the self-balanced capacitors are discussed in detail in Section 2. Capacitor selection criteria, power loss analysis, and switching algorithm are discussed in Section 3. Section 4 presents the comparative analysis of the proposed SCMLI with recently published 13-level MLIs in terms of component used, sources used, gain, and TSV. Section 5 presents the experimental results which were conducted to verify its feasibility and performance under different loading conditions. Finally, conclusions are presented in Section 6.

2. Proposed Switched-Capacitor Topology

The topology and output voltage waveform for the proposed 13-level SCMLI is shown in Figure 1. An elaborate discussion on the proposed SCMLI is presented as follows.

Figure 1. Proposed topology: (a) circuit diagram, (b) 13-level output voltage.

2.1. Circuit Analysis

Figure 1a shows the proposed SCMLI topology comprising one bidirectional switch (S_7), ten unidirectional switches ($S_1, S_2, S_3, S_4, S_5, S_6, S_8, S_9, S_{10}, S_{11}$), three diodes (D_1, D_2, D_3), three capacitors (C_1, C_2, C_3), and one DC source (V_{dc}). The 13-level output voltage waveform with triple voltage boosting is shown in Figure 1b. The capacitors are self-balanced and become charged to desired voltage levels for several instants during the fundamental cycle using the series-parallel voltage balancing principle. The capacitor C_1 is charged to V_{dc} , and the remaining two capacitors are charged to $V_{dc}/2$ to achieve 13 output voltage levels as $0, \pm V_{dc}/2, \pm V_{dc}, \pm 3V_{dc}/2, \pm 2V_{dc}, \pm 5V_{dc}/2, \pm 3V_{dc}$.

2.2. Description of Voltage Levels

Table 1 shows the switching states of the proposed SCMLI. It also shows the capacitors charging and discharging states. The conduction states of the proposed topology during the positive and negative half cycle are shown in Figure 2. Red lines represent the conduction path to the load, and green lines represent the capacitor charging path. The zero-voltage state is produced by switching on S_1, S_2, S_3 , while S_5 and S_9 are used for charging the circuit capacitors as shown in Figure 2a. Voltage level $+V_{dc}/2$ is obtained through the capacitor C_2 voltage, and at the same time, capacitor C_1 is charged to source voltage as shown in Figure 2b. Voltage level $+V_{dc}$ is obtained through capacitor C_2 and C_3 voltages, at the same time all the three capacitors are charged to their respective voltage values as shown in Figure 2c. Voltage level $+3V_{dc}/2$ is obtained through capacitor C_1 and C_2 voltages, as shown in Figure 2d. Voltage level $+2V_{dc}$ is obtained through capacitor C_1 voltage and V_{dc} , as shown in Figure 2e. Voltage levels $+5V_{dc}/2$ is obtained through capacitor C_1, C_2 voltages, and V_{dc} , as shown in Figure 2f. Voltage level $+3V_{dc}$ is obtained through capacitors C_1, C_2, C_3 voltages, and V_{dc} , as shown in Figure 2g. During the negative half-cycle, voltage level $-V_{dc}/2$ is obtained through capacitor C_3 voltage, as shown in Figure 2h. Voltage level $-V_{dc}$ is obtained through V_{dc} , as shown in Figure 2i. Voltage level $-3V_{dc}/2$ is obtained through V_{dc} and capacitor C_3 voltage, as shown in Figure 2j. Voltage level $-2V_{dc}$ is obtained through V_{dc} and capacitor C_1 voltage, as shown in Figure 2k. Voltage level $-5V_{dc}/2$ is obtained through V_{dc} , capacitor C_1 , and C_3 voltages, as shown in Figure 2l. Voltage level $-3V_{dc}$ is obtained through V_{dc} , capacitor C_1, C_2 , and C_3 voltages, as shown in Figure 2m.

Table 1. Switching table and capacitor states for the proposed 13-level inverter.

S_1	S_2	S_3	S_4	S_5	S_6	S_7	S_8	S_9	S_{10}	S_{11}	D_1	D_2	D_3	C_1	C_2	C_3	Output State
1	1	1	0	1	0	0	0	1	0	0	On	On	On	C	C	C	0
0	0	0	1	0	0	1	0	1	0	1	On	Off	Off	C	D	NC	$V_{dc}/2$
1	1	1	0	1	0	0	0	1	0	1	On	On	On	C	C	C	V_{dc}
1	0	0	0	0	0	1	0	1	0	1	On	Off	Off	C	D	NC	$3V_{dc}/2$
1	0	1	0	0	0	0	1	0	0	1	Off	Off	Off	D	NC	NC	$2V_{dc}$
1	0	0	0	0	0	1	1	0	0	1	Off	Off	Off	D	D	NC	$5V_{dc}/2$
1	0	0	0	0	1	0	1	0	0	1	Off	Off	Off	D	D	D	$3V_{dc}$
1	0	0	0	0	0	1	0	1	1	0	On	Off	Off	C	NC	D	$-V_{dc}/2$
0	1	1	1	1	0	0	0	1	0	0	On	On	On	C	C	C	$-V_{dc}$
0	0	0	1	0	0	1	0	1	1	0	On	Off	Off	C	NC	D	$-3V_{dc}/2$
0	0	0	1	0	1	0	1	0	1	0	Off	Off	Off	D	NC	NC	$-2V_{dc}$
0	0	0	1	0	0	1	1	0	1	0	Off	Off	Off	D	NC	D	$-5V_{dc}/2$
0	0	1	1	0	0	0	1	0	1	0	Off	Off	Off	D	D	D	$-3V_{dc}$

Figure 2. Conduction states of the proposed topology: (a) zero voltage level, (b–g) positive half-cycle (h–m) negative half-cycle.

3. System Design and Component Selection

In this section, capacitor design criteria, nearest-level control technique, and power loss analysis of the proposed converter are discussed.

3.1. Capacitor Design

The proposed SCMLI topology utilizes three capacitors C_1 , C_2 , and C_3 along with one DC source to generate the 13-level output voltage. All three capacitor voltages are self-balanced to the desired voltage level through the parallel connection of the source to the capacitor at different instants of time during the fundamental switching cycle. C_1 voltage is maintained equal to the source voltage (V_{dc}) while C_2 and C_3 are charged to half of the source voltage ($V_{dc}/2$). The charging and discharging durations for C_1 , C_2 , and C_3 are shown in Figure 3. The optimal value of capacitors can be calculated by considering the largest discharging cycle (LDC) of the capacitors and the type of loading current. The expression for the total discharge of capacitor C_1 during the LDC interval $[t_4, T/2 - t_4]$ is calculated as,

$$\Delta Q_{C1} = \int_{t_4}^{T/2-t_4} i_L(t) dt \quad (1)$$

Figure 3. Charging and discharging pattern of circuit capacitors C_1 , C_2 and C_3 .

The longest discharging interval of capacitor C_2 and C_3 are equal. Hence the expression for the total discharge of capacitor C_2 and C_3 during the longest discharging interval $[t_5, T/2 - t_5]$ can be expressed as,

$$\Delta Q_{C2,3} = \int_{t_5}^{T/2-t_5} i_L(t) dt \quad (2)$$

From Equations (1) and (2), the values of C_1 , C_2 and C_3 can be evaluated as,

$$C_1 = \frac{1}{\Delta V_{C1}} \int_{t_4}^{T/2-t_4} i_L(t) dt \quad (3)$$

$$C_2 = C_3 = \frac{1}{\Delta V_{C2,3}} \int_{t_5}^{T/2-t_5} i_L(t) dt \quad (4)$$

By considering ΔV_c equal to 10% of the corresponding capacitor voltage magnitude the corresponding values of ΔV_{C1} , ΔV_{C2} and ΔV_{C3} will be equal to 10 V, 5 V and 5 V respectively.

The values of t_1 , t_2 , t_3 , t_4 , t_5 and t_6 can be calculated as follows,

$$v(t) = V_m \sin \omega t \quad (5)$$

$$t = \sin^{-1} \frac{v(t)}{V_m} \quad (6)$$

By using Equation (6), t_1 , t_2 , t_3 , t_4 , t_5 and t_6 is calculated as 0.53 ms, 1.09 ms, 1.67 ms, 2.32 ms, 3.10 ms and 4.3 ms, respectively.

By considering a purely resistive load of 50Ω the load current can be expressed,

$$i_L(t) = I_m \sin \omega t \quad (7)$$

The output voltage peak is 300 V and load resistance is 50Ω then the peak value of load (I_m) will be 6 A.

The solution of Equation (3) for calculating the exact value of capacitor C_1 is given as,

$$C_1 = \frac{2 \times I_m \cos \omega t_4}{2\pi f \times \Delta V_{C1}} \quad (8)$$

The solution of Equation (4) for calculating the exact value of capacitor C_2 and C_3 is given as,

$$C_2 = C_3 = \frac{2 \times I_m \cos \omega t_5}{2\pi f \times \Delta V_{C2}} \quad (9)$$

After putting all corresponding values into Equation (8) the final solution of C_1 comes out to be 2880 μF . The nearest available value of the capacitor in the lab is 4700 μF , that is why it is chosen for experimental purposes. After putting all corresponding values in Equation (9) the final solution of C_1 and C_3 comes out to be 4383 μF . The nearest available value of capacitor in the lab is 4700 μF , that is why it is chosen for experimental purposes.

3.2. Power Loss Analysis

The power loss analysis of the proposed SCMLI provides capacitor charging loss, conduction loss, and switching loss occurring in the system. The conduction loss is due to the voltage drop across the switch when the load current flows through the circuit. The capacitor charging current is responsible for capacitor charging power loss.

3.2.1. Capacitor Charging Power Loss (P_{charging})

During the charging process of the capacitor, the charging current flows through the capacitor whose magnitude depends upon the voltage difference between the present value of the capacitor voltage and the desired value of the capacitor voltage. The power loss associated with capacitor charging is expressed as:

$$P_{\text{charging}} = \sum_{m=1}^3 \left(\frac{C_m}{2} \sum_{i=1}^N \Delta V_{cm,i}^2 \right) f_{\text{ref}} \quad (10)$$

where m is the number of capacitors present in the circuit, $\Delta V_{cm,i}$ is the capacitor voltage ripple in the i th interval cycle. ΔV_{cm} can be calculated as per the following equation,

$$\Delta V_{Cm} = \frac{1}{C_m} \int_{t_0}^{t_d} i_{C,m}(t) dt \quad (11)$$

where, duration $[t_0, t_d]$ is the largest discharging cycle, and i_c is the capacitor charging current.

3.2.2. Conduction Loss Due to Load Current

The conduction loss in an IGBT is caused due to load current flowing through it, which is expressed as,

$$P_{\text{cond_sw}} = V_{\text{on_sw}} \times I_{\text{on_sw}} + R_{\text{on_sw}} \times I_{\text{rms_sw}}^2 \quad (12)$$

where $V_{\text{on_sw}}$ and $R_{\text{on_sw}}$ are the forward voltage drop and on-state resistance of the switch. $I_{\text{av_sw}}$ and $I_{\text{rms_sw}}$ are the respective average and RMS values of switch current.

3.2.3. Switching Loss (P_{SW})

Switching loss occurs during the switching process of IGBTs. It is a turn-on and turn-off loss that can be calculated on the basis of overlap in switch voltage and current at the switching instants. The switching power loss during the turn-on process is computed as:

$$P_{\text{sw_on}} = \int_0^{t_{\text{on}}} v(t)i(t)dt \quad (13)$$

After solving Equation (8) $P_{\text{sw_on}}$ can be written as:

$$P_{\text{sw_on}} = \frac{V_{\text{std}} \times I_{\text{ton}}}{6} \quad (14)$$

Likewise, $P_{\text{sw_off}}$ can be written as:

$$P_{\text{sw_off}} = \frac{V_{\text{std}} \times I_{\text{toff}}}{6} \quad (15)$$

Likewise, V_{std} is the withstanding voltage of the switch, I_{ton} is the current flowing through the switch during turn-on time, I_{toff} is the current flowing through the switch during turn-off time, t_{on} and t_{off} is the turn-on and turn-off time of the switch, respectively.

The total switching power loss during one switching ON and OFF period is calculated as:

$$P_{\text{loss_sw,n}} = P_{\text{sw_on}} + P_{\text{sw_off}} \quad (16)$$

$$P_{\text{loss_sw,n}} = \frac{V_{\text{std,n}} \times I(t_{\text{on}} + t_{\text{off}})}{6} \quad (17)$$

3.3. Nearest Level Control (NLC)

Numerous modulation schemes have been tested and used for multilevel inverters. The nearest level control is a low switching frequency PWM technique in which there is less complexity in implementation for a higher number of levels. NLC is used here for the proposed topology to control the switches so that the desired output waveform is obtained. In NLC, the reference sinusoidal waveform is compared with the desired output waveform to obtain a sampled waveform. The waveform generated is then rounded off to the nearest level and compared according to the switching logic given in Table 1 to produce switching signals for the corresponding IGBTs. The comparison of reference sine wave with the desired output voltage levels is shown in Figure 4 [16]. The working principle of the NLC is shown in Figure 5.

Figure 4. Sampled reference signal.

Figure 5. Nearest level control logic for switching pulse generation.

4. Comparative Analysis

The comparative analysis of the proposed 13-level inverter with recently published 13-level topologies is carried out to show its advantages over other existing topologies. Table 2 shows the detailed comparative analysis on the basis of the number of switches (N_{sw}), number of diodes (N_d), number of DC sources (N_s), the total number of switching components (N_T), number of capacitors (N_c), voltage gain of the converter and TSV. The ratio of the number of levels and total switching components is analyzed and compared. The proposed topology requires a minimum number of switches as compared to other topologies, which have a gain of three or more, as presented in Table 2. The number of switches used is 10 in the case of [11], but the gain is only one. In [13], the number of switches is 10, but it also requires 10 diodes and five capacitors to produce a gain of six. In [9] the number of switches used is 14 with two DC sources to produce a gain of two. In [10] the number of switches is the same as [9] with a reduced number of sources, but the number of capacitors used has increased to four. References [12,14,15] produce higher gain but require more switches as compared to the proposed inverter. Moreover, the TSV of these topologies are higher than the proposed topology. The proposed inverter has the

lowest TSV amongst the compared topologies, which is only 22. Figure 6 shows the total standing voltage across individual switches and diodes.

Table 2. Comparative analysis of the proposed MLI with recent 13-level topologies.

13-Level MLI	N _{SW}	N _D	N _T	N _S	N _C	Gain	TSV($\times V_{dc}$)
[14]	14	0	14	2	2	2	39
[15]	14	0	14	1	4	1.5	40
[16]	10	0	10	4	0	1	32
[17]	19	0	19	1	5	6	39
[18]	10	10	20	1	5	6	59
[19]	29	5	34	1	5	6	34
Proposed	12	3	15	1	3	3	22

Figure 6. Total standing voltage of different switches and diodes.

5. Results and Discussion

In this section, simulation results and hardware results of the proposed 13-level inverter topology is presented for different loading conditions.

5.1. Simulation Results

The simulation results of the proposed topology are shown in Figure 7. Output voltage, capacitor C_1 voltage (V_{c1}), capacitor C_2 voltage (V_{c2}), capacitor C_3 voltage (V_{c3}) and load current waveform of the proposed 13-level inverter for the purely resistive load ($R = 50 \Omega$) is shown in Figure 7a. Figure 7b shows the output voltage V_{c1} , V_{c2} , V_{c3} and load current waveform for series connected R and L of load ($R = 50 \Omega$, $L = 120 \text{ mH}$). The effect of load change on load voltage, V_{c1} , V_{c2} , V_{c3} and load current is shown in Figure 7c, when load is changed from R to series connected R and L load. For varying purely resistive load as well as for series connected R and L load, the output voltage, V_{c1} , V_{c2} , V_{c3} and load current is shown in Figure 7d–g. The effect of change in modulation index on the number of levels at the output voltage is shown in Figure 7h. Simulation parameters are shown in Table 3.

Table 3. Simulation parameters.

Components	Values
DC Voltage Sources	100 V
Capacitors	4700 μF , 200 V, 2200 μF , 100 V
Load Resistance	30 Ω , 50 Ω , 100 Ω
Load Inductance	120 mH
Switching Frequency	50 Hz

Figure 7. Output voltage, capacitor C_1 voltage V_{c1} , capacitor C_2 voltage V_{c2} , capacitor C_3 voltage V_{c3} , and load current waveform of the proposed 13-level inverter for (a) resistive load of $50\ \Omega$ (b) for series connected R and L load ($R = 50\ \Omega$, $L = 120\text{ mH}$) (c) change in load from resistive ($R = 50\ \Omega$) to series connected R and L load ($R = 50\ \Omega$, $L = 120\text{ mH}$) (d) reduction in resistive load from $50\ \Omega$ to $100\ \Omega$ (e) increase in resistive load from $100\ \Omega$ to $50\ \Omega$ (f) increase in series connected R and L load from ($R = 50\ \Omega$, $L = 120\text{ mH}$) to ($R = 30\ \Omega$, $L = 120\text{ mH}$) (g) reduction in series connected R and L load from ($R = 30\ \Omega$, $L = 120\text{ mH}$) to ($R = 50\ \Omega$, $L = 120\text{ mH}$) (h) change in modulation from $M = 1.0$ to $M = 0.8$ to $M = 0.6$.

5.2. Hardware Results

The detailed performance analysis of the proposed 13-level inverter is experimentally validated by using a hardware prototype. It is made with twelve insulated gate bipolar transistor (IGBT) (FGA25N120) and TLP-250 based gate driver circuit for providing gating signals to individual IGBTs. Switching signals are provided using a fundamental frequency switching scheme i.e., nearest level control (NLC). The NLC scheme is implemented using a digital signal processor (DSP) (TMS320F28379D) for the proposed inverter. A FLUKE make 435-II power analyzer is used for measuring experimental % THD of the proposed MLI. Experimental parameters are shown in Table 4. The experiment setup is shown in Figure 8.

Table 4. Parameters for experimental validation.

Components	Values
DC Voltage Sources	25 V (V_{dc})
Capacitors	4700 μ F, 100 V, 2200 μ F, 100 V
Load Resistance	30 Ω , 50 Ω , 60 Ω
Load Inductance	50 mH
Output Frequency	50 Hz
Switching Frequency	50 Hz

Figure 8. Experiment setup.

The 13-level output voltage with a peak voltage of 75 volts and a current peak of 1.5 A for R (50 Ω) load is shown in Figure 9a. When the load is suddenly changed from 50 Ω to 100 Ω , the magnitude of load current changes from 1.5 A to 0.75 A as the load is reduced to half as shown in Figure 9b. Load is also changed from 120 Ω to 80 Ω to validate the performance of the proposed converter which is shown in Figure 9c.

The experimental results are also obtained for RL load, as shown in Figure 9d. By changing the modulation index (M) from 1 to 0.8, the number of levels in the output voltage reduces from 13 to 11 as shown in Figure 9e. If we keep on reducing the value of M, then the number of levels will decrease accordingly. The efficiency curve of the proposed topology is plotted for different loads, and it is also compared with the other 13-level topologies. Figure 9f shows the efficiency curve of the proposed converter for different loading conditions. It is 97.2% when the loading of the inverter is 200 W. It reduces slightly when the load is increased from 200 W to 1000 W. THD result of the generated output voltage is obtained using a FLUKE 435-II power quality analyzer. Figure 10a shows the generated 13-level output voltage waveform measured through a power quality analyzer. The measured %THD of the output voltage waveform is 4.9%. The %THD result is shown in Figure 10b.

Figure 9. Output voltage and current waveform of the proposed 13-level inverter: (a) R load, (b) during load resistance changed from $50\ \Omega$ to $100\ \Omega$, (c) during load resistance changed from $120\ \Omega$ to $80\ \Omega$, (d) with RL load, (e) change in modulation from $M = 1.0$ to $M = 0.8$, (f) efficiency comparison at different loading conditions.

Figure 10. Output voltage and current waveform (a) 13-level voltage and current (b) %THD of the generated output voltage.

6. Conclusions

In this paper, a 13-level switched-capacitor MLI using one bidirectional switch and 10 unidirectional switches, one DC source, three diodes, and three capacitors is proposed and analyzed in detail. The proposed MLI possesses inherent self-voltage balancing capability, which eliminates the need for a complex control circuit for capacitor voltage balancing. A detailed simulation analysis of the proposed 13-level converter is undertaken using MATLAB software. Performance of the proposed MLI is validated experimentally with R and RL loads using the developed laboratory prototype, and a satisfactory operation is observed. It is also tested for different types of loading condition along with sudden load change and change in modulation index (M). TSV of the proposed converter is 22, which is significantly less than other existing topologies. The gain of the proposed converter is three with reduced switch count and reduced TSV. The output voltage THD of the proposed inverter is 4.9% which is within limits as per IEEE-519 standard. The maximum efficiency is 97.2% for a 200 W load.

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