



Article Towards Realization of a Low-Voltage Class-AB VCII with High Current Drive Capability

Leila Safari¹, Gianluca Barile¹, Vincenzo Stornelli^{1,*}, Shahram Minaei² and Giuseppe Ferri¹

- ¹ Department of Industrial and Information Engineering, University of L'Aquila, 67100 L'Aquila, Italy; leilasafari@yahoo.com (L.S.); gianluca.barile@univaq.it (G.B.); giuseppe.ferri@univaq.it (G.F.)
- ² Department of Electrical and Electronics Engineering, Dogus University, Umraniye, Istanbul 34775, Turkey; sminaei@dogus.edu.tr
- * Correspondence: vincenzo.stornelli@univaq.it

Abstract: In this paper, the implementation of a low-voltage class AB second generation voltage conveyor (VCII) with high current drive capability is presented. Simple realization and good overall performance are the main features of the proposed circuit. Proper solutions and techniques were used to achieve high signal swing and high linearity at Y, X and Z ports of VCII as well as low-voltage operation. The operation of the proposed VCII was verified through SPICE simulations based on TSMC 0.18 µm CMOS technology parameters and a supply voltage of ± 0.9 V. The small signal impedance values were 973 Ω , 120 k Ω and 217 Ω at Y, X and Z ports, respectively. The maximum current at the X port was ± 10 mA with maximum total harmonic distortion (THD) of 2.4% at a frequency of 1 MHz. Considering a bias current (I_B) of 29 µA and output current at the X port. The voltage swing at the Z port was (-0.4, 0.4) V. The THD value at the Z port for an input signal with 0.8 V peak-to-peak value and frequency of 1 MHz was 3.9%. The total power consumption was 0.393 µW.

Keywords: CCII; class-AB VCII; high drive; low voltage; VCII; voltage conveyor

1. Introduction

Since the introduction of current-mode signal processing, second generation current conveyors (CCII) [1] have been employed in various circuits, such as inductance simulators [2,3], filters [4–6], oscillators [7–9], and instrumentation amplifiers [10–12] as possible substitutes for conventional operational amplifiers (OAs). It is generally known that the OA-based circuits suffer from many disadvantages, mainly low frequency performance resulting from the limited gain-bandwidth product of OAs. Actually, the introduction of CCII has created a valid alternative to OAs in analog circuit design area, and circuits employing CCIIs offer high frequency operation and simplicity. Despite these benefits, the main weakness of CCII is its output signal in the form of current at the high impedance Z port of CCII. Therefore, CCII is not a good block for applications requiring output signal in the form of voltage.

In [13–15], the concept of dual topology of CCII, called a second generation voltage conveyor (VCII), was introduced. For this duality, VCII shows the additional advantage of providing output signal in the form of voltage. VCII has a low impedance current input port (Y), a high impedance current output port (X) and a low impedance voltage output port (Z). These impedance levels at Y, X and Z ports are of great importance in both voltage based and current based applications. In [16], the authors showed that most of the analog signal processing circuits are realizable by VCII with the advantage of providing output voltage signal at the low impedance Z port of VCII. In [17], a comparison between OA-based circuits and VCII-based circuits was drawn, showing that the problem of the cross-talk effect among inputs in a conventional OA-based non-inverting summing amplifier can be



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Copyright: © 2021 by the authors. Licensee MDPI, Basel, Switzerland. This article is an open access article distributed under the terms and conditions of the Creative Commons Attribution (CC BY) license (https:// creativecommons.org/licenses/by/ 4.0/). cancelled out using VCII. Literature survey shows the possibility of realizing various VCIIbased analog circuits such as filters, integrators, differentiators, rectifiers, and impedance simulators [16–27].

As VCII design is a new research area, the VCII implementations reported up to this point lack the maximum efficiency. Analyzing the previously reported VCII circuits, it appears that most of them [16–24] are designed in class A, which has limited current drive capability at the X port. Due to high power consumption and poor current drive capability of circuits including class A VCIIs, they are unsuitable for low power applications and off-chip loads [28], while the class AB VCII with high current drive capability finds wide application as an integrated circuit front-end block. However, designing circuits with high current drive capability under low supply voltage restriction is a very challenging task. For example, to drive 10 mA in 0.18 µm technology with an aspect ratio of 100 µm/0.5 µm, a gate-source voltage equal to 2 V must be provided [29] for the PMOS transistor, while the maximum allowed supply voltage is 1.8 V. Distortion due to the transistor channel modulation effect (λ effect) is another serious issue [29] in fine technologies. It is worth mentioning that the conventional cascode structures that were conventionally used to mitigate the channel length modulation effect are not practical, due to the limited allowed supply voltage.

Literature survey shows that there are very few VCII circuits designed in class AB [25–27,30]; however, all of them suffer from poor current drive capability. In [25], a flipped voltage follower (FVF)-based VCII circuit was presented, which can provide an output current up to ± 2 mA. In the VCII circuit reported in [26], the maximum current at X terminal is limited to ± 0.5 mA. The VCII circuit presented in [27] is optimized for the minimum number of transistors. Its current drive capability is limited to ± 1.065 mA. The class AB VCII reported in [30] is based on the simple translinear principle. Unfortunately, its current drive capability is only ± 1.22 mA.

In this paper we propose a VCII with high current drive capability at the X terminal. The circuit operates in class AB for increasing current swing and reducing power consumption. The current splitting method used previously in current output stages was employed to increase the linearity of output voltage at the Z port and to obtain a high current drive capability at the X port. Due to low voltage restrictions, cascode structures are avoided and the required high linearity in the X port output current is maintained using simple controlling circuits by means of three transistors. The proposed circuit is able to drive a maximum current of ± 10 mA at the X port at ± 0.9 V supply with a power consumption of 382 μ W.

The organization of this paper is as follows. In Section II, details of VCII internal circuit design are given. The existing challenges and design considerations to increase current swing are also discussed in this section. Simulation results are presented in Section III and finally Section IV concludes the paper.

2. Class AB VCII Realization

The internal structure of VCII is composed of a current buffer (CB) and a voltage buffer (VB) as shown in Figure 1. Y is a low impedance current input port. The input current to the Y port is transferred to a high impedance X port through CB. In practice finite impedance is connected to the X port to convert the conveyed current into the voltage. Then, the voltage produced at the X port is buffered to the low impedance Z port by VB. The matrix operation of a VCII is expressed as:

$$\begin{bmatrix} I_X \\ V_Z \\ V_Y \end{bmatrix} = \begin{bmatrix} \beta 00 \\ 0\alpha 0 \\ 000 \end{bmatrix} \begin{bmatrix} I_Y \\ V_X \\ I_Z \end{bmatrix},$$
(1)

where α and β are non-ideal VB and CB gains, respectively. Other requirements are high current drive capability in Y and X ports, low THD for the current transferred from Y to X ports, and high voltage swing at the Z port. In all applications reported in [16–26], both

CB and VB sections are not included in the negative feedback loop, and as a result, overall performance is determined by VCII linearity and port impedances.



Figure 1. Internal structure of VCII.

In this Section, design considerations of a high drive class AB VCII under low supply voltage are discussed. The analysis is twofold, where the first of which is the CB section.

Figure 2 shows a conventional class AB current buffer [30]. The translinear loop created by M_1-M_4 sets the value of the input voltage at zero for $I_{in} = 0$. Input current is transferred to output node through simple current mirrors (M5-M6, M7-M8). Input impedance is approximately $r_{in} \cong (gm_2) - 1//(gm_4) - 1$. The required minimum supply voltage is:

$$V_{dd} - V_{ss} = Vsg_{M5} + Vds(sat)_{M2} + Vsd(sat)_{M4} + Vgs_{M7}$$
, (2)

where Vgs, Vsg, Vds and Vsd are gate-source voltage, source-gate voltage, drain-source voltage, and source-drain voltage, respectively, of the related transistor. In Equation (2), Vsg_{M5} and Vgs_{M7} are very large for high drain currents. For instance, as mentioned in the introduction, in 0.18 μ m CMOS technology, by setting the aspect ratio of M5 at 100 μ m/0.5 μ m, Vsg_{M5} is approximately 2 V for a drain source current of 10 mA, which exceeds the allowed supply voltage of technology [29]. Evidently, for larger currents, the gate-source voltage is even higher. In the saturation region, the minimum value of the drain-source voltage is Vds(sat) = Vgs – Vth; therefore, in Equation (2), the Vgs terms play a more important role in increasing supply voltage, so if Vgs is replaced with Vds, supply voltage is reduced significantly.



Figure 2. Conventional class AB current buffer [30].

Another problem associated with the conventional class AB current buffer of Figure 2 is harmonic distortion caused by the channel length modulation effect or the λ effect of M₆ and M₈. In other words, in the upper side, as the drain-source voltage of mirroring

transistors M_5 and M_6 are not equal, the current transferred to the output node is not exactly equal to the input current according to:

$$Ids_{M6} = \frac{\mu C_{ox} W_6}{2L_6} (Vsg_{M6} - |Vth_{M6}|)^2 (1 + \lambda Vsd_{M6}),$$
(3)

$$Ids_{M5} = \frac{\mu C_{ox} W_5}{2L_5} (Vsg_{M5} - |Vth_{M5}|)^2 (1 + \lambda Vsd_{M5}),$$
(4)

where μ , C_{ox} , W_i and L_i (for I = 5–6) are the carrier mobility, gate oxide capacitance, channel width and channel length, respectively, of the related transistor. The same holds in the lower side of the circuit. The problems of large Vgs for M_5 and M_7 along with the nonlinearity caused by the non-zero value of λ are eliminated in the topology shown in Figure 3, where the minimum required supply voltage is reduced to:

$$V_{dd} - V_{ss} = V_{sd}(sat)_{M5} + V_{ds}(sat)_{M2} + V_{sd}(sat)_{M4} + V_{ds}(sat)_{M7}$$
 (5)



Figure 3. Proposed high drive class AB CB.

To increase the current drive capability of CB, the required voltage of M_2 , M_4 , M_5 and M_7 must be reduced, through introduction of M_9 and M_{10} splitting transistors [29]. Transistor M_9 in the upper half has an aspect ratio m times larger than the aspect ratio of M_5 . Similarly, in the lower half, M_{10} has an aspect ratio m times larger than that of M_7 . Therefore, a large part of the input current is provided by splitting transistors M_9 and M_{10} . As a result, the currents in M_5 and M_7 are reduced and consequently their Vds is reduced, resulting in lower required supply voltage. Therefore, considering Vds(sat) = Vgs – Vth and $\lambda \cong 0$, Equation (5) can also be expressed in terms of drain-source currents as:

$$V_{dd} - V_{ss} \approx \sqrt{\frac{2Ids_{M5}}{K_5}} + \sqrt{\frac{2Ids_{M2}}{K_2}} + \sqrt{\frac{2Ids_{M4}}{K_4}} + \sqrt{\frac{2Ids_{M7}}{K_7}},$$
 (6a)

or:

$$V_{dd} - V_{ss} \approx \sqrt{\frac{2I_{in}}{(1+m)K_5}} + \sqrt{\frac{2I_{in}}{(1+m)K_2}} + \sqrt{\frac{2I_{in}}{(1+m)K_4}} + \sqrt{\frac{2I_{in}}{(1+m)K_7}}, \qquad (6b)$$

with the usual meaning of symbols for $K_i = \mu C_{ox}(W_i/L_i)$ for i = 2, 4, 5, 7.

From Equation (6a,b), the splitting transistors results in a significant decrease of the supply voltage. In addition, the negative feedback loop provided by the splitting transistors at the input node reduces the Y port impedance by a factor of (1 + m) as follows:

$$\mathbf{r}_{\rm in} \cong \frac{\mathbf{gm}_2^{-1} \| \mathbf{gm}_4^{-1}}{(1+{\rm m})},\tag{7}$$

The channel length modulation effect is reduced using two simple controlling circuitries [31]. In the upper half, the drain-source voltages of M_5 and M_6 are kept equal by a negative feedback loop established by M_{C1} - M_{C2} . Similarly, in the lower side of the circuit, the drain-source voltages of M_7 and M_8 are kept equal by M_{C3} - M_{C4} . Here, M_{L1} and M_{L2} are simple level shifters used to provide appropriate bias voltage at drain nodes of M_{C2} and M_{C4} , respectively. Current sources I_{B2} - I_{B7} are used to bias transistors in controlling circuitries. In the lower half, the drain current of M_{C3} is fixed by the I_{B5} current source. Therefore, its gate-source voltage is a fixed value, and it transfers V_X to the gate of M_{C4} . Any difference between V_X and the drain voltage of M_7 is compared by M_{C4} and the appropriate voltage is produced at its drain node, which is applied to the gate of mirroring transistors M_7-M_8 , and M_{10} by M_{L2} . To elaborate the operation of controlling circuitries of the lower half, let us consider the case that V_X is reduced. Due to the channel length modulation effect, a reduction in V_X tends to reduce the M_{10} drain current. In this case, the gate voltage of M_{C4} is also reduced, which results in an increase in its drain voltage, which is applied to the gate of M7-M8, and M10 through ML2. As a result, the drain current of M_{10} is kept constant regardless of V_X variation.

Similarly, if V_{out} is increased, the gate voltage of M_7 – M_8 , and M_{10} is reduced to avoid any increase in output current.

Therefore, any variation of the M_{10} drain current due to variations in V_X is compensated for. A similar procedure occurs in the upper half by M_{C1} – M_{C2} transistors. As the λ effects of M_6 and M_8 are compensated for by control circuitry, we can ignore their effect on output impedance and therefore, the impedance at the output node is approximately found as:

$$r_{\text{out}} \approx (r_{\text{O}_{\text{IB2}}} + \frac{1}{gm_{\text{MC1}}}) \| (r_{\text{O}_{\text{IB5}}} + \frac{1}{gm_{\text{MC3}}}) \| (\frac{1}{r_{\text{O}_{\text{M6}}}} - \frac{gm_{\text{M6}}}{gm_{\text{M5}}r_{\text{O}_{\text{M5}}}})^{-1} \| (\frac{1}{r_{\text{O}_{\text{M8}}}} - \frac{gm_{\text{M8}}}{gm_{\text{M7}}r_{\text{O}_{\text{M7}}}})^{-1}$$
(8)

To avoid complications, Equation (8) is derived by the assumption that the open loop gain of the λ effect cancelling circuit is infinite. However, in practice, due to its limited gain, it is expected that the impedance at the X port is smaller than Equation (8).

In Figure 3, in the λ effect cancelling circuit at the upper side, there are four poles located at the source of M_{C2} , gate of M_{C1} , source of M_{L1} and drain of M_{C2} . Due to low impedance values at the source of M_{C2} , gate of M_{C1} and source of M_{L1} , their related poles are smaller than the pole related to the drain of M_{C2} . To grantee frequency stability, a compensation capacitor can be added to the drain of M_{C2} to make this pole much smaller than the other poles. Therefore, the negative feedback loop operates as a single pole system and its stability is guaranteed. The same explanations hold for the lower side where a compensation capacitor can be added to the drain of M_{C4} to make the related pole the dominant pole of the lower side.

Starting from Figure 2, we can isolate a conventional Class AB voltage buffer [30] as shown in Figure 4. In the positive cycle, the input voltage is transferred to the output through $M_{11}-M_{12}$ transistors. It follows that in this case we have:

$$V_{out} = V_{in} + Vgs_{M11} - Vgs_{M12},$$

$$\tag{9}$$



Figure 4. Conventional class AB voltage buffer [30].

From Equation (9), to have $V_{out} = V_{in}$, gate-source voltages of M_{11} and M_{12} must be kept equal. However, the drain-source current of M_{11} is a constant value of I_{B8} , while that of M_{12} is not constant and is equal to I_L . In terms of drain currents, Equation (9) can be expressed as:

$$V_{out} = V_{in} + \sqrt{\frac{2Ids_{M11}}{K_{11}}} + V_{thM11} - \sqrt{\frac{2Ids_{M12}}{K_{12}}} - V_{thM12},$$
 (10)

As $I_{dsM12} = I_L + I_{B8}$, by assuming $I_{B8} \ll I_L$, and $V_{thM11} = V_{thM12}$, Equation (10) is:

$$V_{out} \approx V_{in} + \sqrt{\frac{2I_{B8}}{K_{11}}} - \sqrt{\frac{2I_L}{K_{12}}},$$
 (11)

Inserting $I_L = V_{out}/R_L$, Equation (11) becomes:

$$V_{out} \approx V_{in} + \sqrt{\frac{2I_{B2}}{K_{11}}} - \sqrt{\frac{2V_{out}}{K_{12}R_L}},$$
 (12)

One effective method to reduce the non-linearity of V_{out} is to keep the third term in Equations (11) and (12) as small as possible. This can be realized by minimizing the

variation in the drain current of M_{12} . Another disadvantage of the conventional class AB voltage buffer of Figure 4 is its high output impedance, which is equal to:

$$r_{out} \approx gm_{12}^{-1} \|gm_{14}^{-1},$$
 (13)

Figure 5 shows the modified version of the conventional class AB voltage buffer of Figure 4 where the current splitting method reported in [29] is used to keep the Ids_{M12} variation as small as possible. In the upper side, the current mirror made of M_{15} – M_{16} is added and the drain of M_{16} is connected to the input node. By setting the aspect ratio of M_{16} n times larger than that of M_{15} , we have:

$$Ids_{M16} = nIds_{M15} = nIds_{M12}, \tag{14}$$



Figure 5. Proposed class AB voltage buffer with current splitting method.

By assuming a positive cycle of the input signal, for I_L we have:

$$I_{L} = Ids_{M12} + Ids_{M16}, \tag{15}$$

Inserting Equation (14) into Equation (15) we have:

$$I_L = (1+n)Ids_{M12}$$
, (16)

Assuming $Vth_{M11} = Vth_{M12}$, from Equations (16) and (10), we have:

$$V_{out} \approx V_{in} + \sqrt{\frac{2I_{B8}}{K_{11}}} - \sqrt{\frac{2V_{out}}{K_{12}R_L(1+n)}}$$
, (17)

Comparing Equations (12) and (17), we show that by applying the current splitting method, the third term in Equation (12), which is the main cause of non-linearity is reduced by a factor of (1 + n). Similarly, the current mirror made of M_{17} – M_{18} has been added to the lower side to reduce current variation in M_{14} for the negative cycle of the input voltage. Another advantage of applying the current splitting method is to reduce the output impedance by (1 + n) times:

$$r_{out} \approx \frac{gm_{12}^{-1} \|gm_{14}^{-1}}{(1+n)},$$
(18)

In Figure 5, in the upper half, there is only one dominant pole at the gate of M_{15} . In the lower half, the dominant pole is at the gate of M_{17} . In fact, the aspect ratio of M_{18} is much larger (in this design 200 times) than the aspect ratio of M_{14} and M_{17} . Therefore, at the gate of M_{18} , the value of parasitic capacitance is large, which makes the dominant pole of the lower half. Similarly, the large capacitance at the gate of M_{16} makes the dominant pole of the upper half. Consequently, the negative feedback loops at the voltage buffer section operate as a single pole system, which is naturally stable, and no compensation capacitor is required.

The complete implementation of the high drive class AB VCII realization is shown in Figure 6, which is constructed by series connection of the CB of Figure 3 and the VB of Figure 5.



Figure 6. A complete schematic of the proposed class AB high drive VCII.

3. Simulation Results

The proposed circuit of Figure 6 was simulated in TSMC 0.18 μ m CMOS technology [32] with a supply voltage of ± 0.9 V. Transistor aspect ratios are reported in Table 1. The values of m and n were set to 10 and 200. For frequency performance analysis, a load of 50 Ω and 5 pF was connected to the X node. The Z node was connected to 10 k Ω . For frequency stability, 5 pF compensation capacitors were added between the drain and gate of M_{C2} and M_{C4}. All bias current sources (I_{B1} = 1.5 μ A, I_{B2,3,4,5,6,7} = 10 μ A, I_{B8} = 0.5 μ A) were implemented with simple current mirrors with an aspect ratio of 9 μ m/0.9 μ m. As the current splitting section in the voltage buffer has a gain of 200, we selected a low bias current of 0.5 μ A for this section. The current splitting section in the current buffer has a gain of 10 and the output branch transistors gain is 11, so we selected 1.5 μ A for this section. This was done to reduce overall power consumption. The λ effect cancelling circuit operates in class A, so we selected 10 μ A for this section.

Transistor	W (μm)/L (μm)	Transistor	W (μm)/L (μm)
M ₁ , M ₂	36/0.36	ML1, ML2	0.9/0.45
$M_3 - M_4$	72/0.36	MC1	18/0.9
M_5	72/0.9	MC2	0.81/0.9
M_6	792/0.9	MC3	0.9/0.9
M ₇	36/0.45	MC4	9/0.9
M_8	396/0.45	M13-M14	4.5/0.9
M9	720/0.9	M15, M17	0.18/0.36
M ₁₀	360/0.45	M16, M18	36/0.36
$M_{11}-M_{12}$	3.6/0.18		

Table 1. Aspect ratio of the used transistors.

The variation of V_X by I_X in the DC domain was also examined, which is shown in Figure 7. From Figure 7, the value of r_X is about 120.6 k Ω . The frequency performance of r_Y , r_X and r_Z are also shown in Figure 8. The calculated and simulated values of the transistors' small signal parameters are reported in Table 2. Using these values, the simulation and calculation results for r_x , r_Y and r_Z are summarized in Table 3. As it is seen, there is good agreement between the simulation and calculation results for r_x and r_z . The achieved result for r_X is 120 k Ω for simulation and 158 k Ω for calculation. The reason for this difference is that in calculations it is assumed that the open loop gain of the λ effect cancelling circuit is assumed as infinite. However, in practice, due to its limited gain, the value of impedance at the X port is lower than expected.

Table 2. Transistors calculated and simulated small signal parameters used in the formulas.

Transistor	Parameter	Calculated	Simulation
MIB2	gm	208 μA/V	161 μA/V
	ro	740 kΩ	641 kΩ
	Vsat	0.096 V	0.08 V
MIB5	gm	129 μA/V	107 μΑ/V
	ro	1.25 MΩ	1 ΜΩ
	Vsat	0.154 V	0.159 V
MC1	gm	181 μA/V	130 μΑ/V
	ro	1.2 MΩ	1.25 ΜΩ
	Vsat	0.1 V	0.109 V
MC3	gm	207 μA/V	182 μA/V
	ro	740 kΩ	641 kΩ
	Vsat	0.096 V	0.09 V
M2	gm	48 μA/V	72 μA/V
	ro	1.7 MΩ	1.02 MΩ
	Vsat	0.012 V	0.04 V
M4	gm	38.4 μA/V	35 μA/V
	ro	3 MΩ	4.3 MΩ
	Vsat	0.014 V	0.04 V
M8	gm	0.506 μA/V	0.659 μA/V
	ro	298 kΩ	175 kΩ
	Vsat	0.022 V	0.04 V
M6	gm	0.500 μA/V	0.571 μA/V
	ro	235 kΩ	390 kΩ
	Vsat	0.037 V	0.05 V
M12	gm	16.6 μΑ/V	11.8 μA/V
	ro	9.2 ΜΩ	8.8 MΩ
	Vsat	0.033 V	0.047 V
M14	gm	13.3 μA/V	9.7 μA/V
	ro	18.8 MΩ	19 MΩ
	Vsat	0.047 V	0.06 V







Figure 8. Frequency performance of (a) $r_{\rm Y}$ (b) $r_{\rm X}$ and (c) $r_{\rm Z}.$

Parameter	Calculated	Simulated
r _Z (Equation (18))	167 Ω	217 Ω
r_{Y} (Equation (7))	$1.15 \text{ k}\Omega$	973 Ω
r_X (Equation (8))	$158 \text{ k}\Omega$	120 kΩ

Table 3. The calculated simulated values of r_Y , r_X and r_Z .

To examine the frequency performance of the circuit, the X port was connected to 50 Ω resistors and a 5 pF capacitor, while the Z port was connected to a 10 k Ω resistor. The frequency performance of β and α is shown in Figure 9. For β , the DC value and -3dBfrequency were 0.993 and 11 MHz, respectively. For α , the DC value and -3 dB frequency are 0.953 and 50 MHz, respectively. The circuit power consumption was 393 μ W. The DC transfer characteristic between I_Y and I_X is shown in Figure 10. As it is seen, there is good linearity for current transfer when I_Y is varied from -10 mA to +10 mA. The linearity of voltage transfer between X and Z nodes was investigated by applying a DC voltage to the X node and connecting the Z node to a load of 10 k Ω . To compare with theory, Equation (17) was also calculated. The results of the calculations, which are shown in Figure 11, show good agreement between theory and simulations. The limit of voltage range in node X is -0.4 V to +0.4 V. Figure 10 shows a good linearity between X and Z nodes in the range of -0.4 V to +0.4 V. The maximum error was -70 mV, which occurred at 0.4 V. Figure 12 shows the THD of I_X for various amplitudes of input current at 1 kHz and 1 MHz frequencies. Favorably, the value of THD for I_X did not exceed 2.4%. In fact, by increasing the frequency, the gain of the λ effect cancelling circuit reduces, so its effect starts decreasing at higher frequencies. As it is shown, the value of THD at 1 kHz is larger than 1 MHz. Figure 13 shows the resulting THD of V_z for different amplitudes of input voltage. In this case, THD remained below 3.9%. Monte-Carlo simulations in 100 runs for mismatch of 3% between V_{th} and t_{ox} of all transistors are reported in Table 4. In addition, corner case simulation results are summarized in Table 5.



Figure 9. Frequency performance of the $\beta = (I_X/I_Y)$ and $\alpha = (Vz/Vx)$.



Figure 10. DC transfer characteristic between I_X and I_Y .



Figure 11. DC transfer characteristic between V_Z and V_X .



Figure 12. THD for different amplitudes of I_X at frequencies of 1 kHz and 1 MHz.



Figure 13. THD for different amplitudes of V_Z at frequencies of 1 kHz and 1 MHz.

Parameter	Maximum	Minimum	Mean
rY(Ω)	2.35k	233	745
rX(kΩ)	395	40	123
$rZ(\Omega)$	347	143	224.3
β	1.47	0.651	1.02
α	0.938	0.920	0.930
Ix THD at 10 mA and 1 MHz(%)	3.27	1.43	2.46
Vz THD at 0.8 V p-to-p and 1 MHz(%)	8	2	3.53

Table 4. Monte-Carlo Simulation Results.

Table 5. PVT Simulation results.

Parameter	Р			V (Vdd-Vss)		T (°C)			
	FF	SF	FS	SS	$\pm 0.99 \ V$	$\pm 0.81 \text{ V}$	-20	25	80
rY(Ω)	956	965	964	972	894	1 k	804	959	1100
rX(kΩ)	113.7	113.8	114	113.88	98	129.4	93.2	113	147
$rZ(\Omega)$	205	212	213	217	195	233	182.8	211.4	248.1
β	0.993	0.990	0.993	0.992	0.992	0.993	0.9924	0.9971	0.9927
α	0.933	0.952	0.932	0.931	0.935	0.928	0.934	0.932	0.929
THD at I _{in} =									
1 mA and	2.44	2.31	2.24	2.36	2.37	2.3	2.36	2.43	2.48
1 MHz (%)									
THD at $Vx =$									
0.8 V p-p and	3.04	2.46	2.4	3.4	1.59	7.6	3.52	3.37	4.2
1 MHz (%)									

The application of the proposed VCII as a transimpedance amplifier [17] is examined in Figure 14a, while the X port is connected to a load of 100 Ω . The frequency performance is shown in Figure 14b, which shows a gain of 16.5 dB and BW of 1 MHz.



(b)

Figure 14. Application of VCII as a transimpedance amplifier: (**a**) schematic; (**b**) frequency performance.

Comparison summary of the proposed VCII and other works is shown in Table 6. As it is seen, the proposed circuit provides the largest current drive capability ever reported. For a 29 μ A bias current at M₆ and M₈, the circuit can provide ± 10 mA to the X port, which is 345 times larger than the used bias current.

Table 6. Comparison between proposed circuit and some other previously reported VCII topologies.

	Proposed	[16]	[18]	[21]	[25]	[26]	[27]	[29]
Class	AB	А	А	А	А	AB	А	AB
$\alpha(DC, f)_{-3dB}$	(0.953, 50 MHz)	(0.997, 217 MHz)	(0.995, 340 MHz)	(1.017, 330 kHz)	(0.992, 220 MHz)	(0.972, 55 MHz)	(0.968, 2.57 GHz) * (1, 1.92 GHz) **	(1, 100 GHz)
$\beta(DC, f)_{-3dB}$	(0.993, 11 MHz)	(0.998, 200 MHz)	(0.996, 14.6 MHz)	(1.035–108 dB 26 kHz–37 kHz)	(0.978, 22.4 MHz)	(0.996, 165 MHz)	(0.988, 794 MHz)	(0.987, 169.7 MHz)
Max I _X	10 mA	17 µA	40 µA	100 nA	2 mA	0.5 mA	1.065 mA	1.22 mA
THD at I _X	1 2.40%	² 0.10%	NA	NA	³ 3.36%	³ 1.10%	NA	⁴ 1%
r _x	120 kΩ	1.2 MΩ	$0.8 \text{ M}\Omega$	22 GΩ	370 kΩ	522 kΩ	74.28 kΩ	273.8 kΩ
ry	973 Ω	6.7 Ω	49 Ω	27 kΩ	2 mΩ	23 Ω	930 Ω	1.88 kΩ
rZ	217Ω	0.7 Ω	79 Ω	27 kΩ	2 mΩ	160 Ω	705 Ω * 35 Ω **	1.75 kΩ
Vdd-Vss	$\pm 0.9 \text{ V}$	$\pm 1.65 \text{ V}$	$\pm 1.65 \text{ V}$	±0.3 V	$\pm 1.65 \text{ V}$	$\pm 0.9 \text{ V}$	$\pm 0.9 \text{ V}$	±0.9 V
P _d	0.393 mW	0.330 mW	0.7 mW	96 nW	0.320 mW	0.120 mW	0.622 mW * 0.664 mW **	0.179 mW
THD at V _Z	⁵ 3.90%	NA	NA	NA	⁶ 2.48%	7 2.40%	NA	⁸ 1%
#transistors	38	20	16	20	25	37	6 * 11 **	12
Tech.	0.18 μm	0.35 μm	0.35 μm	0.18 µm	0.35 μm	0.15 µm	0.18 µm	0.18 µm

¹ Iy = 10 mAp-p @1 MHz, ² Iy = 20 μAp-p @1 MHz ³ Iy = 1 mA p-p @1 MHz ⁴ 2.44 mAp-p@1 MHz ⁵ 0.8 Vp-p @1 MHz ⁶ 1 Vp-p @1 MHz 7 1.6 Vp-p @1 MHz ⁸ 1.78 Vp-p @1 MHz, * First circuit ** Second circuit.

4. Conclusions

In this paper, the design of a class AB high drive VCII was presented. The current splitting method was used to reduce the required gate-source voltage of transistors in both CB and VB sections, resulting in reduced supply voltage and improved linearity in VB. This also led to reduced impedance for Y and Z ports. High linearity in the CB section was also provided by applying controlling circuitries, which eliminated the channel length modulation effect of mirroring transistors. As a result, high impedance at the X port was also provided. For low voltage operation, cascode current mirrors were avoided. In addition, in all branches, the maximum number of transistors between V_{DD} and V_{SS} was only four, resulting in low voltage operation.

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