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A Chopper-Embedded BGR Composite Noise Reduction Circuit for Clock Generator

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Abstract: A chopper-embedded bandgap reference (BGR) scheme is presented using 0.18 μm CMOS technology for low-frequency noise suppression in the clock generator application. As biasing circuitry produces significant flicker noise, along with thermal noise from passive components, the proposed low-noise chopper-stabilized BGR circuit was designed and implemented for a wide range of temperature from -40 to 125 $^{\circ}\text{C}$, including a startup and self-biasing circuit to reduce critical low-frequency noise from the bias circuitry and op amp input offset voltage. The BGR circuit generated a reference voltage of 1.25 V for a supply voltage range of 2.5 – 3.3 V. The gain of the implemented BGR operational transconductance amplifier is 84.1 dB. A non-overlapping clock circuit was implemented to reduce the clock skew effect, which is also one of the noise contributors. The noise analysis of a chopped bandgap voltage reference was evaluated through cadence periodic steady-state (PSS) analysis and periodic noise (PNoise) analysis. The low-frequency flicker noise was reduced from 1.5 to 0.4 $\mu\text{V}/\sqrt{\text{Hz}}$ at 1 KHz, with the proposed chopping scheme in the bandgap. Comparisons of the noise performance of the chopper-embedded BGR, with and without a low-pass filter, were also performed, and the results show a further reduction in the overall noise. A reduction in the flicker noise, from 181.3 to 10.26 $\text{mV}/\sqrt{\text{Hz}}$ at 100 KHz, was observed with the filter. All circuit blocks of the proposed BGR scheme were designed and simulated using the EDA tool HSPICE, and layout generation was carried out by Laker. The BGR architecture layout dimensions are 285.25 $\mu\text{m} \times 125.38$ μm .

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1. Introduction

The voltage reference is an integral building block for analog-mixed signal circuits and RF design. A bandgap reference circuit is used to provide a stable reference voltage. At the same time, it also has some internal degradation factors, such as biasing circuitry low-frequency noise, which comprises flicker noise and channel thermal noise; passive components as well as transistor-level noise, are very significant in terms of flicker noise, thermal noise and white noise. The main source of flicker noise is lattice defects at the interface of the silicon and the gate oxide, which creates a dangling bond and energy states. These states randomly trap channel charge carriers, causing a fluctuation in the threshold voltage. The time constant of the capture and release process is a few tenths to several milliseconds. Therefore, the corresponding flicker noise is observed at low frequencies. Another important noise source is the channel thermal noise current, as when it is in saturation, a MOSFET has an inversion layer with limited resistance, and this resistor, similar to any other resistor, generates a thermal noise current [1–4]. A switched capacitor resistor circuit was implemented in this work to suppress the thermal noise.

An operational transconductance amplifier (OTA) input offset voltage error can be amplified and introduce a significant error in the reference output voltage. These issues

need to be addressed to obtain a highly precise and stable reference voltage. A BGR scheme of bipolar junction transistors is more accurate and less sensitive to the process variation, in comparison to all MOSFET ones [5–8]. In [9], a MOSFET chopper-stabilized BGR scheme was presented. This design reported a significant variation in the reference output due to a maximum of 20% variation in the resistor value during circuit realization. This design approach strongly recommends multiple trimmings, which is a costly procedure. The BGR design in [10] used a Wilson current mirror with BJT for BGR realization. Another method includes curvature minimization to improve the BGR precision by applying circuit techniques. The piecewise linear technique demonstrated better flexibility for curvature minimization [11–15]. It has an additional requirement of overhead circuits, which consume more power to generate nonlinear signals. The proposed architecture strongly emphasizes resistor matching and employs a very effective resistor matching technique in the complete circuit design to obtain highly accurate resistor values and matching. It also includes a startup and a self-biasing circuit with a triggering loop, and an OTA with three chopper configurations for more accurate low-frequency biasing and offset noise suppression. The proposed BGR scheme provides a comprehensive analysis of noise reduction in time, as well as in the frequency domain. A non-overlapping clock was also implemented to obtain a more precise output. A switched capacitor resistor was implemented to achieve a more flexible BGR composite scheme. There are three techniques, namely trimming, correlated double sampling (auto-zero) and chopper modulation, that can be used to suppress low-frequency noise and the op amp offset. Multiple trimming is not a reliable and cost-effective noise reduction process. On the other hand, auto-zero is not a continuous noise reduction method, unlike chopper modulation.

A bandgap reference (BGR) provides a stable dc reference voltage for many analog circuits, such as A/D converters and clock generators using phase-locked loops (PLLs). The proposed BGR architecture and noise suppression biasing scheme can improve the performance of high-frequency noise-sensitive circuits, much like a clock generator/frequency synthesizer. Clock generators are widely used in many communication system applications as an accurate frequency synthesizer. In a clock generator, the VCO output frequency matches/locks with the reference frequency with the minimum K_{vco} to reduce the jitter noise [16–19]. At the same time, every block, such as the prescaler, charge pump, loop filter and VCO, creates some amount of noise. The biasing circuit and variation in the power supply also contribute to the noise. Hence, a clock generator requires a low-noise voltage regulator with a high PSRR to suppress supply and unwanted bias circuitry noise [20–25].

The proposed BGR circuit block diagram is shown in Figure 1. This architecture describes the chopper-stabilized BGR scheme implementation that suppresses critical flicker noise. It generates a stable voltage reference output for the prescribed process, temperature and supply variation range. Biasing scheme points Vbp1 and Vbp2 in the noise analysis also show a significant reduction in noise by using the proposed BGR circuit. Hence, the proposed architecture is highly effective in reducing the noise of the clock generators. The structure of this manuscript is summarized as follows: Section 2 describes the proposed chopper-stabilized BGR composite architecture; Section 3 explains the key layout features; Section 4 shows the results; and the conclusion is discussed in Section 5.

Figure 1. Block diagram of the chopper-stabilized BGR noise reduction scheme.

2. Chopper-Stabilized Composite BGR Scheme

To suppress unwanted low-frequency noise and input offset errors, three chopper circuits were implemented in the BGR. One chopper circuit was used at the input pair of the BGR and OTA, and the other two chopper circuits were implemented in the PMOS and NMOS current mirror branches. A non-overlapping clock circuit was also designed to suppress the clock skew effect, which is also one of the noise sources. A detailed OTA schematic of the proposed BGR scheme is shown in Figure 2.

Figure 2. Chopper-stabilized operational amplifier circuit of the BGR.

2.1. BGR Chopper-Embedded OTA with Startup and Self-Biasing Circuit

The proposed BGR core comprises self-bias, startup, stop/power-down and a folded cascode op amp with a chopper circuit. The block diagram architecture is displayed in Figure 1, while the core op amp with a chopper schematic is presented in Figure 2.

2.1.1. Operational Transconductance Amplifier

A folded cascode op amp was employed for the OTA to obtain a large common mode range, a high PSSR and output resistance. There are three choppers embedded in the folded cascode structure, as shown in Figure 2. One chopper is in the input pair as a square wave modulator, and the other two are in the PMOS and NMOS cascode branches for demodulation. The OTA structure has a startup/delay circuit and a safety power-down circuit, as discussed below.

2.1.2. Startup Circuit

There may be many degenerate bias points, including the zero current state. This can push the BGR into a non-desired equilibrium state. Hence, to avoid any such possibility, a startup circuit was designed with a large delay (10~200 μ s) and supply-independent biasing. This circuit block is shown in Figure 2, where there is an active biased current

mirror formed by M44 and M45 and a pull-down resistor. A differential input configuration was introduced to first initialize the startup circuit and then to infuse a large delay with a ramp supply voltage to settle down bias points Vbp2 and Vbn2. This prevents the core circuit from being stuck at any possible degenerate bias level. After the execution of pulse switching at node bgp_op_ini_in in the stipulated time delay duration, bias points Vbp2 and Vbn2 are established, the core op amp circuit starts working with self-bias and the startup circuit is stopped. At the beginning of the circuit operation, there may be a large difference at the differential switching of op_inl_in and nop_inl_in. Hence, a triggering loop circuit was designed from the output to the startup/delay circuit to speed up and wake up the circuit faster through transistors M34 and M49.

2.2. BGR Operating Principle

The BGR block diagram is shown in Figure 3a. It contains a chopper-embedded OTA, a PMOS cascode current mirror, two bipolar transistors (BJTs) and polysilicon resistors with a low temperature coefficient. PNP BJTs are used and realized by parasitic BJTs using CMOS technology. In the circuit, multiple symmetrical resistors, R8–R15, of 2 kΩ were implemented instead of a single value resistor. In this parallel configuration, the unit resistor value is identical to the resistor R7 of 2 kΩ. For circuit optimization, a resistor value of 250 Ω was obtained using eight identical 2 kΩ resistors in parallel. This reduced variation and improved the accuracy of the resistor value.

Similarly, for other resistor values in the BGR architecture, the emphasis is on the perfect matching of the lowest variations in the post-layout values. The implemented resistors using an identical unit value resistor are shown in Figure 3b. To realize 40 kΩ and 7.2 kΩ value resistors, a symmetrical and equal value resistor of 2 kΩ was applied. This may consume more area, but it improves the required matching criteria in the layout. BJT Q2 was produced eight times in comparison to Q1 by taking $n = 8$ in the final expression. All component dimensions are shown in Table 1. The PMOS cascode current mirror improves the supply rejection and maintains the branch current and voltage equality in the circuit.

This architecture has the key feature of important components functional flexibility, such as enabling/disabling non-overlapping clocks, and a chopper circuit in the BGR. It also contains an additional safety feature of power-down.

This architecture also realizes reduced noise biasing points Vbp1 and Vbp2 for further clock generator application. Their noise analysis is also discussed in the subsequent sections.

The working principle of the BGR provides the following expression for V_{bg} :

$$\begin{aligned}
 V_{bg} &= I_{M6} \times R_3 \quad [I_{M4} = I_{M6}] \\
 I_2 &= \frac{\Delta V_{BE}}{R_1} = \frac{V_T \ln(n)}{R_1} \\
 V_{bg} &= \frac{V_{BE1}}{R_7 + (R_8 \parallel R_8 \parallel \dots \parallel R_{12})} + \frac{V_T \ln(n)}{R_1} \\
 I_{M4} &= \frac{V_{BE1}}{R_2 (R_4 \parallel R_5)} + \frac{V_T \ln(n)}{R_1} \\
 V_{bg} &= I_{M4} \times R_3 \\
 V_{bg} &= R_3 \left[\frac{V_{BE1}}{R_2 + (R_4 \parallel R_5)} + \frac{V_T \ln(n)}{R_1} \right]
 \end{aligned}$$

The proposed architecture generates a stable 1.25 V reference voltage using the device parameters shown in Table 1.

The Monte Carlo simulation graph is shown in Figure 4. This was performed more than one hundred times to test the BGR startup circuit. The simulation graph shows a stabilized bandgap reference output Vbg, biasing voltages Vbp1 and Vbp2, and power-down signal voltage waveforms.

Figure 3. (a) Bandgap reference circuit with an embedded chopper circuit; (b) implementation of highly matched resistors for the BGR scheme.

Table 1. Summary of component dimensions of the proposed BGR architecture.

Component	Parameter
M1	$W = 10 \mu\text{m}, L = 4 \mu\text{m}, m = 8$
M2	$W = 10 \mu\text{m}, L = 1 \mu\text{m}, m = 8$
M3	$W = 10 \mu\text{m}, L = 1 \mu\text{m}, m = 2$
M4	$W = 10 \mu\text{m}, L = 1 \mu\text{m}, m = 2$
M5	$W = 10 \mu\text{m}, L = 4 \mu\text{m}, m = 2$
M6	$W = 10 \mu\text{m}, L = 1 \mu\text{m}, m = 2$
R1	7.2 k Ω
R2	40 k Ω
R3	40 k Ω
R4	2 k Ω
R5	2 k Ω
R6	2 k Ω
R7	10 k Ω
R8	250 Ω

Figure 4. Stabilized BGR output with a startup circuit.

Operational Amplifier Analysis

The BGR operational amplifier gain and phase margin were simulated with $3.3 \text{ V} \pm 10\%$ variation in the supply voltage at 3.3 V, 2.97 V and 3.63 V. The post-simulation OTA gain was 84.1 dB, with a phase margin of 59.48. The simulation graph is displayed in Figure 5.

For more accuracy, the operational amplifier was simulated and tested for all the process corners, voltages and temperature (PVT) variations. The post-simulation results are summarized in Table 2.

The noise analyses of the operational amplifier at different frequencies and for various process corners are summarized in Table 3.

Figure 5. Bandgap reference op amplifier gain and phase margin analysis.

Table 2. Summary of the operational amplifier PVT analysis.

S.N.	TT	SS	FF
Vdd (Voltage)	3.3 V	2.97 V	3.63 V
Temp (°C)	50	125	−40
Gain (dB)	84.1	80.06	89.12
PM (Degree)	59.48	55.57	66.52

Table 3. Summary of the operational amplifier noise analyses.

S.N.	TT	SS	FF
Vdd (Voltage)	3.3 V	2.97 V	3.63 V
Temp (°C)	50	125	−40
Freq = 1 KHz	7.89574 μ V	7.131022 μ V	6.676753 μ V
Freq = 10 KHz	92.72738 nV	67.98714 nV	118.9222 nV
Freq = 100 KHz	143.3527 pV	95.01332 pV	195.6376 pV

2.3. Non-Overlapping Clock Implementation

Precise clock switching is important for analog and digital systems. The clock signal controls the switching sequences and executes the entire operation of the circuit. Nowadays, a high clock frequency is desirable to improve the system performance, but the non-ideal effects of the increased frequency may result in clock skew and race conditions. To avoid these issues, two-phase non-overlapping clocks were implemented. There is a dead time between the clock edges. The non-overlapping clock signals are executed at the same frequency, and for a short time duration between the pulses; none of them are high. The non-overlapping clock signals are derived from the global overlapping clock signal inside each block to control the skew between the phases of the non-overlapping clock signals. This also reduces the capacitive loading on the global overlapping clock and improves the performance of the timing path. On-chip non-overlapping inverting clocks clk1 and clk2 were implemented from a global off-chip overlapping clock for the chopper circuit, as well

as for the switch capacitor resistor realization. Their schematic and simulation graphs are shown in Figures 6 and 7.

Figure 6. Non-overlapping clock generator.

2.4. Chopper Circuit Embedded in the OTA

The core of a BGR, delay circuit, bias circuit and OTA always has some low-frequency $1/f$ noise, resistor thermal noise and offset noise. These noises may severely degrade the bandgap reference accuracy performance. These unwanted effects can be eliminated/suppressed by the chopper circuit that is implemented in the BGR core circuit, as shown in Figure 2. Its transistor level schematic is shown in Figure 8. The chopper circuit comprises four switches: M1, M2, M3 and M4, which are driven by two phase non-overlapping clock signals: $\text{clk1}(\text{vsw1on})$ and $\text{clk2}(\text{vsw2on})$. The input modulator comprises M1, M2, M3 and M4, and transposes the input differential signal applied at the terminals vinp and vinm . This reduces the input pair mismatch error by swapping the signals at the vinp and vinm of the op amp. Here, a dummy switch is used with every swapping switch in order to cancel out the channel charge effect. Swapping or reverse polarity switches are able to multiply the analog input signal by $+1$ or -1 . As switches can be realized ideally in the CMOS technology, this chopper circuit thus works as a square wave modulator for chopper-stabilized amplifiers. In Figure 2, the square wave modulator chopper circuit is used at the input of the folded cascode structure, and the second square wave modulator chopper circuit is used at the folding node in the PMOS cascode current branch at the output. After the input differential pair, another significant source of noise is the folded NMOS current mirror branch. Hence, the third chopper circuit is used for higher accuracy. The input signal moves through the first square wave modulator, which turns into a square wave and becomes amplified by the high amplifier gain, and then it is demodulated again to dc at the amplifier output by the second chopper switch. Here,

the key point is that the amplifier offset and bias noise are also amplified with the input signal, but they are modulated only once through the amplifier output chopped modulator, meaning that the offset becomes bigger at the output of the amplifier and is filtered out by the low-pass filter. Hence, the input signal is modulated twice and remains unchanged, while the offset is modulated once, passed through the low-pass filter and then filtered out. We implemented a low-pass filter by using the switched capacitor resistor to further suppress the resistive thermal noise. The chopper switches are driven by the complementary non-overlapping clock signals clk1 and clk2 with a 50% duty cycle for the modulated square wave. There is one input chopper, one output PMOS chopper and one extra NMOS current mirror chopper. Here, the extra NMOS chopper cuts the $1/f$ noise and the offset of the NMOS, thereby providing an additional advantage.

Figure 7. Non-overlapping clock circuit simulation graph.

The chopper is fully differential, meaning that it generates matched spikes and therefore a low offset. The chopper-stabilized bandgap reference output was simulated in the time domain as well as in the frequency domain. Figure 9a,b shows the time domain simulation with the removal of noise glitches, when the chopper circuit is enabled. Figure 9a shows the bandgap reference output voltage V_{bg} with the chopper-disabled output. Here, the chopper circuit is disabled, meaning that V_{bg} has glitches, while in Figure 9b, the chopper circuit becomes enabled, and therefore, the output V_{bg} has no glitches.

Figure 8. Schematic of the chopper circuit.

(a)

Figure 9. Cont.

Figure 9. (a) Output Vbg without the chopper circuit; (b) output Vbg with the chopper circuit.

However, some spikes appear in the chopper-enabled Vbg output. This is due to the clock feedthrough effect of non-overlapping clocks.

The circuit was simulated for all process corners with a $3.3 \text{ V} \pm 10\%$ supply voltage at variations of 3.3 V, 2.97 V and 3.63 V and temperatures of 50°C , 125°C and -40°C for the TT, SS and FF corners. Glitches were reduced effectively in all three corners post-simulation when vchop was enabled, as shown in Figure 9b. The proposed BGR output curvature with an output voltage of 1.25 V for a wide temperature range is shown in Figure 10. The simulated graph has a variation of $800 \mu\text{V}$ for the TT corner. The PSRR is -66.8 dB for the typical corner.

Figure 10. Variation in Vbg over a wide temperature range.

2.5. Switched Capacitor Resistor and Low-Pass Filter

A low-pass filter (LPF) was designed and implemented to filter the high-frequency noise component in the chopper-embedded BGR output. Two low-pass filter circuits, Vbp1_filter and Vbp2_filter, were realized, as shown in Figure 11. Vbp1 has a low-pass filter with a switched capacitor resistor for variable desired resistor values and another fixed RC value filter configuration. It also has a direct pass to the BGR output, without filter application. All these three options provide multiple simulation flexibilities. Another filter, Vbp2_filter, was implemented for the cascode devices. Cascode devices are more immune to noise, hence the use of only one filter configuration.

Figure 11. (a) Variable low-pass filter for current source; (b) variable low-pass filter for cascode devices.

A switched capacitor resistor is very compact and is suitable for the on-chip fabrication of any desired resistor value. The resistor value depends only on the ratio of the capacitance and the switching frequency. An equivalent switched capacitor resistor is shown in Figure 12a. It has one capacitor, C_1 , and two switches, S1 and S2. A transmission gate is used for the switches S1 and S2, and non-overlapping clock signals are applied, as shown in Figure 12b. The low-pass filter configuration after adding a capacitor, C_2 , at the output of the switched capacitor resistor, as shown in Figure 12c. The filter loop bandwidth is less than 5 KHz for low-frequency noise removal.

Figure 12. (a) Switched capacitor resistor; (b) non-overlapping clock; (c) low-pass filter.

With the switching sequences of switch S2 being closed and switch S1 being open, and switch S1 being closed and switch S2 being open, we can transfer a charge q from the input V_{IN} to the output V_{OUT} , with the expression:

$$q = C (V_{IN} - V_{OUT})$$

The average current flowing from V_{IN} to V_{OUT} is:

$$I = q/t = qf$$

Hence:

$$I = fC (V_{IN} - V_{OUT})$$

Therefore:

$$R = 1/fC$$

A 3 dB bandwidth can be expressed by the following expression. Its schematic representation is shown by Figure 12.

$$\omega_{-3db} = 1/R_{eq}C_2 = f \times C_1/C_2$$

$$f_{-3db} = (1/2\pi) \times f \times C_1/C_2$$

2.6. Chopper-Enabled Bias Pre- and Post-Simulation

For more accuracy, the BGR output voltage and key nodes were also simulated and were observed to check for any possible variations and the performances of the TT, SS and FF corners in the pre- and post-circuit simulations. Table 4 summarizes the pre and post-simulation results and performances. It is observed that the V_{bg} and key biasing node voltages have significantly less variations in the pre and post-simulations. The lowest post-layout variation is achieved by incorporating the symmetric and matching component strategy discussed above.

The composite BGR circuit was further used to generate a very low noise bias circuit for the clock generator sub-blocks using the V_{bp1_filter} and V_{bp2_filter} biasing nodes from the BGR scheme. The schematic diagram of the clock generator bias sub-blocks is shown in Figure 13. A pre and post-simulation was performed to observe the current value at different clock generator bias circuit nodes for the TT, SS and FF corners. The simulation results and performances are summarized in Tables 5 and 6.

Table 4. Summary of the pre- and post-simulations.

Chopper Enabled	Pre_TT	Post_TT
Voltage	Pre	Post
Vbg	1.2314 V	1.2302 V
Vbp1	1.9474 V	1.9428 V
Vbp2	1.1281 V	1.1232 V
Vbp1_filter	1.9474 V	1.9428 V
Vbp2_filter	1.1281 V	1.1232 V

Figure 13. Clock generator bias circuit using the BGR composite scheme.**Table 5.** Summary of bias circuit current pre-simulation analysis.

Current	TT/3.3 V/50 °C	SS/2.97 V/125 °C	FF/3.63 V/−40 °C
3.75 μ A	3.7872 μ A	3.4434 μ A	4.1977 μ A
7.5 μ A	7.6112 μ A	6.9713 μ A	8.3593 μ A
15 μ A	15.253 μ A	14.021 μ A	16.675 μ A
30 μ A	30.505 μ A	28.0424 μ A	33.348 μ A
60 μ A	61.009 μ A	56.083 μ A	66.692 μ A

Table 6. Summary of bias circuit current post-simulation analysis.

Current	TT/3.3 V/50 °C	SS/2.97 V/125 °C	FF/3.63 V/−40 °C
3.75 μ A	3.8868 μ A	3.52155 μ A	4.3288 μ A
7.5 μ A	7.8594 μ A	7.16935 μ A	8.682 μ A
15 μ A	15.1114 μ A	13.9025 μ A	16.497 μ A
30 μ A	30.4494 μ A	27.9886 μ A	33.284 μ A
60 μ A	60.4294 μ A	55.5984 μ A	65.962 μ A

3. Chopper-Embedded BGR Layout

The chopper-embedded BGR circuit layout with all sub-blocks is shown in Figure 14, and the BGR with a bias circuit sub-block layout is shown in Figure 15.

Figure 14. Chopper-embedded BGR and sub-block layout ($285.25 \mu\text{m} \times 125.38 \mu\text{m}$).

Figure 15. BGR with bias circuit sub-block layout ($423.765 \mu\text{m} \times 315.825 \mu\text{m}$).

The chip layout was generated through the $0.18 \mu\text{m}$ CMOS process with dimensions of $285.25 \mu\text{m} \times 125.38 \mu\text{m}$. For better matching, a resistor layout was also created using a common centroid with dummies. At the same time, each resistor was constructed to

be long so that contact resistance becomes very small and does not have an influence. Polysilicon resistors with a low temperature coefficient were used for the resistor layout. This is better material, compared to diffusion resistors, for precise value fabrication.

The performance comparisons of the proposed BGR circuit with other bandgap references are shown in Table 7. This shows the comparisons between this work and other previous works [12,14,20,22,23]. The work in Reference [20] showed a superior TC, but the trimming technique application incurred an increase in cost. Compared to other bandgap reference circuits, this BGR architecture is compact, and no trimming is required; hence, it is more reliable and cost-effective. We achieved a TC of 4.36 (ppm/°C) with a voltage reference output of 1.25 V. The PSRR value of the proposed circuit is −68.8 dB. This work achieves the minimum current consumption and compact chip area compared to other previous works.

Table 7. Performance summary and comparison with other bandgap reference circuits.

Type	Proposed	[12]	[14]	[20]	[22]	[23]
Supply voltage (V)	2.8	3.6	5.2	26~5	2.5~5	3.5~5
V _{bg} (V)	1.25	1.23	3.65	1.14	1.196	3.11
Temp range (°C)	−40~125	−40~120	−40~100	−40~125	−10~130	−40~130
Trimming method	No-trim	Yes	Single-trim	Multi-trim	Multi-trim	Yes
Current consumption (μA)	30	180	750	33	38	108
Min TC (ppm/°C)	4.36	11.8	3	1.01	3.98	4.6
Line regulation (mV/V)	N.A.	N.A.	N.A.	2	0.19	0.31
PSRR (dB)	−68.8	−31.8	−127	−61	−84	−74
Chip area (mm ²)	0.03	0.1	0.28	0.04	0.053	0.223
Technology	0.18 μm CMOS	0.13 μm CMOS	0.18 μm Bi CMOS	0.35 μm CMOS	0.5 μm CMOS	0.18 μm CMOS

4. Composite BGR Frequency Domain Noise Analysis Results

Frequency domain, as well as time domain noise analysis, was performed for the chopper-enabled composite BGR circuit. Figure 16 shows the noise reduction analysis with and without the chopper scheme simulation graph in the frequency domain. The noise analysis of the composite BGR was evaluated through cadence periodic steady-state (PSS) analysis and periodic noise (PNoise) analysis. The flicker noise was reduced from 1.5 to 0.4 μV/sqrt(Hz) at 1 KHz using chopping techniques. Figure 17 shows that further improvement can be achieved with a filter application in the composite BGR architecture.

The graph shows a reduction in flicker noise from 181.3 to 10.26 mV/sqrt(Hz) at 100 KHz with a filter.

Figure 16. Noise comparisons between chopped and non-chopped bandgaps.

Figure 17. Noise reduction simulation graph for the chopped bandgap with a filter and without a filter.

5. Conclusions

In this paper, a high-performance chopper-embedded BGR architecture was presented to suppress low-frequency and offset noise. The complete architecture was realized through 0.18 μm CMOS technology with a startup and a power-down circuit for good accuracy. The BGR circuit generated a reference voltage of 1.25 V, with a supply voltage range of 2.5–3.3 V.

The operational transconductance amplifier (OTA) achieved a gain of 84.1dB. The chopper stabilization technique greatly reduced the critical low-frequency noise in comparison to the BGR without a chopper. A non-overlapping clock circuit was also implemented to suppress the clock skew effect. The low-frequency flicker noise was reduced from 1.5 to 0.4 $\mu\text{V}/\sqrt{\text{Hz}}$ at 1 KHz with the proposed chopping scheme in the bandgap. Comparisons of the noise performance of the chopper-embedded BGR with and without a low-pass filter were also performed, and the results show a further reduction in the overall noise. A reduction in flicker noise from 181.3 to 10.26 $\text{mV}/\sqrt{\text{Hz}}$ at 100 KHz was observed with the filter. Biasing noise analysis also showed a significant reduction in noise by using the proposed chopper-embedded BGR scheme. Hence, the proposed architecture is highly effective in reducing the noise of the clock generators.

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