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Improved Model Predictive Control for Asymmetric T-Type NPC 3-Level Inverter

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Abstract: In this paper, a model predictive control for an asymmetric T-type NPC 3-level inverter is presented. The mathematical model and characteristics of the reduced switching topology are described. An improvement for the predicted strategy with the pre-selected candidate vectors is proposed. The simulation and experimental results are provided and show good efficiency for the proposed control algorithm. The improved algorithm greatly reduces execution time by about 18% and delivers a better load current THD than the conventional model for predictive control. For comparison, similar tests are performed on both 2-level and conventional 3-level inverters. Although the current load quality of the asymmetrical inverter is not as good as the traditional 3-level inverter, it is much better than the 2-level inverter. In addition, it has the benefits of significantly reducing overall costs, simpler hardware system design, and faster predictive processing than the conventional 3-level inverters. Therefore, this asymmetric inverter has advantages for an application with the required output characteristics like the conventional 3-level inverter and with lower cost.

Keywords: asymmetric inverters; delay compensation; model predictive control; T-type NPC inverter; reduced switching

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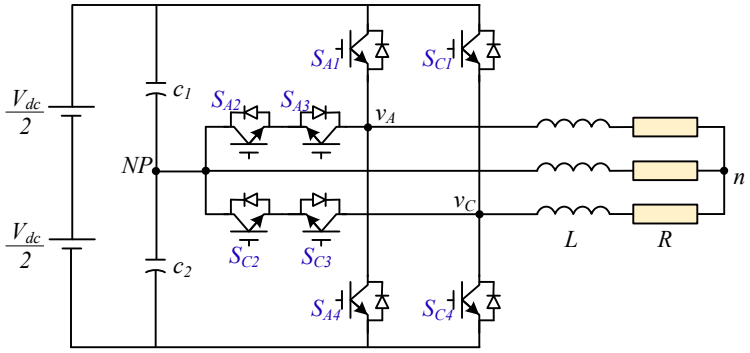
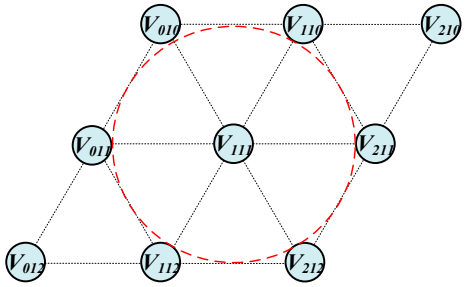
1. Introduction

Three-level voltage source converters have been widely used in industrial applications, which include high-power motor drivers [1], electric vehicles [2], and grid-connected renewable energy conversion systems [3]. Particularly in high-power and medium-voltage applications, they have outstanding advantages compared to 2-level converters, such as lower switching losses, reduced voltage stress in DV/DT across the power devices [4–6], and better total harmonic distortion (THD). The most common inverter topologies among them are the flying capacitor (FC), cascaded H-bridge (CHB), and neutral point clamped (NPC). The T-type NPC inverter was more efficient than traditional NPC inverters up to the medium switching frequency range [7–10].

Although 3-level NPC inverters have many advantages compared with 2-level inverters, as mentioned above, their main disadvantages are a higher cost, increased system volume, and reduced reliability because of the increased number of devices. Many recent studies focus on developing reduced switched topologies [11–17] to reduce cost, with a smaller size and increased system reliability. In [11–13], the diode NPC 3-level 2-leg topology was proposed where the required number of switches is reduced from 12 IGBTs and 6 diodes to 8 IGBTs and 4 diodes. A similar structure for T-type has been proposed to eliminate the diodes [17]. These topologies only need two legs for a three-phase 3-level inverter, so the number of components is reduced by one-third, as shown in Figure 1a. However, its drawbacks are that the linear output voltage is limited to half, as shown in Figure 1b.



(**a**) The topology of the two legs 3−level T−type inverter



(**b**) Space vector diagram of the two legs 3−level T−type inverter

Figure 1. Structure of the two legs T-type 3-level inverter.

The current control of a three-phase inverter has drawn much attention from researchers in the last decades. The conventional control strategy via proportional-integral (PI) current controllers with pulse width modulation (PWM) [18,19] can gain multiple-objectives, such as the reference current tracking, the reduction of the switching losses, reduced common mode voltage, and DC neutral point balancing. However, this technique suffers from many drawbacks such as a low dynamic response and demanding tuning of PI controller parameters.

With the development of digital signal processors, predictive control strategies have been studied intensively for power electronics converter systems. One of them, deadbeat predictive control [20,21] uses the system model to calculate reference voltage of modulator, which makes the error zero in the next sampling time. The deadbeat control achieves fast dynamic response, but its performance can be degraded caused by measurement noise and parameter variations [22]. Another one, named model predictive control (MPC), is known due to its simplicity of control principle, ease of implementation, ability to integrate multi-object control simultaneously, and excellent dynamic [23–27]. Because of its use of one vector in the sampling period, the MPC leads to high current ripples and variable switching frequency for the converter output. Improvement of the steady state performances demands the MPC to run at a high sampling rate. This difficulty can be avoided by multiple-vector-based model predictive control [28–30]. In every sampling period, the control scheme selects the appropriate voltage vector sequence and calculates duty cycles to minimize the cost function. Even if this approach can improve steady state performance, the control complexity is rather high, particularly for multilevel converter topologies.

This paper proposes a so-called asymmetric 3-level T-type NPC inverter by adding a half-bridge leg to the 2-leg 3-level NPC inverter. This new configuration, as shown in Figure 2, enables twice the output voltage range compared to Figure 1. An improved model predictive control (IMPC) algorithm for this configuration is proposed for current tracking and capacitor voltage balancing. The candidate vector selection strategy is presented to avoid high voltage jumps in phase legs without designing any additional cost functions. This significantly reduces execution time and switching frequency and improves load cur-

rent distortion. Simulations and experiments will be performed to verify the effectiveness of the proposed method for asymmetric T-type NPC 3-level inverter.

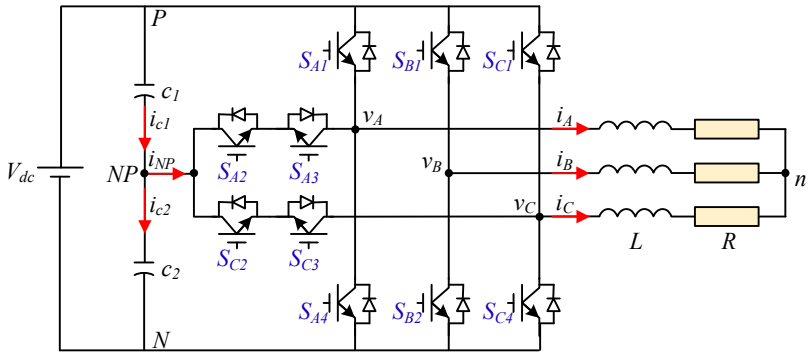


Figure 2. The topology of asymmetric T-type NPC 3-level Inverter.

The rest of the paper is organized as follows: Section 2 presents the mathematical model of asymmetric 3-Level T-type NPC Inverter; Section 3 describes the proposed MPC algorithm; Section 4 discusses simulation and experimental results, and finally, the conclusions are included in Section 5.

2. Mathematical Model of Asymmetric 3-Level T-Type NPC Inverter

The asymmetric inverter topology is shown in Figure 2. The phases A and C are 3-level T-type legs; phase leg B is a half-bridge. Two DC-bus voltages are supplied via DC-link capacitors (c_1, c_2) in series. Three-phase load R-L is connected to the output terminals of the converter.

Under the condition of balanced DC-link capacitor voltages, the phase leg voltage (v_{XN}) can be expressed as follows:

$$v_{XN} = S_X \frac{V_{dc}}{2}, \tag{1}$$

where $X \in \{A, B, C\}$; S_X is the phase switching state.

The switching states of three phases legs are described in Table 1. For 3-level legs phase A, C; S_X can be 0, 1, 2. For 2-level legs phase B; S_X can be 0, 2.

Table 1. Switching states and output voltages of the asymmetric inverter.

For Phase X with $X \in \{A, C\}$						**For Phase B**			
Switching State	**Device State**				**Output Voltage**	**Switching State**	**Device State**		**Output Voltage**
S_X	S_{X1}	S_{X2}	S_{X3}	S_{X4}	v_{XN}	S_B	S_{B1}	S_{B2}	v_{BN}
2	1	1	0	0	V_{dc}	2	1	0	V_{dc}
1	0	1	1	0	$\frac{1}{2}V_{dc}$	-	-	-	-
0	0	0	1	1	0	0	0	1	0

The Clarke formula transforms three phase leg voltages in the abc to $\alpha\beta$ coordinate system as follows:

$$\vec{v}_{\alpha\beta} = \frac{2}{3}\left(v_{AN} + e^{j2\pi/3}v_{BN} + e^{j4\pi/3}v_{CN}\right). \tag{2}$$

Similar for three phase currents:

$$\vec{i}_{\alpha\beta} = \frac{2}{3}\left(i_A + e^{j2\pi/3}i_B + e^{j4\pi/3}i_C\right). \tag{3}$$

Applying (1) and (2) to all switching states, the voltage vectors of the asymmetric T-type NPC 3-level inverter can be deduced. The converter generates 18 voltage vectors v_k; $k = 0 \div 17$, including 6 large voltage vectors (LV), 4 medium voltage vectors (MV), 6 small voltage vectors (SV), and 2 redundant zero voltage vectors (ZV), as illustrated in Table 2.

Table 2. Switching states and output voltage vectors for proposed inverter.

Type	Switching State	Output Voltage			Voltage Vector v_k
	$S_A S_B S_C$	v_{AN}	v_{BN}	v_{CN}	
Zero voltage vector	000	0	0	0	$v_0 = 0 + j0$
	222	V_{dc}	V_{dc}	V_{dc}	$v_7 = 0 + j0$
Small voltage vector	100	$\frac{1}{2}V_{dc}$	0	0	$v_{12} = \frac{1}{3}V_{dc} + j0$
	221	V_{dc}	V_{dc}	$\frac{1}{2}V_{dc}$	$v_{13} = \frac{1}{6}V_{dc} + j\frac{\sqrt{3}}{6}V_{dc}$
	121	$\frac{1}{2}V_{dc}$	V_{dc}	$\frac{1}{2}V_{dc}$	$v_{14} = -\frac{1}{6}V_{dc} + j\frac{\sqrt{3}}{6}V_{dc}$
	122	$\frac{1}{2}V_{dc}$	V_{dc}	V_{dc}	$v_{15} = -\frac{1}{3}V_{dc} + j0$
	001	0	0	$\frac{1}{2}V_{dc}$	$v_{16} = -\frac{1}{6}V_{dc} - j\frac{\sqrt{3}}{6}V_{dc}$
	101	$\frac{1}{2}V_{dc}$	0	$\frac{1}{2}V_{dc}$	$v_{17} = \frac{1}{6}V_{dc} - j\frac{\sqrt{3}}{6}V_{dc}$
Medium voltage vector	120	$\frac{1}{2}V_{dc}$	V_{dc}	0	$v_8 = 0 + j\frac{\sqrt{3}}{3}V_{dc}$
	021	0	V_{dc}	$\frac{1}{2}V_{dc}$	$v_9 = -\frac{1}{2}V_{dc} + j\frac{\sqrt{3}}{6}V_{dc}$
	102	$\frac{1}{2}V_{dc}$	0	V_{dc}	$v_{10} = 0 - j\frac{\sqrt{3}}{3}V_{dc}$
	201	V_{dc}	0	$\frac{1}{2}V_{dc}$	$v_{11} = \frac{1}{2}V_{dc} + j\frac{\sqrt{3}}{6}V_{dc}$
Large voltage vector	200	V_{dc}	0	0	$v_1 = \frac{2}{3}V_{dc} + j0$
	220	V_{dc}	V_{dc}	0	$v_2 = \frac{1}{3}V_{dc} + j\frac{\sqrt{3}}{3}V_{dc}$
	020	0	V_{dc}	0	$v_3 = -\frac{2}{3}V_{dc} + j\frac{\sqrt{3}}{3}V_{dc}$
	022	0	V_{dc}	V_{dc}	$v_4 = -\frac{2}{3}V_{dc} + j0$
	002	0	0	V_{dc}	$v_5 = -\frac{1}{3}V_{dc} - j\frac{\sqrt{3}}{3}V_{dc}$
	202	V_{dc}	0	V_{dc}	$v_6 = \frac{1}{3}V_{dc} - j\frac{\sqrt{3}}{3}V_{dc}$

The space vector diagram of the asymmetric T-type 3-level inverter is shown in Figure 3. The linear modulation range, corresponding to the radius of the largest circle inscribed in the hexagon, of this topology is extended to twice that of the NPC 3-level 2-leg asymmetric inverter [14–17].

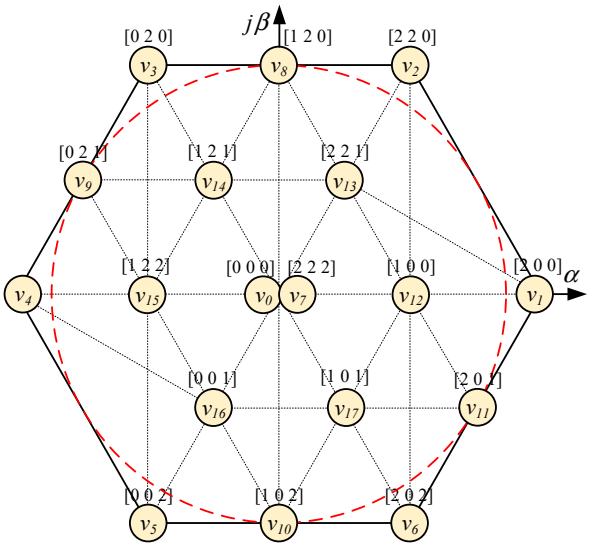


Figure 3. Space vector diagram of asymmetric T-type 3-level NPC inverter.

The specific characteristics of an asymmetric inverter compared with conventional 2-level and 3-level inverters are reported in Table 3. The asymmetric topology can generate line voltages at 5 voltage levels 0, $\pm\frac{1}{2}V_{dc}$, and $\pm V_{dc}$ similarly to the traditional 3-level inverter. Furthermore, the different voltage vectors of the asymmetric inverter are 17, only two less than the space vector diagram of a traditional 3-level inverter. Therefore, it would be expected that the performance of the asymmetric inverter be as good as the 3-level NPC inverter.

Table 3. Typical properties comparison of conventional 2-level, 3-level, and asymmetric 3-level inverter.

Characteristic	2-Level	3-Level	Asymmetric 3-Level
Structure	+Symmetric +Using 6 IGBTs	+Symmetric +Using 12 IGBTs	+Asymmetric +Using 10 IGBTs
Switching states	8	27	18
Different voltage vectors	7	19	17
Line voltage levels	$\pm V_{dc}$;0	$\pm V_{dc}$;$\pm\frac{1}{2}V_{dc}$;0	$\pm V_{dc}$;$\pm\frac{1}{2}V_{dc}$;0

3. Proposed MPC for Asymmetric T-Type NPC 3-Level Inverter

The block diagram of the improved MPC algorithm for the asymmetric T-type NPC inverter to achieve the two main goals of current tracking and voltage capacitor balancing is shown in Figure 4. The algorithm consists of the following stages: establishment of cost functions for current tracking and capacitor voltage balancing based on a mathematical model, design of the global cost function and candidate vector pre-selection strategy to optimize execution time, and improvement of THD of load current.

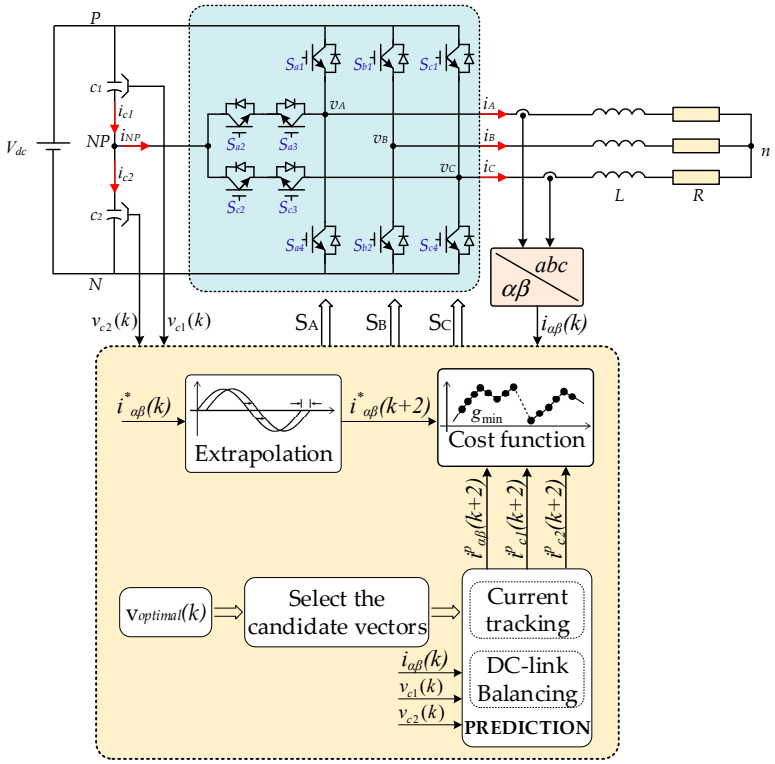


Figure 4. Block diagram of improved MPC algorithm for the asymmetric T-type NPC inverter.

3.1. Current Tracking Control

The mathematical model of the asymmetric configuration is described as follows:

$$\begin{cases} v_{AN} = i_A R + L\frac{di_A}{dt} + V_{nN} \\ v_{BN} = i_B R + L\frac{di_B}{dt} + V_{nN} \\ v_{CN} = i_C R + L\frac{di_C}{dt} + V_{nN.} \end{cases} \tag{4}$$

where V_{nN} is the offset voltage between the neutral-point of load and the negative of the DC-bus.

Using (2) and (3), the Equation (4) can be rewritten in the $\alpha\beta$ coordinate system as follows:

$$v_{\alpha\beta} = i_{\alpha\beta} R + L\frac{di_{\alpha\beta}}{dt}. \tag{5}$$

Euler's forward approximation to convert the continuous domain to the discrete domain with sampling period T_s is as follows:

$$\frac{di}{dt} \approx \frac{i(k+1) - i(k)}{T_S}. \tag{6}$$

Substituting (6) into (5), the predicted current is obtained in the discrete domain as:

$$i^p_{\alpha\beta}(k+1) = \left(1 - \frac{R}{L}T_S\right) i_{\alpha\beta}(k) + \frac{T_S}{L} v_{\alpha\beta}(k), \tag{7}$$

where $i^p_{\alpha\beta}(k+1)$ is the predicted current at time $(k+1)$; $i_{\alpha\beta}(k)$ is the current feedback at time (k); $v_{\alpha\beta}(k)$ is the voltage vector corresponding to the switching states of the inverter.

To obtain delay compensation due to algorithm calculations and analog-to-digital converters, the discrete-time equation of the model (7) is shifted one step forward as:

$$i^p_{\alpha\beta}(k+2) = \left(1 - \frac{R}{L}T_S\right) i_{\alpha\beta}(k+1) + \frac{T_S}{L} v_{\alpha\beta}(k). \tag{8}$$

The cost function for current tracking can be expressed as [26,27,31]:

$$g_i = \left[i^*_\alpha(k+2) - i^p_\alpha(k+2)\right]^2 + \left[i^*_\beta(k+2) - i^p_\beta(k+2)\right]^2, \tag{9}$$

where $i^*_{\alpha\beta}(k+2)$ is the reference current at time $(k+2)$. It can be determined by the Lagrange extrapolation formula as follows:

$$i^*_{\alpha\beta}(k+2) = 6i^*_{\alpha\beta}(k) - 8i^*_{\alpha\beta}(k-1) + 3i^*_{\alpha\beta}(k-2). \tag{10}$$

3.2. DC-Link Capacitor Voltage Balancing

Assuming that $C_1 = C_2 = C$, the DC-link capacitor voltages $(v_{c1},\ v_{c2})$ are described as follows [32]:

$$\begin{cases} \frac{dv_{c1}}{dt} = \frac{1}{2C} i_{NP} \\ \frac{dv_{c2}}{dt} = -\frac{1}{2C} i_{NP.} \end{cases} \tag{11}$$

where i_{NP} is the neutral point current, as shown in Figure 2.

Using Equation (6), the predicted voltage of the capacitor is written in the discrete-time domain as follows:

$$\begin{cases} v^p_{c1}(k+1) = v_{c1}(k) + \frac{T_S}{2C} i_{NP}(k) \\ v^p_{c2}(k+1) = v_{c2}(k) - \frac{T_S}{2C} i_{NP}(k). \end{cases} \tag{12}$$

The delay is compensated by shifting in (12) forward one step as follows:

$$\begin{cases} v_{c1}^{p}(k+2) = v_{c1}(k+1) + \frac{T_S}{2C} i_{NP}(k) \\ v_{c2}^{p}(k+2) = v_{c2}(k+1) - \frac{T_S}{2C} i_{NP}(k). \end{cases} \tag{13}$$

The current $i_{NP}(k)$ is calculated in relation to the switching states as below:

$$i_{NP}(k) = [S_{A2}(k) - S_{A1}(k)]i_A(k) + [S_{C2}(k) - S_{C1}(k)]i_C, \tag{14}$$

where S_{X1}, S_{X2} with $X \in \{A, C\}$ are defined as Table 1; $i_A(k)$ and $i_C(k)$ are the measurement currents at time k on phases A and C, respectively.

The cost function for the DC-link capacitor voltage balance is defined as follows:

$$g_u = \left[v_{c1}^{p}(k+2) - v_{c2}^{p}(k+2)\right]^2. \tag{15}$$

3.3. Global Cost Function

The global cost function for current tracking and capacitor voltage balancing is defined as follows:

$$g = g_i + \lambda_u g_u, \tag{16}$$

where λ_u is the weighting factor to adjust the balance of the capacitor voltages.

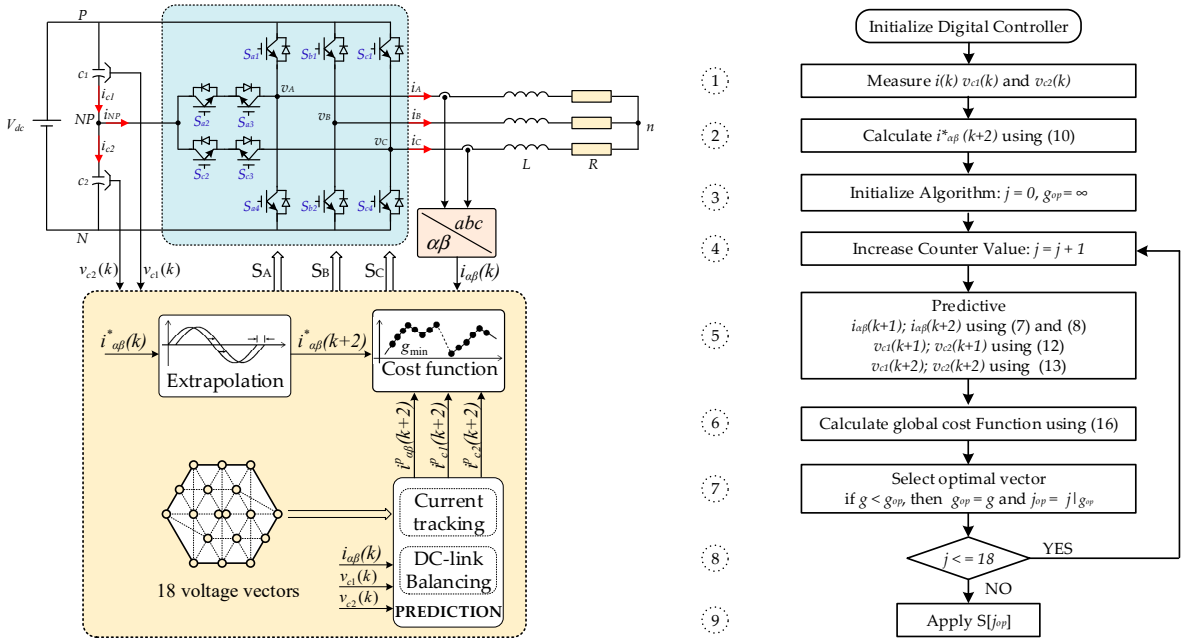
The block diagram of the conventional MPC algorithm is presented in Figure 5a. The implementation flowchart, as shown in Figure 5b, consists of 9 steps:

① Measure current, capacitor voltages from sensor feedback signals;
② The reference current at the time $(k+2)$ is calculated by extrapolation;
③ Initialize the initial values;
④ Enter the loop, where the counter increases j value in steps;
⑤ The output current and DC capacitor voltages are predicted to time $(k+2)$ corresponding to each candidate vector;
⑥ Calculate the global cost function;
⑦ During any iteration, if $g < g_{op}$, the minimum of g value is stored as an optimal value g_{op} and the corresponding position is stored as j_{op};
⑧ Check the loop condition, if $g \leq 18$ is true then return to execute the tasks from step 4, if false, exit the loop and continue to step 9;
⑨ Apply the switching states based on the j_{op} value.

The conventional MPC for an asymmetric T-type 3-level NPC inverter uses 18 switching states for the prediction. The execution time is obviously reduced compared to the traditional 3-level inverter with 27 switching states. The MPC algorithm in this paper is designed to prioritize the current tracking and balance the capacitor voltage by adjusting the weighting factor λ_u.

3.4. Improved Algorithm

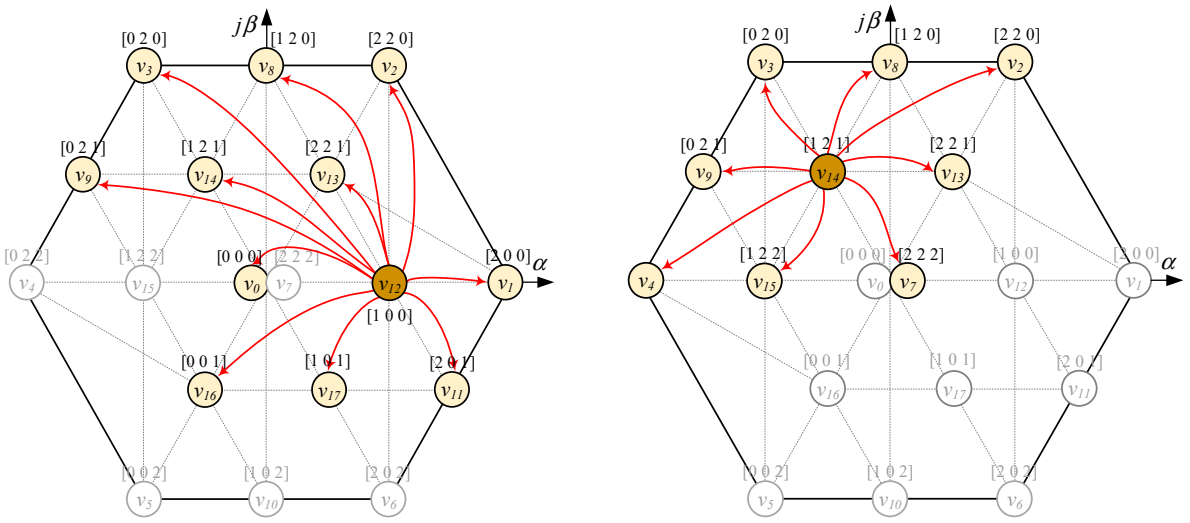
Although the conventional MPC algorithm satisfies the design requirements, it may have associated adverse effects. For example, when vector $v_6(202)$ is being used at time k, the optimal vector at the time $(k+1)$ is $v_{12}(100)$. At phase leg C, the switching from 2 to 0 causes a high voltage jump with amplitude V_{dc}. In addition, all four IGBTs of the phase C switch state cause large switching frequency. The candidate vector pre-selection strategy is proposed to overcome the issues without the need to design any additional cost functions. Based on the vector being applied at instant k, vectors that cause switching 0 to 2 or 2 to 0 will not be included in the predictive model for time $(k+1)$.



(**a**) Block diagram of conventional MPC algorithm. (**b**) Implementation of conventional MPC.

Figure 5. Normal MPC algorithm for the asymmetric T-type NPC inverter.

For example, in the case the vector v_{12} applies at instant k, there are 12 voltage vectors (v_0, v_1, v_2, v_3, v_8, v_9, v_{11}, v_{12}, v_{13}, v_{14}, v_{16}, v_{17}) that are suitable which do not cause a high voltage jump on phase leg A and C, as shown in Figure 6a. These switching states are considered as candidates for the prediction model to select the optimal vector applied at time (k + 1). Another example is v_{14} at instant k as shown in Figure 6b, where all states are satisfied for phases A and C. In this situation, vectors that do not cause a high voltage jump in phase leg B will be chosen as candidate vectors, including (v_2, v_3, v_4, v_7, v_8, v_9, v_{14}, v_{15}).



(**a**) The vector being applied is v_{12}. (**b**) The vector being applied is v_{14}.

Figure 6. The strategy for selecting candidate vectors.

Similarity analysis applies for the remaining vectors, and preselected candidate vectors are listed as shown in Table 4. The improved algorithm uses a maximum 12 vectors for each prediction, so it greatly reduces the computational burden compared to the conventional MPC algorithm.

Table 4. The candidate vector pre-selection strategy based on the vector applied at time k.

Vector	The Candidate Voltage Vectors	Vector	The Candidate Voltage Vectors
v_0	v_0, v_3, v_8, v_9, v_{12}, v_{14}, v_{16}, v_{17}	v_9	v_0, v_3, v_4, v_5, v_8, v_9, v_{10}, v_{12}, v_{13}, v_{14}, v_{15}, v_{17}
v_1	v_1, v_8, v_{10}, v_{11}, v_{12}, v_{13}, v_{14}, v_{17}	v_{10}	v_4, v_5, v_6, v_7, v_9, v_{10}, v_{11}, v_{13}, v_{14}, v_{15}, v_{16}, v_{17}
v_2	v_2, v_8, v_{11}, v_{12}, v_{13}, v_{14}, v_{15}, v_{17}	v_{11}	v_1, v_2, v_6, v_7, v_8, v_{10}, v_{11}, v_{12}, v_{13}, v_{14}, v_{15}, v_{17}
v_3	v_0, v_3, v_8, v_9, v_{12}, v_{14}, v_{16}, v_{17}	v_{12}	v_0, v_1, v_2, v_3, v_8, v_9, v_{11}, v_{12}, v_{13}, v_{14}, v_{16}, v_{17}
v_4	v_4, v_5, v_9, v_{10}, v_{14}, v_{15}, v_{16}, v_{17}	v_{13}	v_1, v_2, v_7, v_8, v_{10}, v_{11}, v_{12}, v_{13}, v_{14}, v_{15}, v_{16}, v_{17}
v_5	v_4, v_5, v_9, v_{10}, v_{14}, v_{15}, v_{16}, v_{17}	v_{14}	v_2, v_3, v_4, v_7, v_8, v_9, v_{13}, v_{14}, v_{15}
v_6	v_6, v_7, v_{10}, v_{11}, v_{13}, v_{14}, v_{15}, v_{17}	v_{15}	v_4, v_5, v_6, v_7, v_9, v_{10}, v_{11}, v_{13}, v_{14}, v_{15}, v_{16}, v_{17}
v_7	v_6, v_7, v_{10}, v_{11}, v_{13}, v_{14}, v_{15}, v_{17}	v_{16}	v_0, v_3, v_4, v_5, v_8, v_9, v_{10}, v_{12}, v_{14}, v_{15}, v_{16}, v_{17}
v_8	v_0, v_1, v_2, v_3, v_8, v_9, v_{11}, v_{12}, v_{13}, v_{14}, v_{16}, v_{17}	v_{17}	v_0, v_1, v_5, v_6, v_{10}, v_{11}, v_{12}, v_{16}, v_{17}

The digital implementation diagram of the improved MPC algorithm is shown in Figure 7, consisting of 9 steps similar to that of the conventional MPC algorithm. However, step 2 incorporates an additional task of selecting candidate vectors. The number of loop executions is equal to the number of candidate vectors, instead of 18 as in the conventional MPC algorithm.

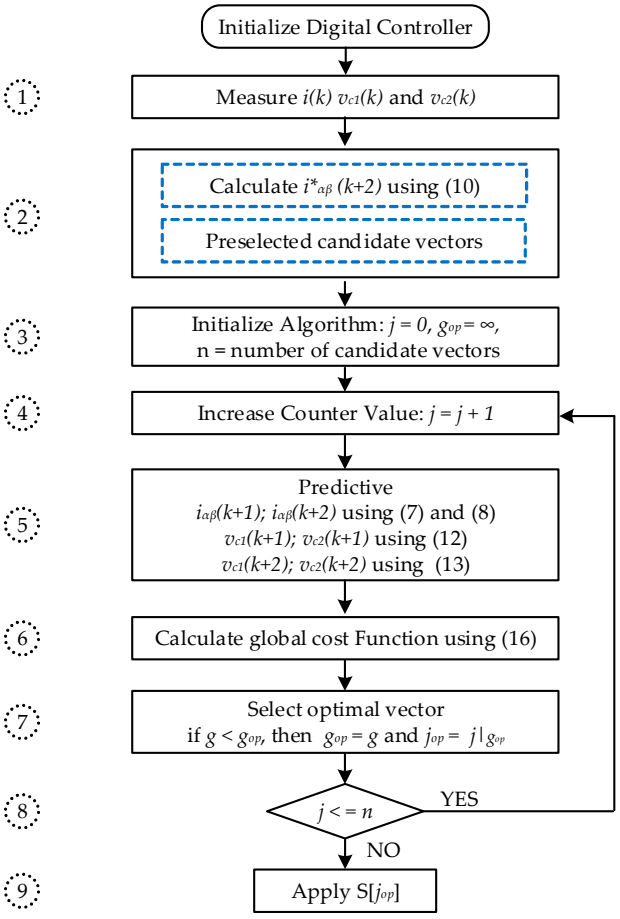


Figure 7. Implementation of improved MPC for the asymmetric T-type NPC inverter.

4. Simulation and Experimental Results

4.1. Simulation Results

To validate the improved MPC algorithm for an asymmetric T-type NPC inverter, simulations were performed using MATLAB/Simulink software with version 2018a, as shown in Figure 8. The system parameters are shown in Table 5.

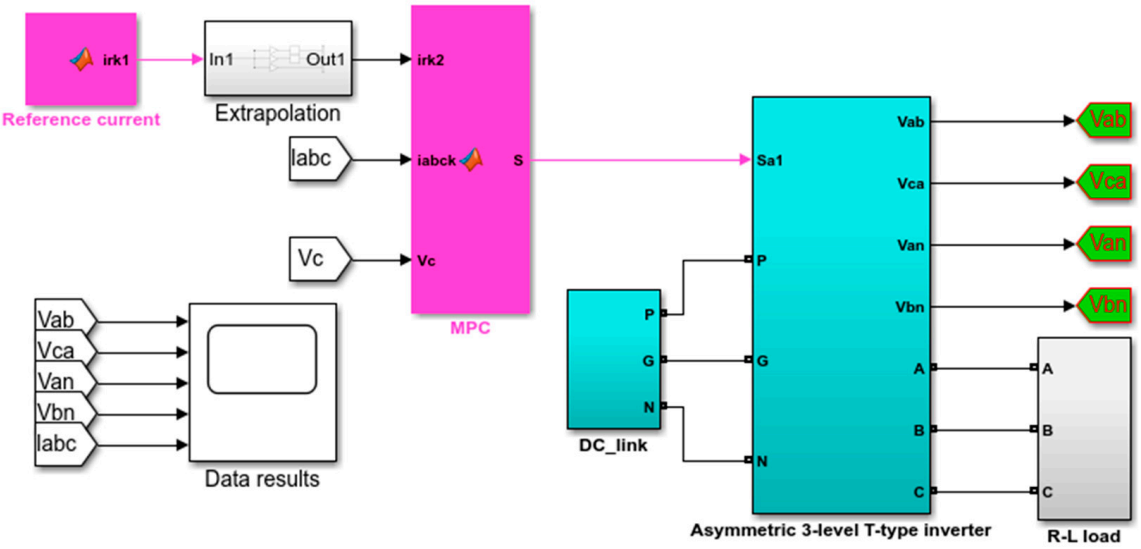


Figure 8. Simulation diagram of the improved MPC algorithm for asymmetric T-type NPC inverter.

Table 5. System parameters for simulation and experimental.

Description	Variable	Value
DC voltage	V_{dc}	200 V
Load 1	R_1, L_1	25 Ω, 50 mH
Load 2	R_2, L_2	25 Ω, 50 mH
DC-link capacitor	C_1, C_2	1200 μF
Sampling frequency	f_s	20 kHz
Frequency	f	50 Hz
Weighting factor	λ_u	0.005

The first simulation is performed with the improved MPC algorithm at reference current 15 A, and the parameter is λ_u weighting factor. The influence of the weighting factor on the THD load current and the voltage difference between the capacitors ΔV_{dc} is described in Figure 9. The higher λ_u, the smaller ΔV_{dc}, but THD tends to be increased. From the figure, for example, the requirement $\Delta V_{dc} < 5$ V (i.e., $\frac{\Delta V_{dc}}{\frac{1}{2}V_{dc}} \leq 2.5\%$) can be obtained if $\lambda_u \geq 0.005$. Therefore, $\lambda_u = 0.005$ for the best THD is selected in the following studies.

Steady-state responses at reference current 3 A of the improved method for the asymmetric T-type NPC inverter are illustrated in Figure 10. Load currents are sinusoidal and stable at the set values with THD about 0.94%, as in Figure 10a,c. The capacitor voltages are maintenance balanced with ΔV about 4 V, as shown in Figure 10b.

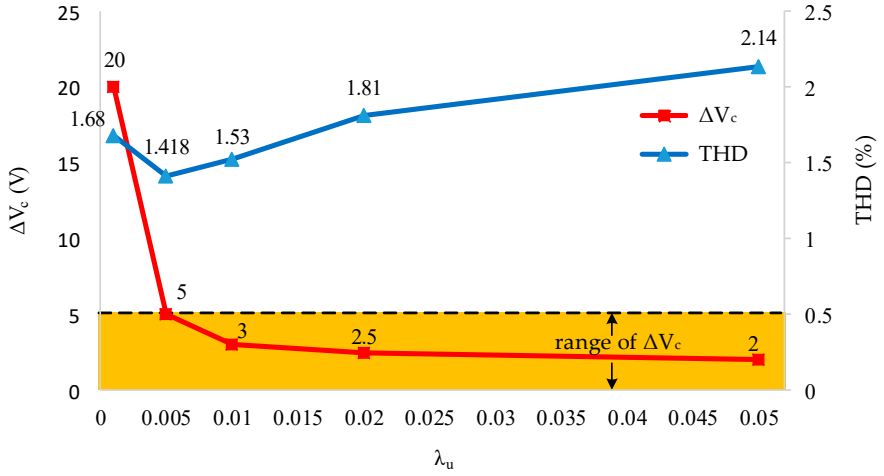
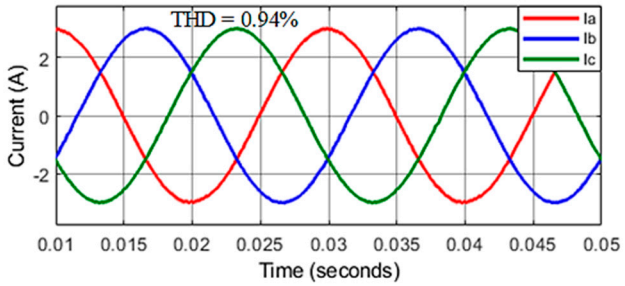
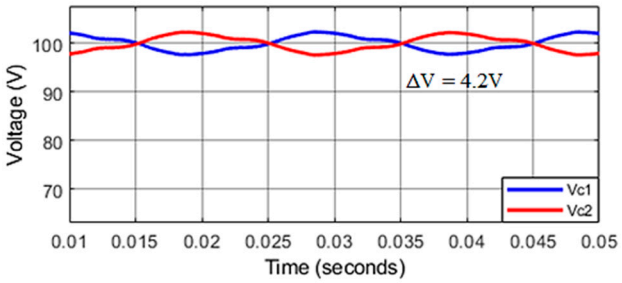


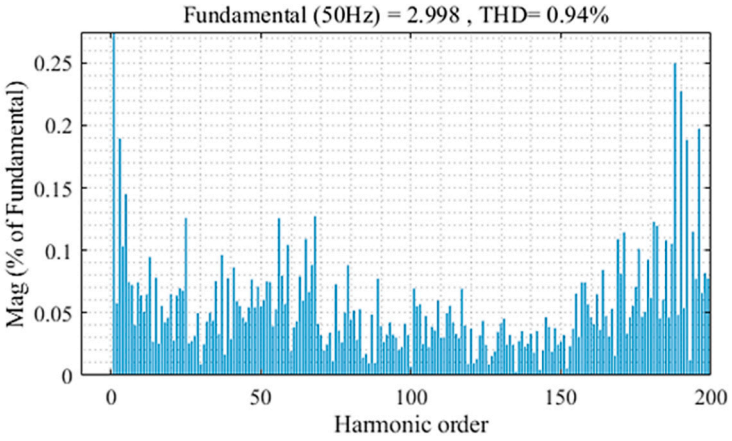
Figure 9. Effect of weighting coefficient on THD and ΔV_{dc} characteristics.



(**a**) Three phase load current.



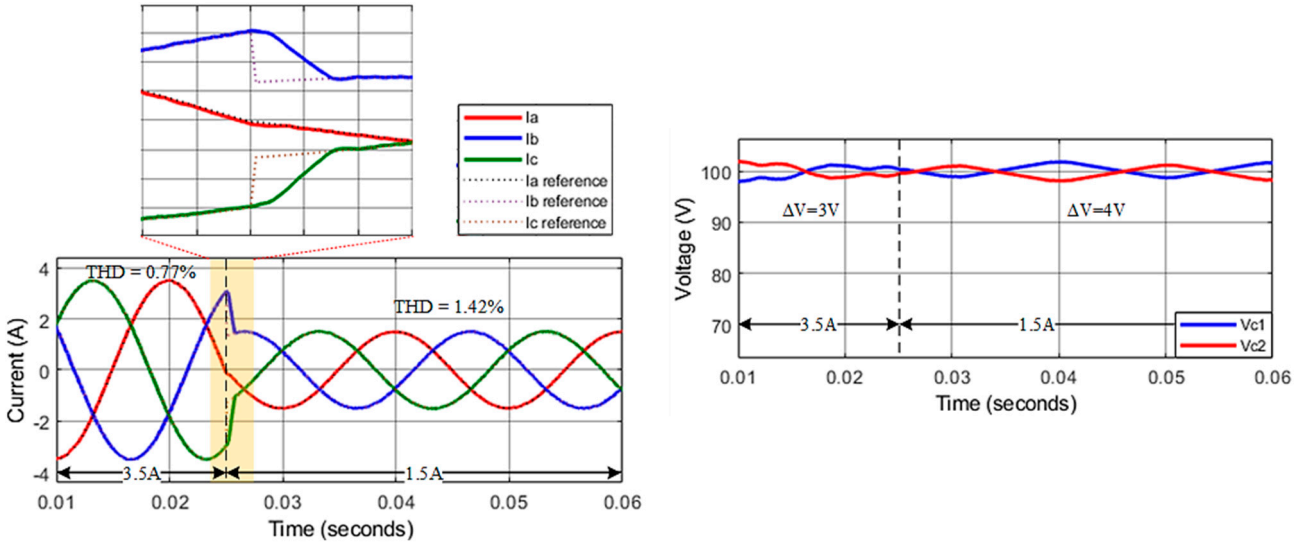
(**b**) Capacitor voltages.



(**c**) Current harmonic spectrum.

Figure 10. The steady−state response of asymmetric inverter using improved MPC algorithm.

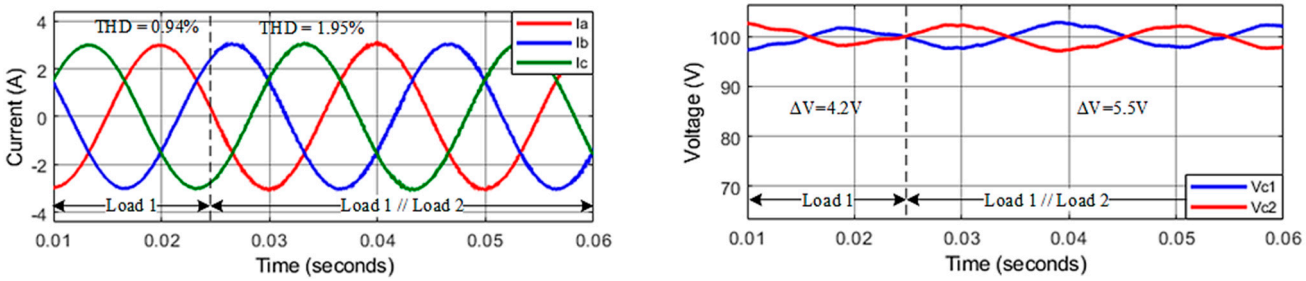
To check the system's dynamic response, a simulation is performed with an abrupt change of reference current from 3.5 A to 1.5 A at time $t = 0.025$ s. The load current quickly tracks and stabilizes at the set value after about 1/10 of the fundamental period, and THD increases from 0.77% to 1.42%, as shown in Figure 11a. The capacitor voltages are maintained in balance, as shown in Figure 11b.



(**a**) Three phase load current. (**b**) Capacitor voltages.

Figure 11. Transient response of asymmetric inverter using improved MPC algorithm.

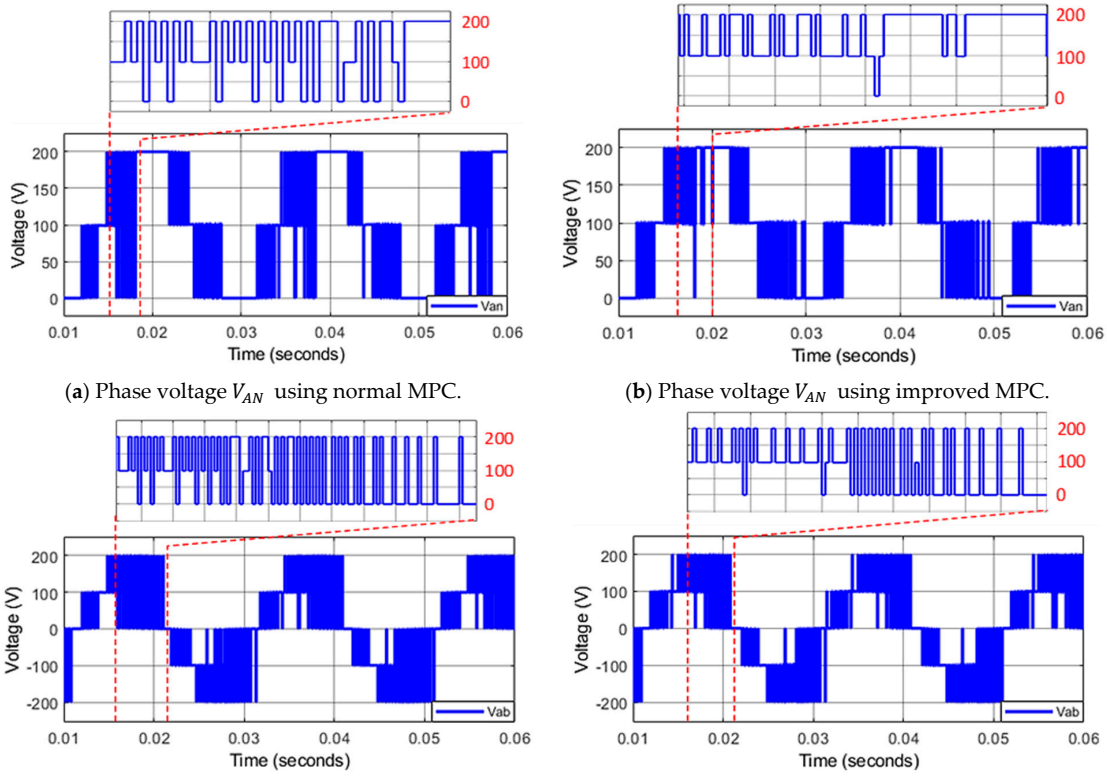
Another simulation scenario is performed under changing load parameters. A short time after connecting the second load ($R_2 = 25\ \Omega$, $L_2 = 50$ mH) in parallel with R_1L_1 at t = 0.025 s, the reference current is maintained at 3 A. The results show that the current is stable at a set value, and THD increases from 0.94% to 1.95%, as illustrated in Figure 12a. The capacitor voltages are well balanced, as shown in Figure 12b. In the previous transient investigation, the improved MPC algorithm applying to asymmetric T-type inverter proves to have good performance during load changing.



(**a**) Three phase load current. (**b**) Capacitor voltages.

Figure 12. Response of the system in conditions of changing load parameters.

A comparison between a conventional MPC and the improved MPC is carried out to prove the effectiveness of the proposed method. Figure 13a,c shows phase voltage and line voltage while using the conventional MPC method. These voltages attain a high voltage jump with amplitude V_{dc} in their waveforms. In contrast, when applying the improved MPC algorithm, the voltage slope steepness of phase voltage reduces its maximum value to $0.5V_{dc}$, a half of the previous case, as shown in Figure 13b. The improvement can be also seen in the line-to-line voltage, as shown in Figure 13d.



(**a**) Phase voltage V_{AN} using normal MPC.

(**b**) Phase voltage V_{AN} using improved MPC.

(**c**) Line voltage V_{AB} using normal MPC.

(**d**) Line voltage V_{AB} using improved MPC.

Figure 13. The phase voltage and line voltage using normal MPC and improved MPC for asymmetric 3-level inverter.

For evaluation of output quality, the graph comparing the THD curve of the load current between the conventional MPC and the improved MPC is illustrated in Figure 14. The proposed algorithm produces output line voltages with lower THD than that of the normal MPC. For example, at $i_{ref} = 2$ A, the THD value of the improved MPC is 1.18% and 1.33% for the normal MPC. This translates to a more than an 11% improvement of load current THD. Likewise, at $i_{ref} = 3.5$ A, the THD values are 0.77% and 0.85% for improved MPC and normal PMC, respectively.

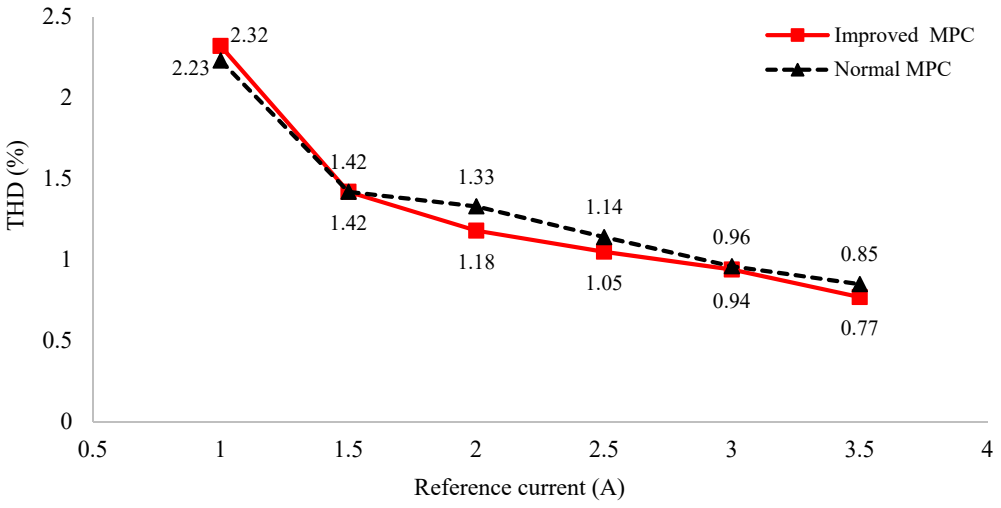


Figure 14. Graph of THD comparison of normal MPC and improved MPC for asymmetric 3-level inverter.

For a better view, the total harmonic distortion performance of the asymmetric T NPC 3-level inverter is also compared with traditional 3-level and 2-level inverters. Figure 15

clearly shows that the load current THD of the asymmetric T-type NPC inverter is much better than that of the 2-level inverter, but slightly worse than that of the conventional 3-level inverter.

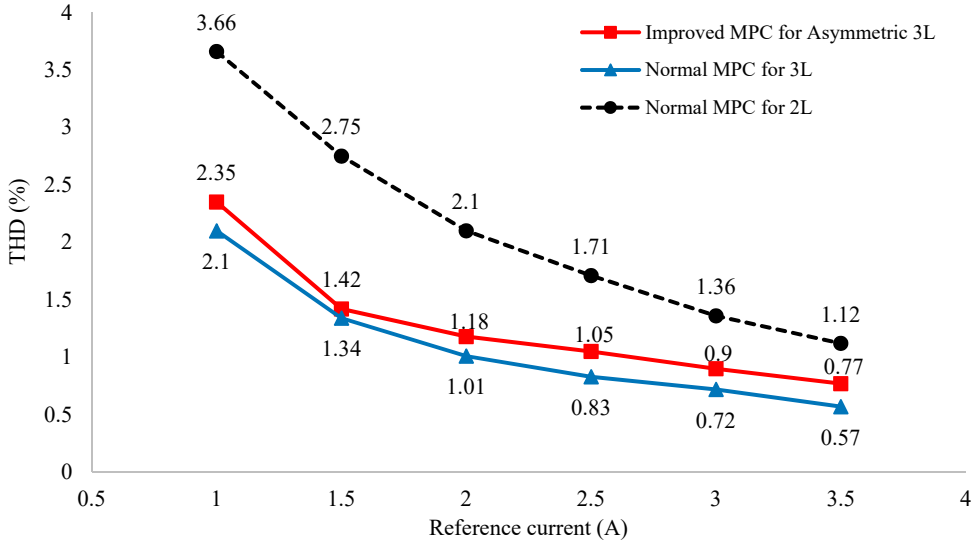


Figure 15. Graph of THD comparison of asymmetric 3-level, conventional 3-level, and 2-level inverter.

Another benefit of the proposed MPC can be demonstrated in switching frequency. Figure 16 shows the average switching frequency curves of the conventional MPC algorithm and the improved MPC for the asymmetric inverter configuration. For example, at $i_{ref} = 3$ A, the average switching frequency of the improved MPC algorithm is 2.56 kHz, while that of the normal MPC algorithm is 2.94 kHz. It gives a reduction of about 13% switching frequency. Similar results are also obtained for the remaining load currents. For more detail, Figure 17a illustrates the switching frequency distribution among switching devices of the conventional MPC method, which is less uniformly distributed than that of the improved MPC algorithm, as shown in Figure 17b, which possibly leads to failures in some switching devices that have to experience a considerable amount of switching frequency over a long-term operation [33].

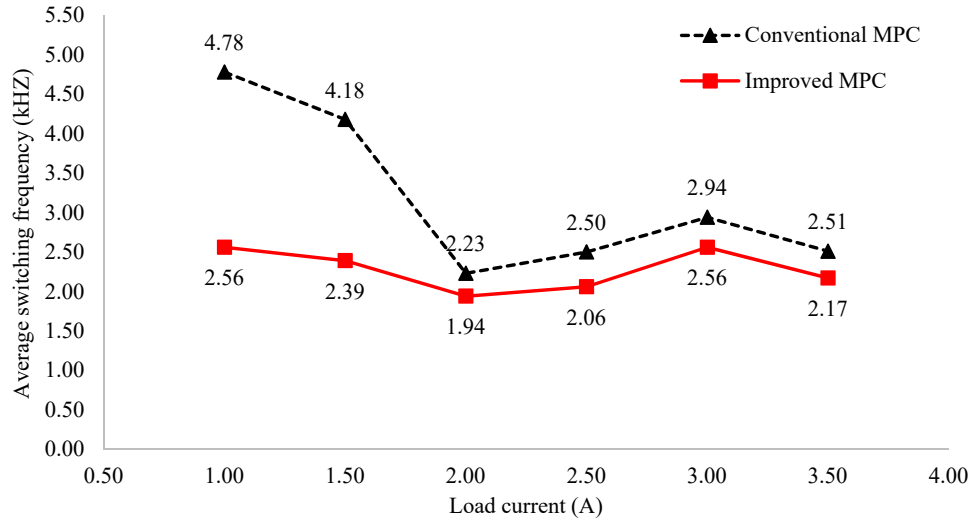


Figure 16. Average switching frequency comparison of normal MPC and improved MPC for asymmetric 3-level inverter.

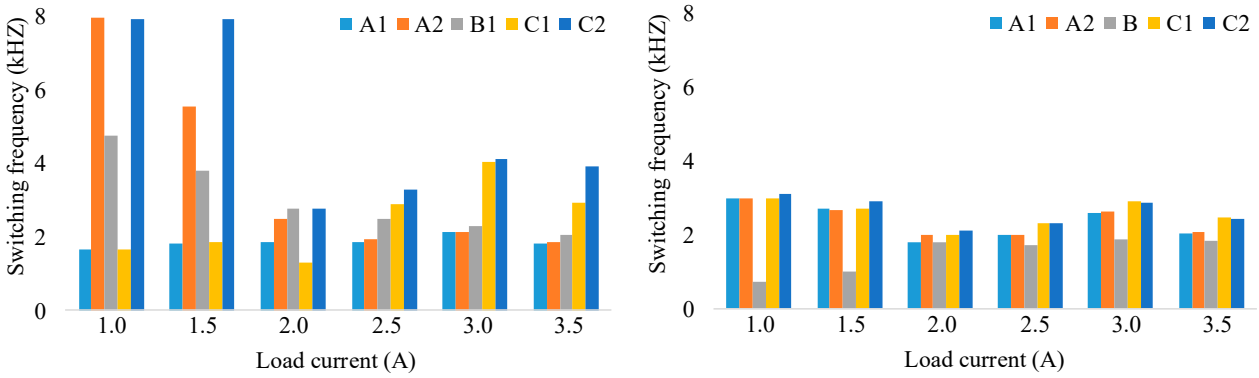


Figure 17. The switching frequency distribution among switching devices.

4.2. Experimental Results

To verify the effectiveness of the asymmetric T-type NPC inverter when applying the improved MPC algorithm, experiments are performed for both transient and steady-state conditions. A laboratory model was built, as shown in Figure 18, including: ① a digital signal processor TMS320F28379D to perform algorithms built-in Matlab/Simulink environment with Embedded Coder Support Package for TI C2000 Processors; ② the inverter is made from TOSHIBA's IGBT GT50J325-type; ③ IGBT driver circuit uses QP12W08S-37 type; ④ DC-bus voltage is fed from 2 capacitors 1200μf-450VDC;⑤the load R = 25 Ω, L = 50 mH;⑥Tektronix TDS2024C oscilloscope. The detailed parameters are listed in Table 5.

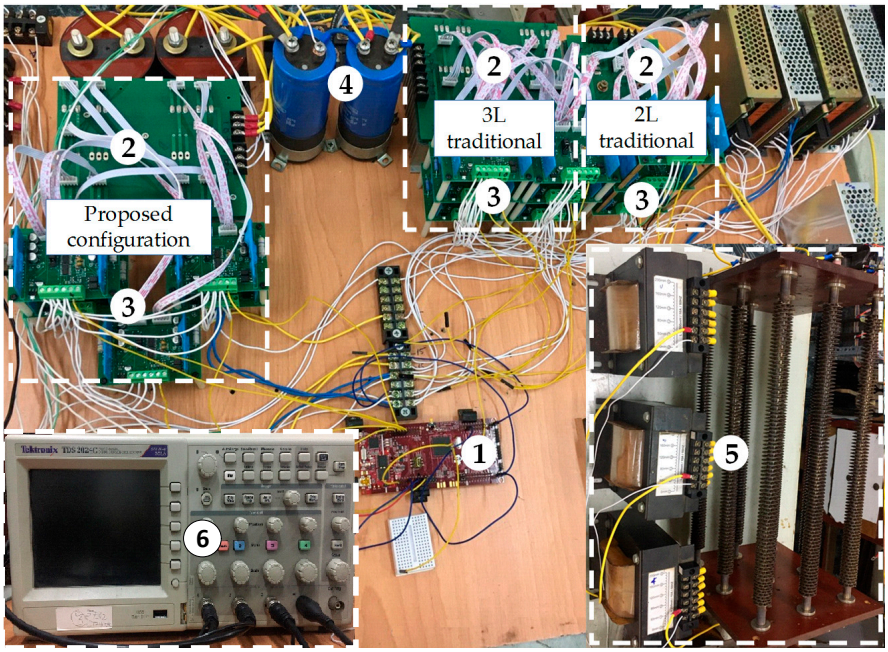
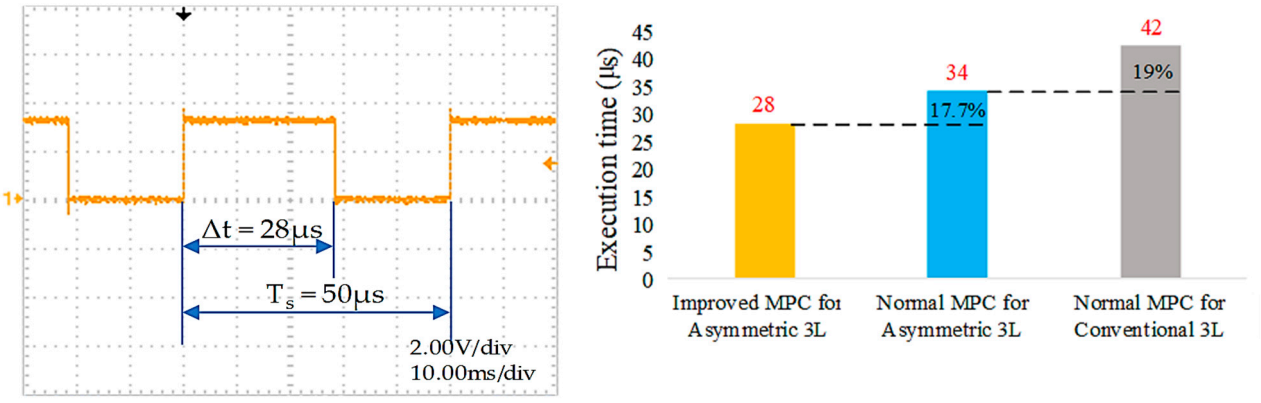


Figure 18. Experimental model in the laboratory.

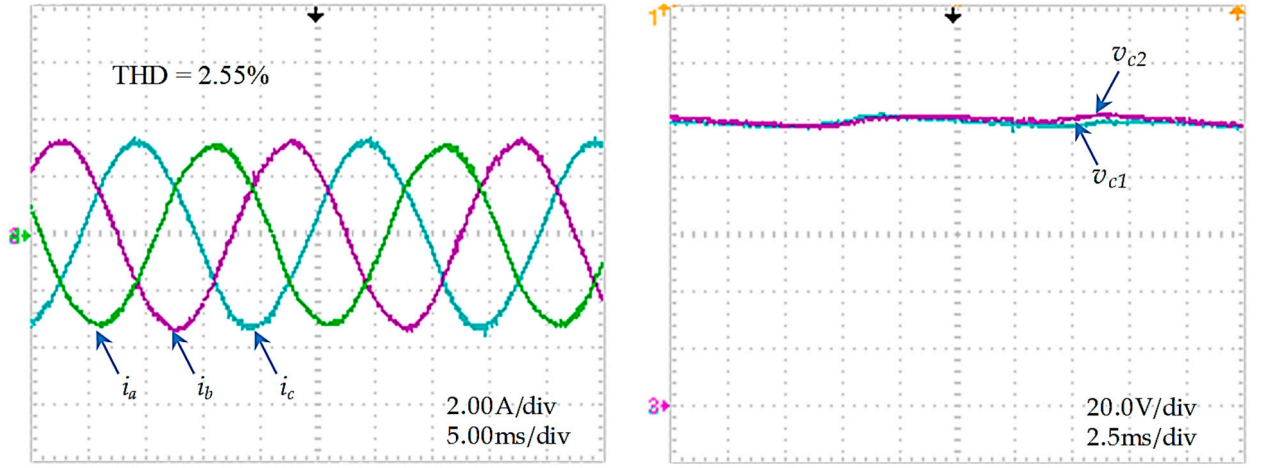
The digital signal processing (DSP) generates the signals for switching devices of the inverter via general-purpose input/output (GPIO) outputs at sampling time 50 μs and DC-bus voltage at 200 V. The execution time efficiency of the improved MPC algorithm for the asymmetric inverter configuration has been demonstrated by the results shown in Figure 19. It can be seen that the conventional MPC algorithm for asymmetric 3-level inverter takes about 34 μs, which is about 19% less compared with a conventional 3-level inverter, as presented in Figure 19b. Meanwhile, the improved MPC method takes about 28 μs, as shown in Figure 19a, improving by about 17.7% compared to a conventional MPC.



(**a**) Improved MPC for Asymmetric inverter. (**b**) Comparison graph of execution time.

Figure 19. Execution time.

The steady-state current responses are sinusoidal and stable at a set-value 3 A with THD about 2.55%, as illustrated in Figure 20a. The capacitor voltages are maintained in good balance, as shown in Figure 20b.

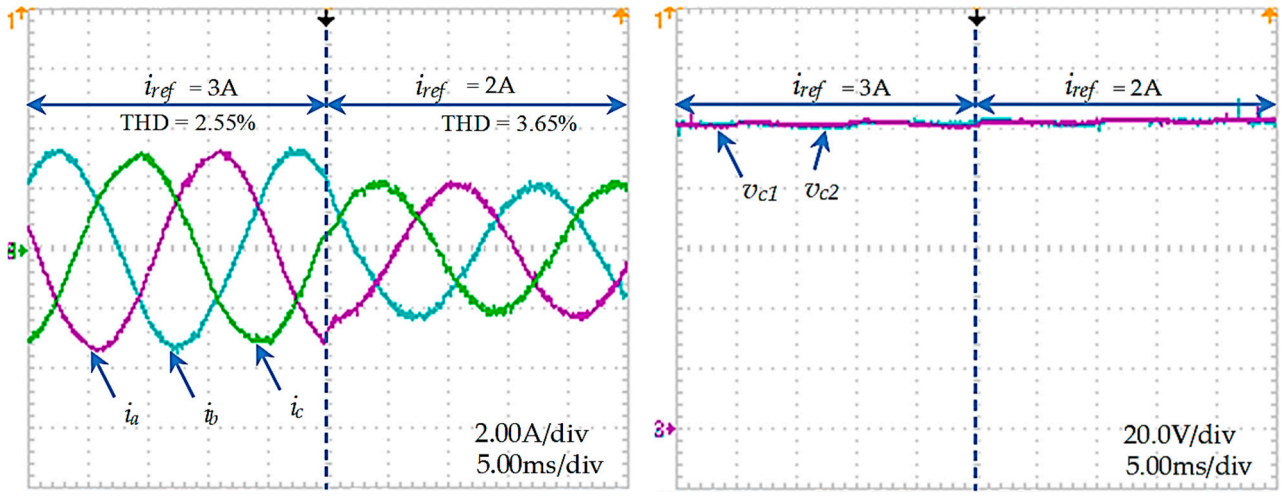


(**a**) Three phase load current. (**b**) Capacitor voltages.

Figure 20. Steady−state of the improved PMC method for an asymmetric T-type NPC inverter.

Another experiment on changing the reference current was also performed. The reference current is initially set at 3 A, then suddenly changed to 2 A. The capacitor voltages are stable at balance, as shown in Figure 21b. The current response quickly reached a steady state at the reference value, with THD increasing from 2.55% to 3.65%, as presented in Figure 21a.

Similar experiments were also carried out on 2-level and conventional 3-level inverters for comparison, and the results are shown in Figure 22. For example, at $i_{ref} = 3$ A, the current load THD of the asymmetric inverter is 2.55% compared with 2.7% of the 2-level inverter and 2.42% of the 3-level inverter. The THD increased to 4.45% at $i_{ref} = 1.5$ A for the asymmetric inverter, compared with 4.92% and 4.09% of the 2-level inverter and 3-level inverter, respectively. The load current THD of the asymmetrical T-type NPC inverter was not as good as the 3-level inverter although better than the 2-level inverter. The characteristics in Figure 22 are similar to those of the simulation shown in Figure 15.



(**a**) Three phase load current. (**b**) Capacitor voltages.

Figure 21. Transient response of the improved PMC for an asymmetric T-type NPC inverter.

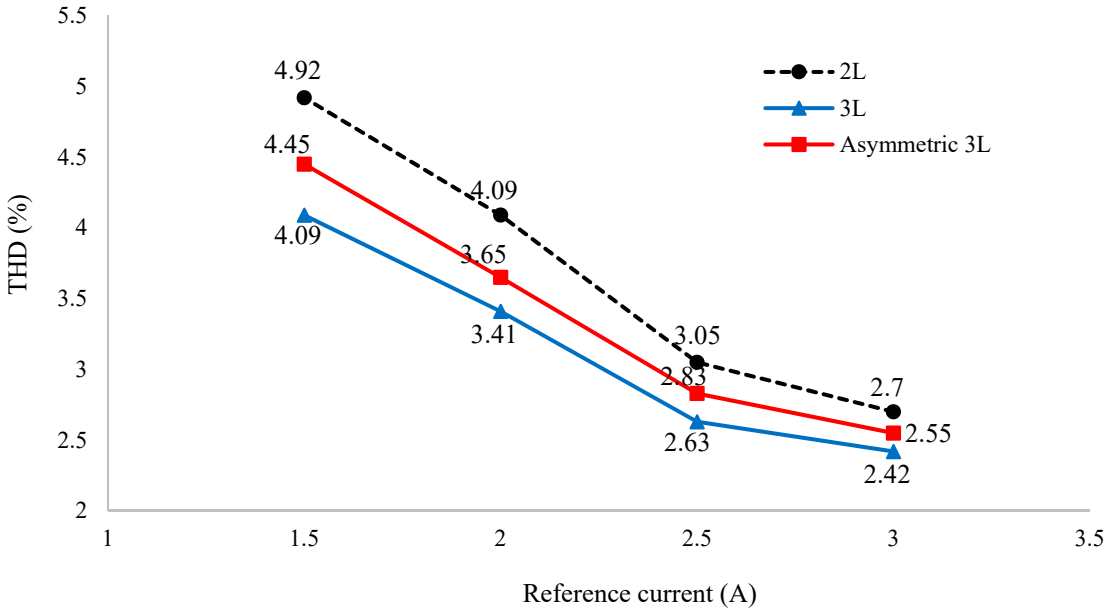


Figure 22. Experimental results of THD comparison of asymmetric 3-level, conventional 3-level, and 2-level inverter.

5. Conclusions

This paper presented the asymmetric T-type NPC inverter topology. An improved predictive control strategy is proposed to control this configuration. A comparative evaluation of output current performances between asymmetric 3-level T-type, conventional 3-level, and 2-level inverters was performed. Simulation and experimental results have demonstrated the benefits of the asymmetric inverter when controlled by the improved MPC algorithm. The proposed MPC also proves to be better than the conventional MPC for a shorter execution time. Applying the proposed MPC method, the load current THD of the asymmetric inverter is obviously better than the 2-level inverter, and its quality is close to that of the traditional 3-level inverter. Therefore, the asymmetric 3-level inverter is shown to be attractive for applications that require the full range of output voltage and low harmonic distortion like the traditional 3-level inverter, but at a lower cost. Furthermore, in another application, control of this topology can be applied for a conventional 3-level NPC in faulty situations where one T-leg connected to the neutral point is faulty and open.

For simplicity, the paper presents the improved MPC method for RL load. In order to ensure its use in real-life applications such as electrical motor drives and utility converter systems, further studies are needed such as analysis and modeling of the whole system fed by asymmetrical inverter and control design with IMPC algorithm and system stability issue. In addition, the overall performance of IMPC will be further assessed by executing a comparative study with linear controllers based on PWM.

Author Contributions: Formal Analysis by N.V.N., Investigation by N.X.D., Software by N.X.D., Supervision by N.V.N., Validation by N.V.N., Writing—Original Draft by N.X.D., Writing—Review and Editing by N.V.N. All authors have read and agreed to the published version of the manuscript.

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