Article

Dual-Frequency RF Impedance Matching Circuits for Semiconductor Plasma Etch Equipment

Jeongsu Lee and Sangjeen Hong *

Department of Electronic Engineering, Myongji University, Seoul 17058, Korea; wjftn123@gmail.com

* Correspondence: samhong@mju.ac.kr

Abstract: The change in electrode impedance of semiconductor equipment due to repetitive processes is a major issue that creates process drift. In the current plasma etch chamber with a dual-frequency power system, the high-powered radio frequency (RF) source contributes to the enhancement of the plasma density, and the low-frequency bias power at the bottom electrode is adopted to enhance the injected ion energy in the plasma. The impedance control of the top electrode in dual-frequency capacity coupled plasma limits the impedance matching capability of the RF matching system because it only considers the high-frequency RF source. To control the precise impedance in dual-frequency semiconductor equipment, independent impedance control is required for each frequency. In this study, the impedance corresponding to a specific frequency was independently controlled using L (inductor) and C (capacitor). A 60 MHz stop filter and VVC were used to control 2 MHz impedance at a specific point, and a 2 MHz stop filter and VVC were used to control 60 MHz impedance. In the case of 2 MHz impedance control, the 2 MHz impedance changed from $10.9 - j893$ to $0.3 - j62$ and the 60 MHz impedance did not change. When controlling the 60 MHz impedance, the 60 MHz impedance changed from $0.33 + j26.53$ to $0.2 + j190$ and the 2 MHz impedance did not change. The designed LC circuits cover the impedance of 60 and 2 MHz separately and are verified by the change in the capacitance of the vacuum variable capacitors implemented in the RF impedance matching system.

Citation: Lee, J.; Hong, S.Dual-Frequency RF Impedance Matching Circuits for Semiconductor Plasma Etch Equipment. *Electronics* **2021**, *10*, 2074. <https://doi.org/10.3390/electronics10172074>

Academic Editor: Fabian Khateb

Received: 9 August 2021

Accepted: 25 August 2021

Published: 27 August 2021

Publisher's Note: MDPI stays neutral with regard to jurisdictional claims in published maps and institutional affiliations.

Copyright: © 2021 by the authors. Licensee MDPI, Basel, Switzerland. This article is an open access article distributed under the terms and conditions of the Creative Commons Attribution (CC BY) license (<https://creativecommons.org/licenses/by/4.0/>).

Keywords: dual-frequency capacitively coupled plasma; process drift; impedance matching

1. Introduction

The requirement for a higher performance of semiconductor equipment is continuously growing with the increased demand for a more precise control of plasma process equipment to satisfy the next level of device technology of dynamic random-access memory and three-dimensional (3D) NAND flash memory [1–3]. Plasma process equipment normally applies radio frequency (RF) powers to generate the plasma, and the frequency and power magnitudes vary with the chamber size and the process applications [4]. Among the various plasma processes, plasma etch requires an increased degree of selectivity, anisotropy, and critical dimension uniformity control to realize next-generation high-performance semiconductor devices.

The dry etch process using plasma must supply power to the electrode to make a smaller semiconductor. Making plasma using DC follows a process, but RF power is mainly used to shorten the process time and solve problems caused by the electrode charge. The frequency mainly used by semiconductors is 13.56 MHz. However, the semiconductor process becomes complicated, and the process time is extended because of the 3D device geometry with a high aspect ratio. To alleviate this problem, several studies are being conducted to increase the frequency and improve the plasma uniformity. Plasma is generated by accelerating and colliding electrons with process gas molecules, such that the electron density is related to the plasma density [5]. The dual-frequency capacitively coupled plasma (CCP) etch device currently accelerates electrons by applying RF power to two electrodes. Some ions are ionized by receiving sufficient energy from

electrons and radicals that can easily react with surrounding substances because of the high energy that cannot be ionized. The plasma materials mainly used in the etch process are ions and radicals. Ions mainly use physical methods, whereas radicals use chemical reactions for etching [6]. The electron collision must be increased, and the collision energy must be high. When a high-frequency RF power is applied to the electrode, the number of electron collisions increases; thus, the plasma density increases. High frequencies can increase radical production rates because of the elastic collision of electrons, which process processes through chemical reactions with ions. Due to this characteristic, studies using very high frequencies (VHFs) are being conducted [7,8].

An impedance matching unit is a key component that uniformly transmits power to load. Since the chamber where plasma is generated has a difference from the impedance coming from the RF generator, if it is not matched, power is reflected, and power loss occurs. This is an important factor in the process because it has a great effect on the constant plasma.

A commonly used impedance matching circuit performs impedance matching using L and C. L-type, T-type, and π -type are found in the impedance matching circuit. L-type uses two components, it but has a disadvantage in that the matching capability is small. T-type and π -type have wider impedance matching capability than L-type. [9] In RF-front-end transceivers, RF impedance matching maintains a small power loss and requires impedance matching even in a wide bandwidth, so studies on material change and adaptive algorithm improvement are continuing [10,11]. As such, In dual-frequency semiconductor equipment, VVC is used to withstand high power, and frequency tuning and electronic matchers are being developed to increase matching speed. A mismatched RF impedance can be a cause of process drift and fault. The RF matching unit performs impedance matching such that the impedance viewed from the RF generator becomes 50 Ω . The RF impedance matching unit recognizes the remaining parts, except the RF generator, as load impedance. A variable vacuum capacitor (VVC) has limitations in capacity and reliability guarantee and physical limitations, such as heat generation, noise, and size. The RF impedance matching unit manufacturers design and manufacture matching units for specific equipment and processes. Thus, an impedance matching region corresponds to a specific semiconductor device, and the load impedance must be in the impedance matching region. If a process drift occurs, and the load impedance is out of the matching region, the impedance matching is unreliable and can severely fail to match. The loss of power supplied from the RF generator increases in the form of a reflection if impedance matching fails. Consequently, the plasma stability is perturbed, and the possibility of a process failure increases. Process drift is a major cause of dynamic plasma impedance change under an impedance mismatch.

To alleviate the above concern, improvement involves applying a circuit capable of impedance control to the electrode [12]. However, in semiconductor equipment using dual frequency, controlling the impedance with one variable capacitor is challenging. Moreover, the larger the difference between frequencies, the smaller the impedance change range. Thus, this study proposes an impedance controller circuit that independently controls two frequencies using at least two VVCs.

2. RF Power in the Plasma System

Figure 1 is a simple diagram of dual-frequency semiconductor equipment. Figure 1a is a capacitively coupled plasma (CCP), which generates plasma using RF power to two electrodes. Figure 1b is an inductively coupled plasma (ICP) that generates plasma by using RF power to the upper antenna (coil) and bottom electrode. RF power is supplied with a precise RF frequency and power from an external RF generator. The RF impedance matching unit reduces power loss by matching the load impedance change due to plasma to 50 Ω and helps supply constant power. Plasma is a collection of ionized gas species in a volume with external energy in a pressure condition. The plasmas in semiconductor processing can be generated by external RF power. The net movement of electrons in

the plasma allows a current path between two powered electrodes in an electrical circuit model. Depending on the type of plasma generation source (e.g., inductively coupled plasma and CCP), the ionized gas species can be modeled with a resistor–capacitor and resistor–inductor dominant impedance circuit. Unlike conventional lumped elemental electrical circuits, the plasma impedance continuously changes along the degree of molecular dissociation and atomic ionization. The delivered RF power to the wafer-in-process via plasma also continuously changes. What matters is that the total amount of delivered power should be maintained consistently over consecutive individual runs to obtain a consistent process result, as shown in Figure 1a,b. Thus, the impedance matching network is indispensable in plasma process equipment.

Figure 1. Plasma chamber schematic diagram: (a) capacitive coupled plasma and (b) inductively coupled plasma.

Electrons have a relatively smaller mass than ions; thus, they can be controlled independently using different frequencies. Previous studies showed that the electron density increases with the increasing frequency. When the bottom electrode is fixed at 2 MHz and 10–100 MHz frequency is supplied to the top electrode, the number of electrons is gradually increased. Accordingly, the number of electrons also increases as the source frequency increases [13]. In previous studies, when the ion supplies 27 MHz to the top electrode and a frequency of 1–100 MHz to the bottom electrode, the ion density decreases as the frequency increases; however, no change is observed as the frequency increases [14]. This confirms that electrons and ions can be controlled independently.

The ion flux and energy are essential parameters for the etch profile of the high aspect ratio. The production speed is generally fast in plasma with many ions and high energy. High plasma density, high ion flux, and large ion energy are important. The ion flux can be increased by increasing the plasma density; thus, it supplies a high frequency to the source power. A frequency of 13.56 MHz is often used as a source power. However, the ion energy is greater than the ion flux, which damages the substrate and is not used well but uses a higher frequency [15]. A frequency of 60 MHz can increase the ion flux while reducing the ion energy to some extent. If a frequency higher than 60 MHz is supplied, a standing wave and skin effects occur, resulting in a poor plasma uniformity, which makes it difficult to make a high-aspect-ratio shape.

The frequency supplied to the bias power is often used to control the ion characteristics. Bias power is used in various ways from 400 KHz to 20 MHz, but high frequencies are not used well because the ion energy rapidly decreases when it exceeds 20 MHz [16]. In the dual-frequency capacity coupled plasma (DF-CCP) equipment in the etch process, 2 MHz of bias power is the most common because high selectivity can be produced through ion transition. The source and bias powers affect each other. The frequency selections considered in this research are 13.56 MHz/2 MHz, 27.12 MHz/2 MHz, 40 MHz/2 MHz,

and 60 MHz/2 MHz of the source/bias frequency. The 60 MHz/2 MHz combination must be investigated because it is the most preferred combination for the silicon dioxide etcher manufactured by a domestic equipment industry.

This frequency combination of RF generators belongs to a VHF. Even a small impedance change of the electrode can significantly influence the plasma. The physical size of dies decreases as the miniaturization of the semiconductor device technology continues. Consequently, the process yields at the wafer edge region became more interesting by reducing the center to edge variation. For instance, the allowable gate critical dimension variation is less than 2.4 nm in the 14 nm technology node and 0.5 nm in the next-generation 5 nm technology node. The process variation has become more important than ever. In semiconductor etch equipment, plasma is formed between two electrodes in a circular shape, and the plasma faces the surrounding wall or object with a plasma sheath, where the number of ions is much less than that in bulk plasma. Hwang et al. defined three types of plasma discontinuities between the wafer edge and the edge ring: (1) electrical discontinuity, (2) chemical discontinuity, and (3) thermal discontinuity [17].

Electrical discontinuity leads to plasma sheath bending. The ion trajectory in the child Langmuir region is perpendicular to the plasma sheath, and the bended sheath causes the ion injection direction to yield an undesired etch pattern at the edge [18]. The materials for the edge ring (e.g., quartz, silicon, and silicon carbide) are etch-resistive, and the etch rate of the edge ring is much retarded compared with the materials to be etched on the wafer. The bended-down electric field outside the wafer edge region (or near the edge ring region) lowers the electric field perpendicular to the wafer surface. It yields a lowered ion flux while the neutral flux increases [19]. One may imagine that the amount of by-product and the associated ion densities on the wafer side are larger than those of the edge ring. Therefore, it causes a chemical discontinuity in case etch rate variation in the wafer edge region. In terms of temperature, the electrostatic chuck (ESC) maintains a consistent temperature during the etch, but the actual wafer surface temperature is much higher than that of the ESC under temperature control. The current etch equipment applies a temperature-controlled edge ring; however, a temperature gradient exists between the wafer edge and the edge ring [20–22]. Although a symmetric chamber has been designed with the consideration to overcome three types of discontinuity, the variations in the current process requirement are difficult to overcome.

An electrode supplies the power required for the plasma generation and is directly connected to the wafer. Some studies focused on plasma control using these electrodes. One study controlled the current flowing through the plasma by inserting an impedance control circuit into the bottom electrode. In the DF-CCP using 60 and 13.56 MHz, impedance was created by directly inserting an impedance control circuit between the bottom electrode and the RF matching circuit. The current flowing through the plasma can be controlled, and a stable plasma can be formed [23]. However, the impedance range is limited because the control of the two frequencies is carried out by one capacitor. The deposition process demonstrates plasma control with impedance control of the electrode. An impedance controlling circuit is included in the chamber wall and the bottom electrode to reduce the film stress and uniformity. Controlling the plasma impedance at the chamber wall reduces the plasma radiation pattern. The impedance control at the bottom electrode also improves the RF field formed by the plasma [24]. Research was also conducted to control plasma characteristics using a resonance circuit that blocks the flow of a specific frequency in the electrode. In the CCP equipment, 2, 27, and 60 MHz were supplied to the bottom electrode, and an impedance control circuit was inserted to block a specific frequency in the top electrode. The changes in the ion density and etch rate were then checked. The uniformity of the ion density and the etch rate can be improved by blocking and passing the specific frequency signals flowing through the electrode [25,26]. The abovementioned results confirmed that the electrode in the CCP equipment is an essential factor affecting the etch process and plasma. However, repeating the etch process damages the electrode and changes the impedance.

3. Impedance Matching Circuit

A filter is essential for extracting the desired electrical signals by selecting the desired frequency information among various frequencies. This filter can select and cut off the frequency only by the operation characteristics and the combination of inductors and capacitors. In the semiconductor equipment, filters composed of capacitors and inductors are commonly used to protect the circuits of the semiconductor equipment components. These filters protect the RF generator by allowing only the frequency of the components that the internal circuit of the RF generator can withstand to flow. A filter is also used in a voltage–current (VI) sensor to detect the voltage and current components occurring at a specific frequency. A filter is designed using the inductor and capacitor device characteristics.

$$X_L = j\omega L, X_C = -j\omega C, \text{ and } \omega = 2\pi f$$

X_L is the impedance according to the inductor value, and X_C is the impedance according to the capacitance. The higher the frequency, the larger the X_L value and the smaller the X_C ; hence, the low-frequency signal flows well in the inductor, and the capacitors have the property of the high-frequency signal flowing well. The capacitor has a negative impedance, whereas the inductor has a positive impedance. Using this, one can adjust the total impedance of a specific circuit and the impedance of a specific frequency. Resonance is a representative example of good usage. It occurs because of the device's charging and discharging characteristics and acts to pass or block specific frequencies. The resonant frequency is the point where the imaginary impedance becomes 0, and the following formula is satisfied:

$$X = j\omega L - j1\omega C = 0, \omega^2 = 1/LC, \text{ and } f = 1/LC$$

f is the resonance frequency. Different phenomena occur depending on the arrangement. A filter uses this resonance phenomenon and the device characteristics to make the desired frequency impedance close to 0 and pass it through and can make a circuit that cuts off the unwanted frequency.

The concept of the dual-frequency RF impedance control circuit is like that of a diplexer, but the output ports are connected to VVCs for capacitance modification. The control of the VVC capacitance makes the pulse width modulation of the stepping motor connected at the end of the VVC. Figure 2 depicts the conceptual diagram of the suggested dual-frequency RF impedance control circuit. The LC filter design requires the selection of the type of filters and the determination of the inductance and capacitance values. Considering the frequency responses of the inductor and the capacitor, the physical limitations of the inductance due to the increased parasitic capacitance from the space of the inductor coil and the capacitance were determined as 60 μ H and 22–1000 pF, respectively, as a rule of thumb by RF engineers. We performed herein a stepwise circuit simulation study to have the desired impedance control circuit for the dual-frequency RF power system. RF filter circuit models were investigated with VVC1 connected to a 2 MHz signal path and VVC2 to a 60 MHz path. We investigated the crosstalk of the two signal paths within the normal capacitance range of the VVC between 100 and 1000 pF. Observing the capacitance change in the fixed capacitance of VVC2 while the capacitance of VVC1 was varied showed the impedance control functionality of the dual-frequency RF impedance matching circuits. Meanwhile, it is valuable to ensure that the circuit has no crosstalk beyond the normal operating capacitance. We also studied the extended capacitor range of VVCs from 100 to 100,000 pF. Table 1 presents a summary of the simulation routines.

Figure 2. Conceptual block diagram of the proposed dual-frequency impedance control circuit.

Table 1. Performance summary (measurements).

Simulation Routine	Normal Capacitance Range	Extended Capacitance Range	Comments	Note
Design 1	60 MHz 2 MHz		Significant crosstalk in extended range	Figure 3
Design 2	60 MHz 2 MHz	Variable VVC1 Fixed VVC2	Small amount of crosstalk in normal/extended range	Figure 4
Design 3	60 MHz 2 MHz	(100–1000 pF) (100 pF)	Small in normal range Negligible in extended	Figure 5
Design 4	60 MHz 2 MHz		Negligible in all fixed VVC2 and VVC1	Figure 6

Figure 3. RF filter circuit Design 1: (a) conceptual diagram, (b) designed filter circuit, (c) impedance simulation under 100~1000 pF of the normal capacitance range, and (d) impedance simulation under 100~1,000,000 pF of the extended capacitance range. The figures intend to demonstrate the effect of the variation of the 2 MHz VVC on the fixed 60 MHz capacitance and that of the 60 MHz VVC on the fixed 2 MHz capacitance.

Figure 4. RF filter circuit Design 2: (a) conceptual diagram, (b) designed filter circuit, (c) impedance simulation under 100~1000 pF of the normal capacitance range, and (d) impedance simulation under 100~1,000,000 pF of the extended capacitance range. The figures intend to demonstrate the effect of the variation of the 2 MHz VVC on the fixed 60 MHz capacitance and that of the 60 MHz VVC on the fixed 2 MHz capacitance.

Figure 5. RF filter circuit Design 3: (a) conceptual diagram, (b) designed filter circuit, (c) impedance simulation under 100~1000 pF of the normal capacitance range, and (d) impedance simulation under 100~1,000,000 pF of the extended capacitance range. The figures intend to demonstrate the effect of the variation of the 2 MHz VVC on the fixed 60 MHz capacitance and that of the 60 MHz VVC on the fixed 2 MHz capacitance.

Figure 6. RF filter circuit Design 4: (a) conceptual diagram, (b) designed filter circuit, (c) impedance simulation under 100~1000 pF of the normal capacitance range, and (d) impedance simulation under 100~1,000,000 pF of the extended capacitance range. The figures intend to demonstrate the effect of the variation of the 2 MHz VVC on the fixed 60 MHz capacitance and that of the 60 MHz VVC on the fixed 2 MHz capacitance.

Design 1 is a simple parallel combination of an LPF for the 2 MHz signal and an HPF for 60 MHz in Figure 3. The figures intend to demonstrate the effect of the variation of the 2 MHz VVC on the fixed 60 MHz capacitance and that of the 60 MHz VVC on the fixed 2 MHz capacitance. The interest is in the observations of the crosstalk in the fixed VVCs in the proposed circuits, which are depicted by dotted circles in the presented Smith charts and denoted by fixed VVC1 and VVC2 throughout the Smith chart figures. Design 1 shows a relatively acceptable performance with a small amount of capacitance variation of the fixed VVC2. It also, however, demonstrates a notable change in the fixed VVC1 for 2 MHz, whereas the VVC2 connected to 60 MHz varies from 100 to 1000 pF. Therefore, both 2 and 60 MHz impedance control circuits are not independently functioning with some crosstalk, and Design 1 is not suitable for controlling the dual-frequency RF impedance system.

Double-frequency blocking circuits are considered in Design 2 to alleviate the crosstalk observed in Design 1 in Figure 4. For the 2 MHz VVC1 circuit, the high-frequency components were blocked with a very small inductance. For the 60 MHz VVC2 circuit, the low-frequency components were blocked with a very large capacitance. Additionally, by-passing band pass filters were added to the ground to quench out the undesired signals. The same simulation routine for the crosstalk visualization in both VVC2 and VVC1 was obtained. Unlike our postulation of the signal by-pass, we observed a small amount of crosstalk for both the fixed VVC2 in the normal capacitance range and the fixed VVC1 in the extended range. Thus, Design 2 may be acceptable for the dual-frequency RF matching system that requires intermediate accuracy but not suitable for the current high-end precision RF system.

Learning from the previous filter designs, the band pass filters of 2 and 60 MHz were considered in Design 3, as shown in Figure 5, applying series resonance circuits. The corresponding impedances of the 2 MHz circuit block were $-j0.072 \Omega$ (short) for 2 MHz and $-j2345 \Omega$ for 60 MHz (open). The corresponding impedances of the 60 MHz circuit block were $-j3613 \Omega$ (open) for 2 MHz and $-j0.027 \Omega$ for 60 MHz (short). The simulation result was relatively satisfying with a negligible crosstalk in the extended capacitance range but still suffered from the cut off frequency whose impedance was lower than that obtained using parallel resonance. The impedance range may be limited if the impedance is small enough. Having a large impedance is efficient. However, the disadvantage of the band pass filter can be overcome with the band stop filter.

Design 4 presented in Figure 6 with band stop filters was investigated with the parallel connection of an inductor and a capacitor. Allowing a 2 MHz signal transmitted by blocking 60 MHz signals for the 2 MHz control circuit, the 60 MHz impedance should be close to infinity as an open circuit, whereas the 2 MHz impedance is better when smaller. If the 60 MHz signal does not flow through the circuit, the impedance change by the influence of VVC1 is negligible. By contrast, the opposite phenomenon is expected for the 60 MHz impedance control circuit. We investigated both cases of impedance changes in the fixed VVC2 while the VVC1 was varied from 100 to 1000 pF and that in the fixed VVC1 while the VVC2 was varied from 100 to 1000 pF. Figure 6c depicts the result. No crosstalk was observed in both cases, implying that the two parallel connected band stop filters can independently control the dual-frequency impedance circuit. The extended capacitance range of 100–100,000 pF was also tested, as shown in Figure 6d, and the same results were achieved. We implemented the dual-frequency control circuits based on the achieved result shown in Figure 6. The performed actual measurement is presented in the next section.

4. Circuits Implementation

Actual circuit implementation was followed based on the designed RF filter theory and the simulation result. The test circuit of the 2 MHz impedance circuits includes a 22 pF capacitor supplied by American Technical Ceramics and a 319 nH hand-made inductor. That of 60 MHz comprises 1000 pF of the capacitor and 6.3 μ H of the inductor, as the same method, as shown in Figure 7. Figure 8 shows an experiment to determine if only the 2 MHz impedance is controlled by the impedance. The VVC was controlled through a control computer and measured using a network analyzer (E5071C, Agilent Technology: Santa Clara, CA, USA). The change in impedance at 60 MHz and the impedance result of 2 MHz were confirmed with a Smith chart. In Figure 8b, no impedance change was observed in the 60 MHz circuit while the 2 MHz impedance was varied by the connected VVC. Figure 9 shows the measurement result with the fabricated test circuit and presents no impedance change in the 2 MHz circuit with the capacitance varying in 60 MHz. Thus, we are convinced that the suggested RF filter is suitable for 2 and 60 MHz of dual-frequency RF impedance control circuits.

Figure 7. Implementation of the impedance controller filter.

Figure 8. Implemented 2 MHz impedance control circuit and impedance measurement with a network analyzer. No crosstalk was observed in the 60 MHz circuit while the VVC for 2 MHz was varied. (a) Realized circuit and (b) measured responses.

Figure 9. Implemented 60 MHz impedance control circuit and impedance measurement with a network analyzer. No crosstalk was observed in the 2 MHz circuit while the VVC for 60 MHz was varied. (a) Realized circuit and (b) measured responses.

5. Conclusions

This study proposed an RF filter circuit design for dual-frequency RF impedance control to improve the wafer uniformity in the plasma etch process by independently controlling the chamber impedance between the source electrode or antenna and the bottom electrode via reactive plasma. The increasing complexity of semiconductor processes and chamber damage caused by strong ionic energy in the etching process is increasing, affecting not only the chamber but also the wafer inside the chamber and the electrode impedance, which is a semiconductor component. This change affects the plasma uniformity by changing the load impedance and changing the part for the plasma uniformity. The control range is small because the frequency-dependent impedance cannot be controlled independently. This study proposed an impedance control circuit according to several frequencies. We confirmed through an experiment that the impedance corresponding to different frequencies independently changes. Thus, we believe that it is possible to prevent process drift by improving the impedance change of the semiconductor equipment components caused by plasma.

Author Contributions: Conceptualization, principal investigation and supervision, funding acquisition, writing—review and editing, S.H.; methodology, visualization, data curation, writing—original draft preparation, J.L. Both authors have read and agreed to the published version of the manuscript.

Funding: This work was supported by a Korea Institute for Advancement of Technology (KIAT) grant funded by the Korean Government (MOTIE) (P0008458, the Competency Development Program for Industry Specialists).

Acknowledgments: The authors are grateful to B.K. Jeon at Korea Semiconductor Industry Association for serving as a project leader for POSEER.

Conflicts of Interest: The authors declare no conflict of interest.

References

1. Yamada, N.; Tachikawa, T.; Nagami, K.; Ikenari, T.; Maehara, D. Plasma Processing Apparatus. U.S. Patent 9,355,822, 31 May 2016.
2. Hoffman, D.J.; Brown, K.M.; Rui, Y.; Pipitone, J. Physical Vapor Deposition Chamber with Capacitive Tuning at Wafer Support. U.S. Patent 9,593,411, 14 March 2017.
3. Or, D.T.; Collins, J.; Chang, M. Directional SiO₂ etch Using Plasma Pre-treatment and High-Temperature Etchant Deposition. U.S. Patent 9,245,769, 26 January 2016.
4. Lee, H.-C. Plasma Diagnostic Technology for Semiconductor and Display Process Industries. *Vac. Mag.* **2018**, *5*, 19–27. [\[CrossRef\]](#)
5. Kim, J.; Lee, S.W. Impedance Matching Method and Impedance Matching System. U.S. Patent 10,270,418 B2, 8 April 2013.
6. Singh, H.; Lill, T.; Vahedi, V.; Paterson, A.; Titus, M.; Kamrathy, G. Internal Plasma Grid for Semiconductor Fabrication. U.S. Patent 9,245,761, 26 January 2016.
7. Kim, K.S.; Sirse, N.; Ellingboe, A.; Kim, K.N.; Yeom, G.Y. Characteristics of silicon nitride deposited by VHF (162 MHz)-plasma enhanced chemical vapor deposition using a multi-tile push-pull plasma source. *J. Phys. D Appl. Phys.* **2016**, *49*, 395201. [\[CrossRef\]](#)
8. Kim, K.S.; Kim, K.H.; Ji, Y.J.; Park, J.W.; Shin, J.H.; Ellingboe, A.R.; Yeom, G.Y. Silicon Nitride Deposition for Flexible Organic Electronic Devices by VHF (162 MHz)-PECVD Using a Multi-Tile Push-Pull Plasma Source. *Sci. Rep.* **2017**, *7*, 13585. [\[CrossRef\]](#)
9. Alibakhshikenari, M.; Virdee, B.S.; Shukla, P.; Wang, Y.; Azpilicueta, L.; Naser-Moghadasi, M.; See, C.H.; Elfergani, I.; Zebiri, C.; Abd-Alhameed, R.A.; et al. Impedance Bandwidth Improvement of a Planar Antenna Based on Metamaterial-Inspired T-Matching Network. *IEEE Access* **2021**, *9*, 67916–67927. [\[CrossRef\]](#)
10. Alibakhshikenari, M.; Virdee, B.S.; Shukla, P.; See, C.H.; Abd-Alhameed, R.A.; Falcone, F.; Limiti, E. Improved adaptive impedance matching for RF front-end systems of wireless transceivers. *Sci. Rep.* **2020**, *10*, 14065. [\[CrossRef\]](#)
11. Alibakhshikenari, M.; Virdee, B.S.; See, C.H.; Abd-Alhameed, R.A.; Falcone, F.; Limiti, E. Impedance Matching Network Based on Metasurface (2-D Metamaterials) for Electrically Small Antennas. In Proceedings of the 2020 IEEE AP-S/URSI, Montréal, QC, Canada, 5–10 July 2020; pp. 1953–1954.
12. Iwata, M. Plasma Processing Apparatus. U.S. Patent 10,264,662, 16 April 2019.
13. Jeon, M.; Mishra, A.; Kang, S.-K.; Kim, K.; Kim, I.; Lee, S.; Sin, T.; Yeom, G. Characteristics of SiO₂ etching by using pulse-time modulation in 60 MHz/2 MHz dual-frequency capacitive coupled plasma. *Curr. Appl. Phys.* **2013**, *13*, 1830–1836. [\[CrossRef\]](#)
14. Tsai, W.; A Mueller, G.; Lindquist, R.G.; Frazier, B.; Vahedi, V. High selectivity plasma etching of silicon dioxide with a dual frequency 27/2 MHz capacitive radio frequency discharge. *J. Vac. Sci. Technol. B Microelectron. Nanometer Struct.* **1996**, *14*, 3276. [\[CrossRef\]](#)

15. Marot, L.; Moser, L.; Steiner, R.; Erni, W.; Steinacher, M.; Dine, S.; Porosnicu, C.; Lungu, C.; Soni, K.; Antunes, R.; et al. RF discharge mirror cleaning for ITER optical diagnostics using 60 MHz very high frequency. *Fusion Eng. Des.* **2021**, *163*, 112140. [[CrossRef](#)]
16. Sobolewski, M.A.; Goyette, A.; Wang, Y. Measurements and modeling of ion energy distributions in high-density, radio-frequency biased CF₄ discharges. *J. Appl. Phys.* **2002**, *91*, 6303. [[CrossRef](#)]
17. Sriraman, S.; Kamp, T.A.; Paterson, A. Extreme Edge Sheath and Wafer Profile Tuning through Edge-Localized Ion Trajectory Control and Plasma Operation. U.S. Patent 10,163,610, 25 December 2018.
18. Yamazawa, Y. Electrode impedance effect in dual-frequency capacitively coupled plasma. *Plasma Sources Sci. Technol.* **2015**, *24*, 034015. [[CrossRef](#)]
19. Hayashi, D.; Nagaseki, K. Substrate Processing Apparatus, Focus Ring Heating Method, and Substrate Processing Method. U.S. Patent 8,941,037, 2015.
20. Dhindsa, R.; Singh, V.; Tokunaga, K. Focus Ring. U.S. Patent 6 039 836, 2000.
21. Sasaki, Y. Zone Temperature Control Structure. U.S. Patent 9,484,232 B2, 2011.
22. Pal, A.; Sallinas, M.J.; Lubomirsky, D.; Yousif, I.; Nguyen, A. Thermal Management of Edge Ring in Semiconductor Processing. U.S. Patent 9,947,559, 2018.
23. Chen, J.J.; Rocha-Alvares, J.C.; Ayoub, M.A. Apparatus and Method for Tuning Electrode Impedance for High Frequency Radio Frequency and Terminating Low Frequency Radio Frequency to Ground. U.S. Patent 10 032 608, 24 July 2018.
24. Marakhtanov, A.; Dindsa, R. Multi-Radio Frequency Impedance Control for Plasma Uniformity Tuning. U.S. Patent 10,593,516 B2, 2020.
25. Marakhtanov, A.; Dhindsa, R.; Huston, E.; Fischer, A. Hybrid RF Capacitively and Inductively Coupled Plasma Source Using Multifrequency RF Powers and Methods of Use Thereof. U.S. Patent 7,837,826, 23 November 2010.
26. Dhindsa, R.; Marakhtanov, A.; Deigadino, G.; Hudson, E.; Yen, B.M.; Bailey III, A.D. Triode Reactor Design with Multiple Radiofrequency Powers. U.S. Patent 8,652,298, 2014.