Article

Low-Power Multiplexer Structures Targeting Efficient QCA Nanotechnology Circuit Designs

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Abstract: Quantum-dot cellular automata (QCA) technology is considered to be a possible alternative for circuit implementation in terms of energy efficiency, integration density and switching frequency. Multiplexer (MUX) can be considered to be a suitable candidate for designing QCA circuits. In this paper, two different structures of energy-efficient 2×1 MUX designs are proposed. These MUXes outperform the best existing design in terms of power consumption with approximate reductions of 26% and 35%. Moreover, similar or better performance factors such as area and latency are achieved compared to the available designs. These MUX structures can be used as fundamental energy-efficient building blocks for replacing the majority-based structures in QCA. The scalability property of the proposed MUXes is excellent and can be used for energy-efficient complex QCA circuit designs.

Keywords: low-power QCA circuit; multiplexer; energy dissipation; logic synthesis

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1. Introduction

Designing low-power circuits in nanoscale has been a promising area of research among scientists for a long time. As complementary metal-oxide semiconductor (CMOS) technology reaches its physical limitation [1], several nanotechnologies have been considered to be possible alternatives for CMOS to implement binary and multiple-valued logic circuits [2–6]. One of these nanotechnologies that is expected to provide the implementation of low-power, high-density, and high-speed integrated digital circuits is quantum-dot cellular automata (QCA) [7–12]. In the literature, many studies have been conducted on developing different QCA designs for various fundamental digital circuits such as Multiplexer (MUX) [13–22], XOR/XNOR [23], arithmetic circuits [24–28], memory [18], reversible gate [29], etc. If we investigate the development of QCA architectures, the designers used majority logic gates as a fundamental building block for the design of digital circuits. Recently, several studies have been conducted on developing other QCA structures as alternatives for the majority logic gate for specific functions such as MUX, XOR, XNOR, Reversible gates, Flip Flops, etc.

The Shannon Expansion Theorem is a powerful tool for expanding any Boolean function [30]. MUX is one of the basic building blocks that uses this theorem hierarchically for designing large-scale integrated circuits. There are different QCA MUX designs have been developed based on different priorities. The different aspects that need consideration while developing any QCA circuit are the functional level which corresponds to the netlist of the function to be implemented, the physical level considering all the constraints such as area, latency, power, etc., and geometric level which deals with the layout of the design [31]. The priority of available techniques in the literature targeting better QCA designs of MUX circuits, are more focused on area and latency. Even though area and latency are important factors, power consumption should play a vital role in overall performance of the designed circuits. In this paper, QCA MUX designs targeting better energy dissipation are proposed.

Different QCA MUX designs are available in the literature based on their functional level or physical level implementation. Most of these designs were developed considering functional level where the majority logic structure is used as the fundamental building block [14–16,20,21]. An additional available QCA structure which is a modified majority gate reported in [32] was also used to develop a MUX [19]. Other designs were developed as special structures without considering the existing majority gate as a basic building block [13,17,18]. The current majority logic-based architectures limit the synthesis tools to constraint to a two-way design in which the first part is purely on functional level and then do a conversion of this functional level into a majority-based design. In this paper, the MUX structure is developed by considering the physical level aspects of energy dissipation as the first priority. Here, we use the relative positioning of the cells in the QCA architecture for the MUX implementation. This design can be used as a fundamental building block and as a possible replacement for the basic structures of QCA for energy-efficient circuit designs. In addition, other physical level aspects such as latency and area, and the geometrical aspects such as the placement of the input/output cells can be optimized for overall circuits using the proposed MUXes and their different positions. Moreover, the availability of such QCA structures will expand the fundamental library available to the QCA designs and will allow the designers to develop low-power large-scale circuits.

2. Methodology

2.1. Proposed QCA Structures of a 2×1 MUX

MUX is one of the fundamental functions used for implementing logic circuits. The $2^n \times 1$ MUX consists of 2^n inputs, n selector inputs, and 1 output. A 2×1 MUX performs the function given in Equation (1).

$$F = \bar{S}I_0 + SI_1 \quad (1)$$

In this paper, two different energy-efficient 2×1 MUX designs are proposed. These low-power designs are characterized by the relative positioning of the cells in the architecture. The first QCA structure of the proposed MUX is shown in Figure 1a. This is a square-like structure with three inputs (S , I_1 , I_0), one constant, and one output (F). The constant is always set at logic 0, i.e., with a charge of -1.00 . The input (I_1) which is near the selector input (S) is the most significant bit in this 2×1 MUX. The input diagonally opposite to the selector is the least significant bit, which is I_0 in this case. An alternate design is also possible by changing the constant to logic 1. In this case, the inputs I_0 and I_1 will interchange their positions as shown in Figure 1b. Throughout this paper, the designs of the proposed 2×1 MUX with constant logic 0 and logic 1 are known as MUX1 and MUX2, respectively. The availability of MUX1 and MUX2 will give the options of selecting the best structure for designing different efficient-energy circuits.

Figure 1. Two different QCA structures of 2×1 MUX: (a) Design with constant -1.00 (MUX1); (b) Design with constant $+1.00$ (MUX2).

2.2. Basic Two-Input Functions Using the Proposed MUXes

By selecting different values of I_0 and I_1 , different two-input logic functions such as AND, OR, NAND, NOR, X-OR, and X-NOR can be implemented using 2×1 MUX without using any additional logic gates other than the inverter. The proposed 2×1 MUX designs are used to implement these basic logic operations as shown in Table 1. The selector is always used as one of the input (A), and the second input (B) is used directly or as a complement to the input lines of the MUX based on the function. The AND, NAND and X-OR operations are designed using MUX1. On the other hand, the OR, NOR and X-NOR are designed using MUX2. The selection between MUX1 and MUX2 are done based on energy dissipation. The better energy dissipation is achieved when the inputs are close to each other (S, I_1 for MUX1, and S, I_0 for MUX2). The energy dissipation of these designs is provided in Section 3. Since all the basic two-input logic functions can be implemented with MUX, it can be added to the QCA library of fundamental logic units along with the majority gate and inverter.

Table 1. Implementation of basic 2-input logic functions using MUX.

Function	Simplifications	QCA Implementation
AND ($F = AB$)	$I_0 = 0, I_1 = B, S = A$
OR ($F = A + B$)	$I_0 = B, I_1 = 1, S = A$
NAND ($F = \overline{AB}$)	$I_0 = 1, I_1 = \overline{B}, S = A$
NOR ($F = \overline{A + B}$)	$I_0 = \overline{B}, I_1 = 0, S = A$
X-OR ($F = A \oplus B$)	$I_0 = B, I_1 = \overline{B}, S = A$
X-NOR ($F = \overline{A \oplus B}$)	$I_0 = \overline{B}, I_1 = B, S = A$

2.3. Modularity Property

When dealing with the synthesis tools to minimize the logic circuits, one of the major factors is the modularity of the basic building block. The geometrical arrangement such

as fundamental blocks placement, I/O locations, routing, etc. of the QCA structures also play an important role in the QCA logic synthesis. One of the advantages of the proposed MUX designs is the availability of 16 different positions which can perform the same way. A total of 8 such positions for the MUX1 are shown in Figure 2. In the same way, other 8 positions are possible with MUX2. By considering all these 16 positions and selecting the suitable combinations of these positions, the QCA circuits can be optimized in terms of energy dissipation and other performance factors such as area and latency.

Figure 2. Different possible positions for MUX1.

There are many well-known techniques such as binary decision diagram (BDD) for implementing any logic functions using MUXes. For instance, we can design a 4×1 MUX using three 2×1 MUXes. In addition, an 8×1 MUX using three 4×1 MUXes, etc. In addition, there are further simplification techniques available to reduce the number of MUXes in the design [33]. A 4×1 MUX has four input lines, two selector lines, and one output. An abstract diagram of a 4×1 MUX design using three 2×1 MUXes and the QCA implementation are shown in Figure 3a,b, respectively.

Figure 3. 4×1 MUX using 2×1 MUXes: (a) Abstract diagram; (b) QCA Implementation.

It can be seen that the design is developed using MUX2 in the first level, and MUX1 in the second level. These positions are selected in a way that it will result in optimum energy dissipation. Here, the inputs to the first level MUXes are at clock zone 0, and the squares are in clock zone 1. The outputs of the first level MUXes are in clock zone 2 and are fed as

the inputs to the second level MUX. The square for this MUX is in clock zone 3 and the final output is considered to be in clock zone 0. This clocking scheme is selected to obtain better energy dissipation for the overall design. The selector (S_0) for the first level MUXes is common, and it is the least significant bit in the selection lines. When $S_0 = 0$, 1st MUX (upper right) will pass I_0 and 2nd MUX (upper left) will pass I_2 . Similarly, when $S_0 = 1$, 1st MUX will pass I_1 and 2nd MUX will pass I_3 . The 3rd MUX in the second level passes the output of the 1st MUX when $S_1 = 0$ and the output of 2nd MUX when $S_1 = 1$.

2.4. Further Designs Using MUX

The use of both MUX and majority logic gate can lead to optimized QCA circuits. An abstract diagram of a full adder circuit using the MUX and majority logic gate is shown in Figure 4a. The majority logic gate is used to design the carry output (C_{out}) and the MUX to design the sum output (Sum) in the circuit. The QCA implementation of the full adder circuit is shown in Figure 4b. The position 7 is used here for both MUXes. This design has 4 clock zones and uses an area of $0.05 \mu\text{m}^2$.

Figure 4. Full adder using MUX and Majority logic gates: (a) Abstract diagram; (b) QCA Implementation.

One of the major factors which decide the total energy dissipation of any circuit is the energy dissipation of the fundamental logic structure used in that circuit [31]. From a QCA energy dissipation point of view, the implementation of the fundamental logic operations using proposed MUXes is more efficient compared to the majority-based equivalent designs. Additionally, the number of circuits that can be implemented using a single majority logic gate is limited. However, using the 2×1 MUX and without adding additional logic gates, any two-input logic functions can be implemented with lower energy dissipation. For example, a two-input X-OR function require three majority logic gates, while the same function can be designed with only one 2×1 MUX.

Even though the proposed MUX-based designs are energy efficient compared to majority-based designs for the fundamental logic operations, special QCA structures such as majority, X-OR, etc. perform better for these particular logic operations. When building logic synthesis tools, the proposed MUXes will be a great addition to the library of basic structures for building energy-efficient QCA circuits.

3. Simulation Results and Comparison

This section discusses the energy dissipation of the proposed MUXes and the comparison with the other existing designs. The simulations for the proposed designs are done in QCA DesignerE [31] with the coherence vector engine. The energy dissipation is calculated using simulation engine coherence vector (w/ Energy). Other settings used to do the simulations and calculations of energy dissipation are shown in Table 2.

Table 2. QCA DesignerE settings for simulations.

Parameter	Standard Value
Size of a quantum dot	5 nm
Dimensions of each cell	18 nm × 18 nm
Distance between two cells	20 nm
Layer Separation	11.5 nm
Operating temperature	1 K
Relaxation time	1×10^{-15} s
Clock Period	4×10^{-12} s
Input Period	4×10^{-12} s
Time Step	1×10^{-16} s
Total simulation time	50×10^{-12} , 50×10^{-11} * s
Max. saturation energy of clock signal	9.8×10^{-22} J
Min. saturation energy of clock signal	3.8×10^{-23} J
Clock Shift	0
Clock Slope	1×10^{-12} s
Shape of clock signal slopes	GAUSSIAN
Radius of Effect	80 nm
Relative permittivity of material for QCA system	12.9

* Used for 4×1 MUXes to obtain the power dissipation of all input combinations.

3.1. 2×1 MUX Designs

The simulation results for the proposed 2×1 MUX1 and MUX2 are shown in Figure 5a,b, respectively. One of the major advantages of the proposed structure is the lower energy dissipation of the circuit.

Figure 5. Simulation results of the proposed 2×1 MUXes: (a) MUX1; (b) MUX2.

The comparison of energy dissipation of the proposed MUX designs with other existing MUX designs are shown in Table 3. The average energy is calculated by taking the average of the result of all the different input combinations.

Table 3. Comparison of proposed 2×1 MUX with existing designs.

Circuit Design	Energy Dissipation (meV) with Respect to the Following Input Assignments ($I_0 I_1 S$)								Average Energy Dissipation (meV)	Area (μm^2)	Clock Zones
	000	001	010	011	100	101	110	111			
Proposed MUX1 (2 zones)	0.328	0.175	0.307	0.649	0.409	1.278	0.328	0.889	0.545	0.01	2
Proposed MUX1 (1 zone)	0.347	0.193	0.327	0.783	0.542	1.326	0.443	1.003	0.621	0.01	1
Proposed MUX2 (2 zones)	0.492	0.407	0.356	0.180	1.278	0.479	0.176	0.465	0.479	0.01	2
Proposed MUX2 (1 zone)	0.607	0.522	0.490	0.201	1.327	0.612	0.194	0.483	0.554	0.01	1
[13] (b) *	0.361	0.208	0.340	1.581	0.904	1.102	0.785	1.265	0.818	0.01	2
[13] (c) *	1.076	1.515	1.029	1.488	0.418	2.170	0.907	1.764	1.296	0.01	2
[14]	1.182	1.291	1.273	0.709	0.811	1.305	0.855	0.725	1.019	0.02	2
[20]	0.802	1.487	1.371	0.876	0.697	2.095	1.263	1.484	1.259	0.02	2
[15]	1.045	1.937	0.972	0.900	0.965	1.945	0.890	0.908	1.195	0.02	2
[21]	1.284	1.793	1.815	0.918	0.724	2.331	1.275	1.449	1.449	0.02	3
[16]	0.363	1.334	0.361	0.734	0.796	1.343	0.792	0.752	0.809	0.01	2
[17]	0.743	0.845	0.508	0.638	0.719	0.876	0.688	0.878	0.737	0.01	1
[18]	1.049	0.778	1.043	1.054	0.784	0.783	0.780	1.064	0.917	0.01	2
[19]	0.762	1.550	0.274	0.405	1.417	1.544	1.427	0.896	1.034	0.01	2
[31]	2.477	1.285	2.282	2.476	1.911	2.233	1.713	2.208	2.073	0.09	5
[22]	1.782	1.687	1.718	0.910	0.848	1.701	0.743	0.926	1.290	0.01	2

* The circuits are designed with 2 clock zones to meet the functionality in coherence vector simulation.

From the table, the proposed MUX designs outperform all the other existing MUX designs in terms of power consumption. The proposed MUX1 and MUX2 designs with 2 clock zones have averages energy dissipation of 0.545 meV and 0.479 meV, which provide approximate reductions of 26% and 35% compared to the best existing design [17], respectively. The table also compare area and clock zones used in all these designs. The proposed MUXes with 2 clock zones provide better energy dissipation compared to their 1 clock zone designs. Even with 1 clock zone, the proposed designs give better energy dissipation compared to the best existing design. In addition, it can be noticed that the area and latency of the proposed designs are similar to the best MUX design [17].

3.2. MUX as a Fundamental Building Block for the Basic Two-Input Functions

As we discussed earlier, the MUX designs can be used as a basic building block for developing different fundamental digital logic circuits such as AND, OR, NAND, NOR, and XOR. Currently, QCA technology uses majority logic gate as the fundamental building block for designing these basic operations. Here, these circuits implemented using the proposed MUXes and majority gate are compared. Table 4 is comparing the average energy dissipation of each circuit for all input combinations. The table listed the energy dissipation for each function implemented with both MUX1 and MUX2 designs (with 2 clock zones) and their equivalent majority-based design. It is observed that the AND, NAND, and XOR operations give better energy dissipation while using MUX1 with reductions of 51%, 71%, and 67%, respectively. Additionally, OR and NOR operations give better energy dissipation with MUX2 design with reductions of 66% and 73%, respectively. In all these functions, the MUX-based designs give much better energy dissipation compared to the majority-based designs. For area, AND and OR functions give similar results, NAND and NOR give 50% reductions, and X-OR give 77% reduction. For clock zones, it can be noticed that the proposed MUX-based designs give similar results for all functions except X-OR which gives a reduction of 50%. The total energy dissipation of a circuit depends on the energy dissipation of the fundamental logic gates. Hence, the proposed MUX-based fundamental logic structures can be used to build circuits with better energy dissipation replacing the existing majority-based circuits.

Table 4. Comparison of basic logic functions using the proposed 2×1 MUX with existing majority-based designs.

Function	Circuit-Based Design	Energy Dissipation (meV) with Respect to the Following Input Assignments (AB)				Average Energy Dissipation (meV)	Area (μm^2)	Clock Zones
		00	01	10	11			
AND	Proposed MUX1	0.2784	0.1243	0.2566	0.5860	0.3113	0.01	2
	Proposed MUX2	0.2702	0.9271	0.1922	0.3688	0.4396	0.01	2
	Majority [31]	0.2962	0.9880	0.8646	0.3708	0.6299	0.01	2
OR	Proposed MUX1	0.3663	0.1995	0.8484	0.3836	0.4495	0.01	2
	Proposed MUX2	0.2989	0.1266	0.1252	0.4129	0.2409	0.01	2
	Majority [31]	0.3056	0.9979	0.8762	0.6801	0.7150	0.01	2
NAND	Proposed MUX1	0.2905	0.1723	0.2005	0.1640	0.2068	0.01	3
	Proposed MUX2	0.1735	0.1688	1.1841	0.3552	0.4704	0.01	3
	Majority [31]	0.3891	1.0825	0.9573	0.4559	0.7212	0.02	3
NOR	Proposed MUX1	0.3546	1.1847	0.1678	0.1745	0.4704	0.01	3
	Proposed MUX2	0.1599	0.2023	0.1685	0.2942	0.2062	0.01	3
	Majority [31]	0.3892	1.0783	1.0095	0.5079	0.7462	0.02	3
X-OR	Proposed MUX1	0.5495	0.4482	0.4381	1.4901	0.7315	0.02	3
	Proposed MUX2	0.3851	0.7173	1.4229	0.4929	0.7545	0.02	3
	Majority [31]	1.8431	2.9851	2.6477	1.4990	2.2437	0.09	6

3.3. 4×1 MUX Design

A 4×1 MUX can be designed by cascading the 2×1 MUXes. The simulation result of a 4×1 MUX using the proposed 2×1 MUXes is shown in Figure 6.

Figure 6. Simulation result of proposed 4×1 MUX.

The parameters of a QCA design such as energy dissipation, area, and clock zones were compared with the existing designs in Table 5. The average energy dissipation is calculated by setting the total simulation time to 50×10^{-11} s in the QCA DesignerE. It can be noticed from the comparison that even though there are some designs with fewer clock zones and less area, the proposed design gives better average energy dissipation with a reduction of 19% compared to the best available design [19]. Following the same principle, larger MUXes (8×1 , 16×1 , etc.) can be designed using the proposed MUX structures which will lead to better overall average energy dissipation.

Table 5. Comparison of proposed 4×1 MUX with existing designs.

Circuit Design	Average Energy Dissipation (meV)	Area (μm^2)	Clock Zones
Proposed	1.72	0.04	5
[13]	2.83	0.03	3
[19] (a)	2.13	0.05	5
[19] (b)	2.97	0.08	6
[17]	2.19	0.08	4

As discussed earlier, a 2×1 MUX can perform all the two-input functions without using any additional logic gates. This will give the designer the option to develop any logic circuit with only MUXes. However, by considering the available basic special QCA structures, the circuit can be further optimized in view of functional, physical, and geometrical levels. Such a design for the full adder using the MUX and majority logic gate was discussed in Section 2.4.

From the results discussed in this section, the proposed MUXes outperform all the existing MUX designs. These MUXes can be used as a basic building block for designing large-scale circuits targeting the optimization of energy efficiency. Furthermore, it can be observed that the proposed MUX designs can replace the majority structure in QCA for the fundamental logic operations for energy-efficient designs. Even though the proposed MUXes might not be the efficient structure for all the circuit designs in terms of other parameters which define the cost of the circuit such as area, latency, etc., the addition of these MUXes into the library of the QCA structures will optimize the implementation of circuits.

4. Conclusions

This paper proposes two energy-efficient designs of 2×1 MUX. These designs give better performance in terms of energy dissipation compared to the existing MUX designs. In addition, the proposed MUXes outperform the majority-based structures to design the fundamental logic circuits such as AND, OR, NAND, NOR, and X-OR in terms of energy efficiency. Other QCA circuit parameters such as area and latency are also similar or better compared to the existing designs. Using the proposed MUXes, larger energy-efficient MUX designs are also possible. A 4×1 MUX is designed using three 2×1 MUXes with better energy dissipation compared to the other available designs. In future, circuit developers can add the proposed MUX designs to their logic synthesis tool library which can greatly contribute to developing low-power efficient QCA nanotechnology circuit designs.

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