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A Hybrid Control Scheme with Fast Transient and Low Harmonic for Boost PFC Converter

Sen-Tung Wu [1], Fu-Yuan Chen [2], Min-Chu Chien [2], Jian-Min Wang [3,*] and Yan-Ying Su [3]

[1] Department of Electrical Engineering, National Formosa University, No. 64, Wunhua Rd., Huwei Township, Yunlin County 632, Taiwan; stwu@nfu.edu.tw
[2] Aplustek Integrated Circuits Corp, National Formosa University, No. 372, Minsheng Rd., Taoyuan Dist., Taoyuan City 330, Taiwan; Ryan@atkic.com.tw (F.-Y.C.); darren_chien@atkic.com.tw (M.-C.C.)
[3] Department of Vehicle Engineer, National Formosa University, No. 64, Wunhua Rd., Huwei Township, Yunlin County 632, Taiwan; 10858102@gm.nfu.edu.tw
* Correspondence: jmw@nfu.edu.tw; Tel.: +886-5-631-5692

Abstract: In this study, a new control strategy was proposed to improve transient response and the input current harmonic distortion of power factor correction (PFC) regulators operating in an average current mode. The proposed technique required only two additional gain selectors and a peak detector circuit on the feedforward voltage loop and output voltage feedback loops. It provided a direct reading for the average voltage value of feedback control loops and the peak voltage of feedforward control loops, producing PFC boost regulators with fast dynamic responses and low-input current harmonic distortion. The use of digital potentiometers for directly changing the gain of control loops did not require any divider or squarer to reduce the complexity of control circuits. The operating principles and control strategies of 300 W boost PFC with the new control strategy are presented with detailed analysis and discussion. The experimental results were satisfactory.

Keywords: boost converter; PFC; average current mode

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1. Introduction

Currently, mainstream power supplies on the market are designed and developed using high-frequency switching technologies to achieve compactness and high performance. However, power switching is affected by nonlinear resistance, which leads to harmonic pollution of electrical devices and even increases the loss of transmission lines [1]. Therefore, the International Electrotechnical Commission (IEC) stipulated relevant standards for power harmonics such as the IEC 61000-3-2 standard [2].

In order for the problem of harmonic pollution to be solved, the active power factor correction (PFC) technique is the most suitable method because it increases the input power factor (PF) and reduces input current harmonic distortion [3]. Common current mode control methods include peak current control and average current control methods. Because the peak current control method is likely to be affected by noise [4] and requires slope compensation [5], the average current control method is extensively applied in switching power supply industries. As shown in Figure 1, the average current control method features current and voltage control loops [6,7]. The current control loop controls the phase difference between input current and voltages, whereas the voltage control loop regulates the direct current (DC) output voltage. Both control loops contain twice-line frequency ripples; therefore, the input currents generate second harmonic distortion. The increase in the ripple voltage increases input current harmonic distortion (total harmonic distortion; THDi). Commonly, to reduce the second harmonic effect, the voltage and current loop bandwidth are limited. However, this design drags the system transient response. In applications for light-emitting diode drivers or adapters, fast dynamic responses must be considered because, when load currents change, the output voltage frequently generates oscillation.

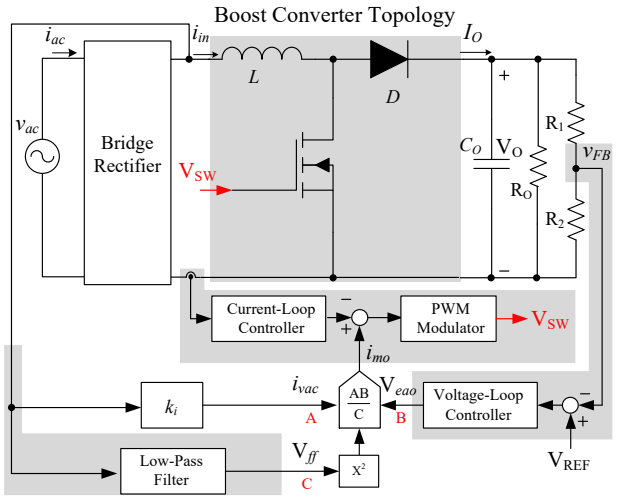

Figure 1. PFC regulators control scheme operating in the average current mode.

To achieve THDi with a fast dynamic response and reduced input current, researchers have proposed many methods [8–14]. Studies [8–10] have adopted a two-stage scheme, with the front-end and back-end schemes serving to reduce THDi and improve transient responses, respectively. In addition, increasing additional circuits in the control loop is an effective improvement method. For example, the studies [11–13] used a sample-and-hold (S/H) circuit to sample output feedback voltage at the zero crossing point of input voltage. Digital control technologies are other common solutions [5,14–17] because digital controllers have the advantages of accurate time control and easily increased system flexibility. For example, the average sliding control technique can be used to determine the relationship between the sliding surface and the input voltage and current and to further reduce input current harmonics [17–20]. The digital signal processors can be used as the control core and combined with the reference commands provided by phase-locked loops to avoid voltage loops from being affected by twice-line frequency. Subsequently, the voltage loop bandwidth can be increased, and PFC transient responses improved [21].

The described methods can prevent voltage loops from being affected by twice-line frequency and increase voltage loop bandwidths, addressing the defects of conventional techniques. However, the complexity of the controllers will increase, and complex algorithms and high-cost microcontrollers are required.

Moreover, one cycle control method is also a novel technique. It does not need a multiplier and the rectifying signal from input voltage; consequently, high power factor can be achieved easier with fewer components. This method will not be influenced by 120 Hz ripple from the rectified input voltage, and this benefit helps PFC to operate in wider range of the bandwidth. However, this technique requires a resettable integrator and a comparator. The switching noise will be a major concern and impact for the comparator [22].

Therefore, in this study, a new control technique was proposed that requires only two additional digital potentiometers, two analog-to-digital converters (ADCs), and a zero-point detection circuit. When the zero-point detection circuit detected input voltage zero points, ADCs are employed to sample input voltage peaks and feedback error signals. The sampling results inform the adjustment of digital circuits to change the system loop gains and complete PFC operations. This prevents the system from being affected by twice-line frequency ripples and subsequently increased the system bandwidths. In this system, the controller requires no dividers or squarer, thereby reducing the overall circuit complexity.

This paper comprises six sections. Section 2 illustrates the operating principles. Section 3 explains the control circuit design. Section 4 describes the stability analysis and compensator design. Section 5 provides the experimental results, which were verified for the 300 W boost power PFC prototype. Section 6 provides the conclusions of this study.

2. Description of the Proposed Scheme

Figure 1 shows the control circuit block diagram conventionally operating in the average current mode. In the circuit scheme, the boost converter is adopted. In terms of the simplification of the analysis, all components are assumed to be ideal. The current command i_{mo} decides the waveform of the input current i_{in}, which is composed of three main parameters, namely, rectified input current i_{vac}, feedforward voltage v_{FF}, and feedback voltage V_{eao}. In a steady state, the current control command i_{mo} can be expressed as follows:

$$i_{mo}(t) = i_{vac}(t) \times \frac{V_{eao}}{v_{FF}^2} \tag{1}$$

The input voltage is a sinusoidal wave rectified through a bridge full-wave rectifier, and filter capacitors are added at the feedforward loop; therefore, V_{eao} and v_{FF} simultaneously feature DC and low-frequency 120 Hz alternating current (AC) components, as shown in Figure 2 [21]. To avoid PFC-induced input current harmonic distortion, the conventional method uses narrow bandwidth filters to inhibit low-frequency components; however, the PFC transient response speed is limited.

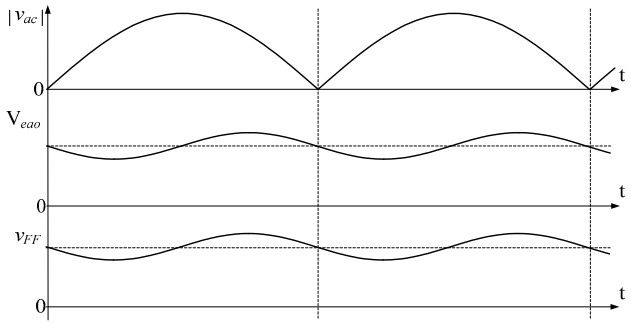

Figure 2. Crucial command waveform.

Figure 2 shows that, when the input voltage v_{ac} is at the peak or zero point, the values for the voltage error signal V_{eao} and the voltage feedforward signal v_{FF} are their respective means. Therefore, the input voltage peak and feedforward means are proportionally related. When the input voltage peak increases, the feedforward signal means increase. Conversely, when the input voltage peak decreases, the feedforward signal means decrease. In summary, the feedforward loops in this study use no filter capacitors; instead, they use peak detectors to read the feedforward signal peak voltage as the feedforward command v_{FF} to improve the input transient responses. For the output feedback, a 120 Hz S/H device is employed to sample the voltage error signal V_{eao}. This method maintains the signal V_{eao} at the mean value between sample intervals.

A new control scheme was proposed, as shown in Figure 3, with two gain control circuits (k_{FF}, k_{FB}), two ADCs, a peak detector, a transconductance amplifier, and an S/H circuit. The core of the controller consists of two adjustable gain modulators, which are separately located at the feedforward loop (dotted blue line) and the voltage feedback loop (dotted red line). On the feedforward loop, the voltage v_{FF} is generated by the input voltage v_{ac} through a bridge rectifier. Peak detectors sample voltage v_{FF} results to adjust the gain k_{FF} size. In addition, to eliminate the effect of output voltage ripples on voltage feedback loops, the error signals V_{eao} for controlling the gain k_{FB} size are determined by the S/H circuit with a 120-Hz sampling frequency and an ADC. Through the aforementioned analysis, the input current reference command i_{mo} can be rewritten as follows:

$$i_{mo}(t) = k_{FF}(k)k_{FB}(k)i_{vac}(t) \tag{2}$$

where $k_{FF}(k)$ and $k_{FB}(k)$ are respectively the kth feedforward gain and feedback gain. The comparison results of (1) and (2) reveal that, when $k_{FF}(k) = 1/v_{FF}^2$ and $k_{FB}(k) = V_{eao}$, the size of the two gains can be adequately adjusted for PFC control.

According to (2), the current control command is determined by the output of the rectified line voltage peak and the voltage error amplifier. Therefore, the command can simultaneously control the converter input impedance, demonstrating resistance and stable output voltage. Subsequently, the roles of the gains $k_{FF}(k)$ and $k_{FB}(k)$ in this study are explained.

The gain $k_{FF}(k)$ provides an open-loop modification that maintains voltage loop gain at a constant value. For example, when the output power remains unchanged (fixed k_{FB}) and the input voltage doubles, the peak detector readjusts the gain controller size as follows:

$$k_{FF}(k+1) = \frac{1}{4}k_{FF}(k) \tag{3}$$

The results reveal that, although the current i_{vac} is doubled, the current command $i_{mo}(t)$ is halved, maintaining input power identical to that in the previous state.

The gain $k_{FB}(k)$ is controlled using the voltage error amplifier. When the output power increases, the output voltage V_{eao} of the voltage error amplifier increases. Through the digital output of the ADC, the gain $k_{FB}(k)$ is increased to change the value of the root mean square of the current command $i_{mo}(t)$ to stabilize the output voltage. By contrast, when the output power decreases, the gain $k_{FB}(k)$ decreases the root mean square value of the current command $i_{mo}(t)$. Notably, on the basis of the twice-line frequency, sampling of the S/H circuit is conducted to obtain a point within a half-wave cycle of the supply mains to ensure that the gain $k_{FB}(k)$ is unaffected by the 120 Hz output ripple voltage.

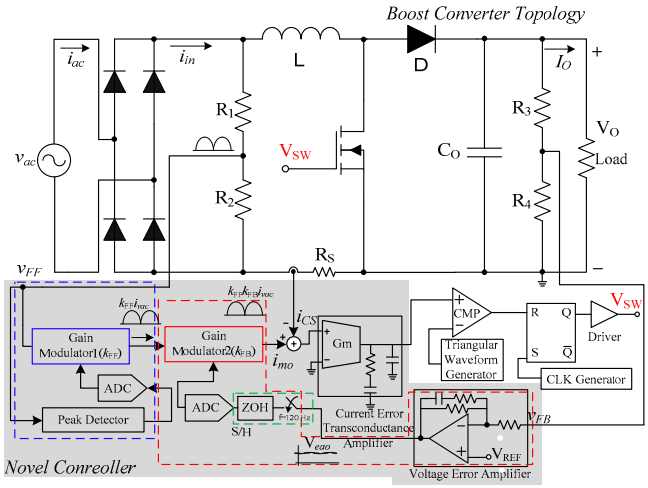

Figure 3. Proposed PFC control circuit block.

3. Control Circuit

3.1. Feedforward Loop Control Circuit

Figure 4a shows the feedforward loop control circuit scheme of the proposed new control strategy, which uses digital potentiometers and an operational amplifier to adjust the k_{FF}. The digital potentiometers play key roles in the circuits because they adjust the command of the gain k_{FF} according to the feedforward voltage v_{FF} peak. General digital potentiometers comprise resistor ladder and wiper. The resistor ladder is composed of equivalent series resistances, and the wiper uses digital signals to control the conduction of analog switches and set series resistance [23].

The square of feedforward voltage v_{FF} is used to determine the gain k_{FF}; therefore, the resistor ladder of the first digital potentiometer is not composed of equivalent series resistance but has an appropriate design. Figure 4b illustrates the process of feedforward

control circuit adjustment for k_{FF} when the input voltage varies. Next, Figure 4a,b illustrates *Case* I, *Case* II, and *Case* III to demonstrate the operating principles of the feedforward loop control circuit. To simplify the analysis of operating principles, all components are assumed to be ideal:

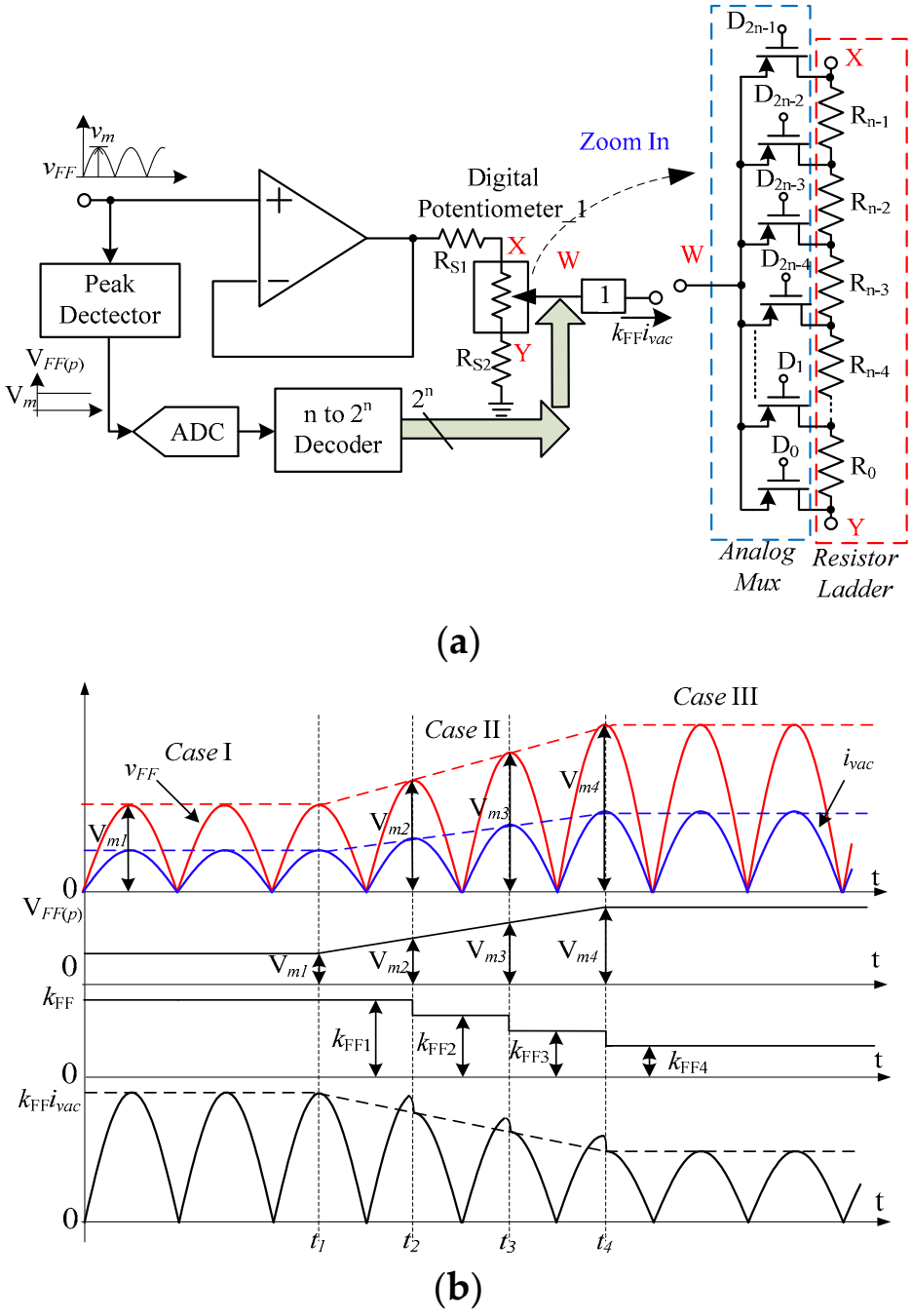

Figure 4. (**a**) The proposed novel feedforward loop control circuit scheme; (**b**) relevant key waveforms.

Case I:

In this interval, the peak detectors begin to sample the voltage peak for v_{FF} as shown in Figure 4b. When the voltage peak V_{m1} is determined, the ADC converts analog signals into a certain proportion of digital signals. The n-bit decoder is then used to generate D(0)

to D(2^n-1) outputs to set the wiper and adjust the resistance value to determine the size of the gain k_{FF}. The gain k_{FF} is calculated using the following equation.

$$k_{FF} = \frac{R_{WY\_1}}{R_{WX\_1}} \tag{4}$$

where R_{WX_1} and R_{WY_1} respectively represent the sums of series resistance between terminals W and X and between terminals W and Y. Equation (4) indicates that the gain k_{FF} contains no 120-Hz ripple component subject to steady-state operation; accordingly, the input current harmonic distortion can be reduced.

Case II:

This interval is the transient region (t_1–t_4) of input voltage variation, as shown in Figure 4b. At t_1, the voltage peak begins to increase from V_{m1} to V_{m4}, and the peak detector output voltage increases accordingly. According to the ADC output value, the decoder then controls the analog switch of the digital potentiometer to move terminal W toward terminal Y, thereby completing the operation of reducing gain k_{FF}. Notably, the ADC samples only at t_2, t_3, and t_4. Therefore, the gain k_{FF} changes once in a cycle (8.33 ms). For example, in the interval $t_1 < t \leq t_2$, the peak detector output voltage increases with time, but the gain k_{FF} only changes from k_{FF1} to k_{FF2}.

Case III:

At t_4, the output voltage again reaches a steady state, and the input voltage peak remains identical. The digital potentiometer maintains the feedforward gain k_{FF4} according to the ADC digital data, as shown in Figure 4b. Although the input voltage varies with time, the proposed control strategy enables the feedforward loop gain to be maintained at a fixed value, simplifying the design of the loop compensator.

The analysis results indicate the role of gain k_{FF} in PFC feedforward loop control. Subsequently, the design for gain k_{FF} is described. The general grid specification is between 90 and 265 V_{rms}. For the facilitation of the PFC operation in the specification, the gain k_{FF} is designed accordingly. First, the resolution of the digital potentiometer is considered. Higher resolution increases the accuracy of signals. However, each piece of data requires increasing numbers of bits, and the ADC price increases.

In this study, the ADC is only required to sample the input peak voltage; thus, the resolution has the minimum bit requirement, which can be expressed using the following equation:

$$n \geq \frac{\log\left(\frac{v_{ac(peak\_max)} - v_{ac(peak\_min)}}{\text{Minimum resolution of voltage}}\right)}{\log(2)} \tag{5}$$

where $v_{ac(peak\_max)}$ and $v_{ac(peak\_min)}$ respectively represent the maximum input voltage peak and minimum voltage peak. For the proposed specification, the maximum input voltage peak was 375 V, and the minimum resolution unit was 4 V. Equation (5) can be used to determine the resolution bit for $n \geq 5.90$. A 6-bit resolution ADC and a digital potentiometer with 6-bit resolution are adopted to satisfy the varying input voltage peaks corresponding to various gain k_{FF} sizes.

Equation (2) indicates that, in fixed output power conditions, the current command can be determined through $k_{FF}i_{vac}$. Figure 5 shows the proposed feedforward loop circuit scheme, which uses a 6-to-64 line decoder to decode input voltage peak results and control the conduction position of analog switches, thereby changing the current command size. Table 1 shows the truth table of the 6-to-64 line decoder corresponding to input peak voltage. When the input peak voltage $V_{FF(p)} = V_{mB}$ is decoded as $((B)_{10} = (A_5A_4A_3A_2A_1A_0)_2)$,

$D_{(B)}$ = 1 is output to drive conduction of the analog switch. The current command $k_{FF}i_{vac}$ can be expressed as follows:

$$k_{FF}i_{vac} = v_{FF}\left(\frac{R_{S2} + \sum_{n=1}^{B} R_{n-1}}{R_{S1} + \sum_{n=0}^{62} R_n + R_{S2}}\right) \tag{6}$$

where B is a constant ranging from 1 to 63.

In particular, when B = 0, the current command can be expressed as follows:

$$k_{FF}i_{vac} = v_{FF}\left(\frac{R_{S2}}{R_{S1} + \sum_{n=0}^{62} R_n + R_{S2}}\right) \tag{7}$$

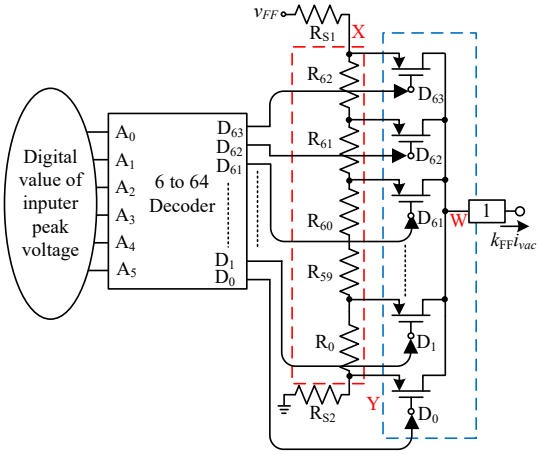

Figure 5. The proposed feedforward loop circuit scheme.

Table 1. TO-64 line decoder corresponding to input peak voltage.

$V_{FF(p)}$	Inputs						Outputs					
	A_5	A_4	A_3	A_2	A_1	A_0	D_{63}	D_{62}	D_{61}	...	D_1	D_0
V_{m64}	0	0	0	0	0	0	0	0	0	...	0	1
V_{m63}	0	0	0	0	0	1	0	0	0	...	1	0
.	.	.	.	.	.	.	.	.	.	.	.	.
.	.	.	.	.	.	.	.	.	.	.	.	.
.	.	.	.	.	.	.	.	.	.	.	.	.
V_{m3}	1	1	1	1	0	1	0	0	1	...	0	0
V_{m2}	1	1	1	1	1	0	0	1	0	...	0	0
V_{m1}	1	1	1	1	1	1	1	0	0	...	0	0

3.2. Voltage Feedback Loop Control Circuit

The main function of the voltage feedback loop is to regulate PFC and maintain a stable output voltage. In the conventional design method, the rectified input voltage is multiplied by the voltage error signal V_{eao} and the product divided by squared feedforward voltage v_{FF}. Subsequently, a current control command i_{mo} is generated to regulate the input current size and achieve stable output voltage control. As such, the voltage V_{eao} and current control command i_{mo} are in direct proportional relationship. Moreover, the bandwidth of voltage loops must be set far lower than that of the input line voltage because excessively wide bandwidth may cause severe input current harmonic distortion [24]. Therefore, the conventional method cannot simultaneously improve the voltage transient response and input current harmonic distortion.

To improve the shortcoming of the conventional PFC control strategy caused by the voltage loop, we adopted a digital potentiometer, an ADC, and an S/H circuit in the voltage loop, as shown in Figure 6a. When the input load varies, the voltage feedback control circuit adjusts k_{FB} through the process in Figure 6b. To simplify the analysis of operating principles, we assumed all components to be ideal.

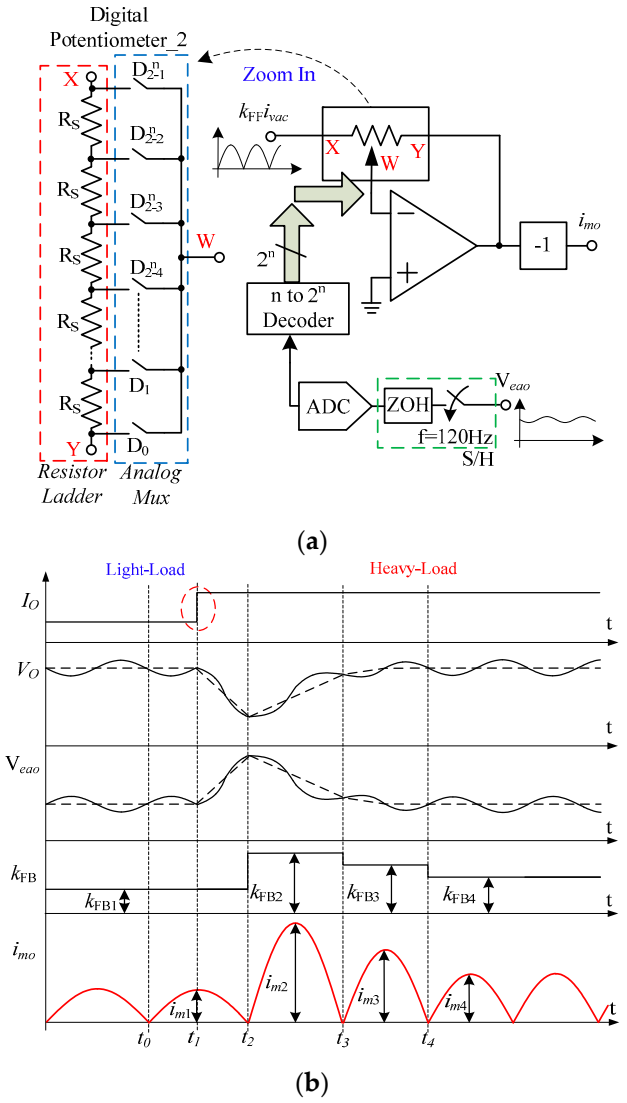

Figure 6. (**a**) The proposed new control strategy–based voltage feedback loop control circuit scheme; (**b**) relevant critical waveforms.

State 1 (t_0–t_1):

Before t_1, PFC is performed at a steady state. The second digital potentiometer adjusts the wiper W to a suitable position according to the V_{eao} decoded using the ADC, as shown in Figure 6b. Because the ADC sampling time is determined by the twice-line frequency, PFC can avoid from the effect of voltage V_{eao} ripples.

According to Figure 6a, the resistor ladder structure of the second digital potentiometer is different from that of the first. It is composed of equivalent series resistance R_S, where a total of 2^n series resistances is observed between terminal X and terminal Y. The wiper of the second potentiometer has identical functions to that of the first, namely, to set any of the $2^n - 1$ resistances through conduction of the analog switch.

Because the terminals X and Y of the digital potentiometer are respectively connected to the feedforward loop control command signal $k_{\mathrm{FF}} i_{vac}$ and the operational amplifier output end, the circuit output is expressed as follows:

$$i_{mo}(t) = k_{\mathrm{FF}} k_{\mathrm{FB}} i_{vac}(t) \tag{8}$$

where

$$k_{\mathrm{FB}} = \frac{\mathrm{R_{WY\_2}(D)}}{\mathrm{R_{WX\_2}(D)}}$$

$$\mathrm{R_{WX\_2}(D)} = \frac{\mathrm{D}}{2^n - 1}\mathrm{R_{XY}}$$

$$\mathrm{R_{WY\_2}(D)} = \frac{(2^n - 1) - \mathrm{D}}{2^n - 1}\mathrm{R_{XY}}$$

Equation (8) indicates that the adjustment of gain k_{FB} can facilitate a proportional relationship between voltage V_{eao} and current control command i_{mo} without any 120 Hz ripple component in k_{FB}.

State 2 (t1~t4):

When the PFC output load is instantaneously switched from a light load (10%) to a heavy load (100%), the potential of the output voltage decreases suddenly, as shown in the dotted red line in Figure 6b. The error amplifier then compares the feedback voltage v_{FB} and reference voltage V_{REF} to obtain the required error signal V_{eao}. Through the error signal, the wiper of the potentiometer is adjusted to increase k_{FB}, thereby facilitating the rapid restoration of PFC output voltage from a lower value to the normal voltage range. Consequently, the goal of stable output voltage is achieved, as shown in Figure 6a.

In this state, although ADC sampling is conducted only at $\mathrm{t_2}$, $\mathrm{t_3}$, and $\mathrm{t_4}$, the voltage loop bandwidth—without the effect of the output voltage ripple—can be set at a larger value compared with for the conventional method.

In addition, the output power specification must be considered in the resolution of the second digital potentiometer. Theoretically, higher ADC resolutions entail more accurate sampling results for the output power. However, due to cost limits, this study used 2% output power as the minimum resolution unit. The minimum resolution bit can be determined using (9):

$$n \geq \frac{log(\frac{P_{o(max)}}{P_{o(max)\times 0.02}})}{log(2)} \tag{9}$$

where $P_{\mathrm{O}(max)}$ is the maximum output power. This study set a specification of 300 W for the maximum output power. Equation (9) indicates that the ADC resolution and the resolution of the second digital potentiometer must be 6 bits. The ADCs with 50-kHz sampling frequencies are currently common on the market. This sampling frequency is enough to increase voltage loop bandwidth. Thus, this study adopted the ADC with said sampling frequency.

Table 2 provides a comparison between the predictive CCM average current control technique and the proposed technique. It is worth noticing that the predictive CCM average current control technique performs better, but it requires a DSP to achieve the algorithm. This is much more complex, and the cost of circuit is higher. In this paper, the proposed control technique can be integrated as an IC by using the ADC and the digital potential meter structure. The cost is much lower than the control technique with DSP controller.

Table 2. Comparison of predictive ccm average current control technology and proposed ccm average current control technology for boost pfc converter.

	Computational Complexity	Difficulty of IC Integration	PI Controller Design Requirements	Cost
Predictive CCM average current controller [25,26]	Medium	Large	No	High
Proposed CCM average current controller	Small	Small	Yes	Low

4. Design Criteria

Two adjustable gain modulators are used to resolve the defects of poor conventional PFC transient response. Therefore, the settings of the two digital variable resistances are critical. The selection of a compensator, digital potentiometer resolution, and gain range require consideration as well as the inductors, power switch, and diode voltage and current-withstand capacities. For the proposed PFC, we applied the following circuit parameter settings.

- Input AC voltage: v_{ac} = 110 V_{rms}~220 V_{rms};
- Output DC voltage: V_O = 385 V_{DC};
- Output maximum power: $P_{O(max)}$ = 300 W;
- Switching frequency: f_S = 70 k_{HZ}.

4.1. Digital Potentiometer

In (6), the current command $k_{FF}i_{vac}$ and feedforward voltage v_{FF} are crucial parameters for determining the series resistance of the first digital potentiometer. If maximum output power is set as a condition, when the input voltage reaches the maximum peak, the feedforward voltage v_{FF} maximum peak is $V_{m(max)}$. Table 1 indicates that, D_0 = 1 for the decoder when the voltage peak is at its maximum. The minimum peak of the current command $k_{FF}i_{vac}$ can be predicted because its peak value depends on the input current. The relationship for resistance R_{S2} can be expressed as follows:

$$R_{S2} = \left(\frac{k_{FF} i_{vac(min)}}{V_{m(max)} - k_{FF} i_{vac(min)}} \right) \left(R_{S1} + \sum_{n=0}^{62} R_n \right) \tag{10}$$

By contrast, when the feedforward voltage v_{FF} is at the minimum peak $V_{m(min)}$, the decoder D_{63} = 1. The relationship for resistance R_{S1} is expressed as follows:

$$R_{S1} = \left(\frac{V_{m(min)} - k_{FF} i_{vac(max)}}{k_{FF} i_{vac(max)}} \right) \left(R_{S2} + \sum_{n=0}^{62} R_n \right) \tag{11}$$

Reorganization of (10) and (11) yields the following relationship between the resistances R_{S2} and R_{S1}:

$$R_{S1} = \left(\frac{V_{m(max)}}{k_{FF} i_{vac(min)}} - \frac{V_{m(max)} k_{FF} i_{vac(max)}}{V_{m(min)} k_{FF} i_{vac(min)}} \right) R_{S2} \tag{12}$$

Per the aforementioned specification, the maximum peak range of the input current is between 1.60 and 4.88 A. Therefore, the current command $k_{FF}i_{vac(min)}$ = 1.60 A and $k_{FF}i_{vac(max)}$ = 4.88 A. $V_{m(max)}$ = 15 V and $V_{m(min)}$ = 4.92 V. Equation (11) yields the resistance R_{S2} = 10 k Ω and R_{S1} = 827 Ω. In summary, the resistance of the first digital potentiometer can be determined; $\sum_{n=0}^{62} R_n$ = 82.923 kΩ.

When the input voltage v_{ac} peak decreases to 371 V, the feedforward voltage peak is $v_{FF(peak)}$ = 14.84 V, and D_1 = 1 for the decoder. The current command peak $k_{FF}i_{vac1} = 1.617$ A, and the resistance R_0 is expressed as follows:

$$R_0 = \left(\frac{k_{FF}i_{vac1}}{v_{FF(peak)}}\right)\left(R_{S1} + \sum_{n=0}^{62} R_n + R_{S2}\right) - R_{S2} = 214\ \Omega \quad (13)$$

Following this inference, we find that different input voltage peaks correspond to different resistance values, which can be plotted as shown in Figure 7. Figure 7 shows that the resistances R_0 to R_{62} are nonlinear. Therefore, the first digital potentiometer cannot use the equivalent series resistance scheme.

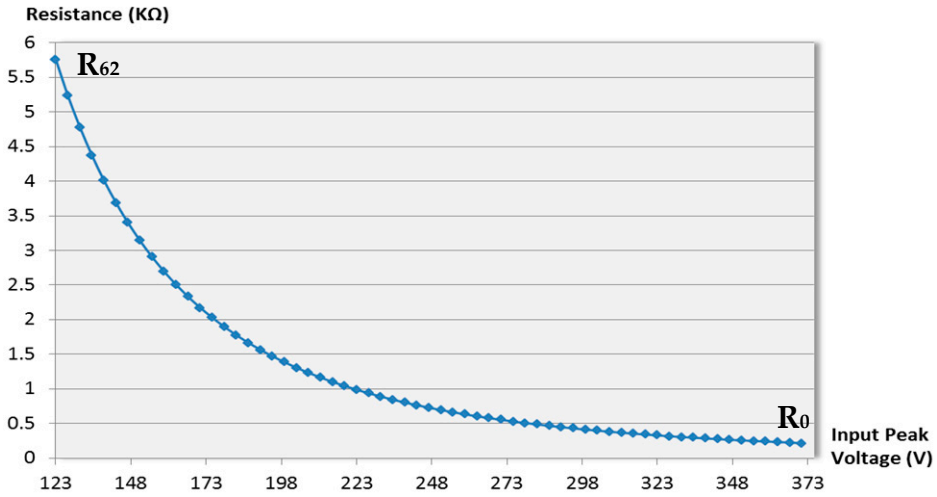

Figure 7. Resistance corresponding to various input voltage peaks.

The second digital potentiometer has the main function of stabilizing the output voltage. Changes in the output power of a converter generally cause output voltage errors. To enable precise adjustment of the output power, this study adopted 6-bit digital potentiometers (10 kΩ).

4.2. Inductor

For the setting of inductors, when switching frequency is 100 kHz, the duty cycle of the converter at a low voltage input is represented as $D = (V_O - V_{in})/V_O = 0.59$. The inductor current ripple peak-to-peak value is set as 20% of the maximum line current peak. Thus, the inductance relationship is expressed as follows [17]:

$$L = \left(\frac{V_{peak(min)} \times D}{f_S \times \Delta I}\right) = 367\ \mu H \quad (14)$$

This study set the inductance at 380 μH.

4.3. Capacitor

A crucial consideration in the selection of output capacitors is the hold-up time of the output voltage when the input energy is withdrawn. Hold-up time is typically approximately 10 ms. Although ripple current and output ripple voltage are factors that require consideration, the capacitance set with the two factors is low. Generally, the hold-up time is the main factor for consideration.

$$C_O = \left(\frac{2 \times P_{O(max)} \times \Delta t}{V_O^2 - V_{O(min)}^2} \right) = 183\ \mu F \quad (15)$$

where the hold-up time Δt = 10 ms and the minimum output voltage $V_{O(min)}$ = 340 V.

4.4. Power Switch and Diode

The withstand current of the power switch selected must be higher than the maximum peak current of the inductor. Therefore, the withstand current of the power switch must be at least 5.36 A, and the withstand voltage must be higher than the 400-V output voltage. Diodes must feature the same level rating values as the power switch.

4.5. Design Consideration of the Compensator

Many studies have analyzed boost PFC power transfer functions [24,27]. Relevant literature has revealed that, when boost PFC is operated with resistive load, the control-to-output transfer function of the boost PFC is a one-order system. Hence, the compensator adopts PI controller for providing the phase margin for 45° to 60° and high cross-over frequency [28]. The bandwidth for the voltage loop of conventional PFC is set for 5 HZ to 10 HZ. In this paper, the proposed method can avoid the influence from the 120 HZ ripple voltage. The maximum bandwidth can be designed for 60 HZ.

5. Experimental Results

The following experimental parameters were used: input voltage 110 V_{rms}, output voltage V_O = 400 V, output power P_O = 40–300 W, switching frequency f = 70 kHz, output inductance L = 382 µH, and output capacitor C_O = 220 µF.

Figure 8a,b respectively represent the grid waveforms for output power P_O = 40 W and P_O = 300 W at an input voltage v_{ac} = 110 V_{rms}. The waveforms suggest that the proposed control strategy generates input line current waveforms that achieve phases almost perfectly consistent with that of the input line voltage waveforms. The results reveal that the boost PFC converter used according to the proposed method increases the system PF.

According to the experimental data, the proposed technique not only prevents effects on the PF but also resolves the ripple components of the twice-line frequency, improving the input line current THDi. These effects are obtained by measuring the input voltage in the following conditions: v_{ac} = 110 V_{rms} (P_O = 40 W) and v_{ac} = 110 V_{rms} (P_O = 300 W). The line current THDi values of both conditions were lower than 5.9%. In particular, the THDi at 300 W was 0.95%, as shown in Figure 9a,b.

The proposed method requires no additional capacitor on the feedforward loop to attenuate second harmonic waves, and the bandwidth settings of the voltage loops are higher than in conventional methods. Therefore, the proposed control strategy realizes greater input transient response than conventional methods do, as shown in Figures 10 and 11. Figure 10a depicts the input transient response measured in the conditions of input current THDi = 4% and output power P_O = 300 W. According to Figure 10a, when the input voltage increased from 110 V_{rms} to 220 V_{rm}, the time for the output voltage to transfer from a transient state to a steady state was approximately 200 ms, and voltage maximum overshoot was approximately 32 V in the conventional method. The proposed method reduced the transient time by approximately 170 ms and voltage maximum overshoot by approximately 24 V, respectively, as depicted in Figure 10b. By contrast, in the same conditions, when the input voltage changed from 220 to 110 V_{rms}, the steady-state time and voltage maximum overshoot respectively exhibited 260-ms and 5-V differences, as shown in Figure 11a,b.

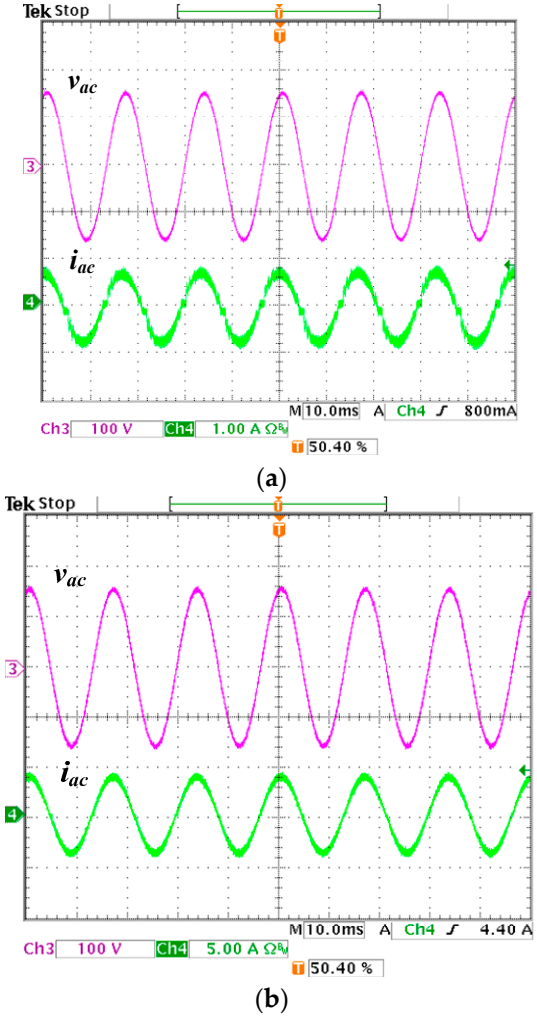

Figure 8. At an input voltage of 110 V_{rms}, the boost PFC input voltage and current waveforms with (**a**) output power of 40 W and (**b**) output power of 300 W (V_{ac}: 100 V/div., i_{ac}: 1 A/div., Time: 10 ms/div.).

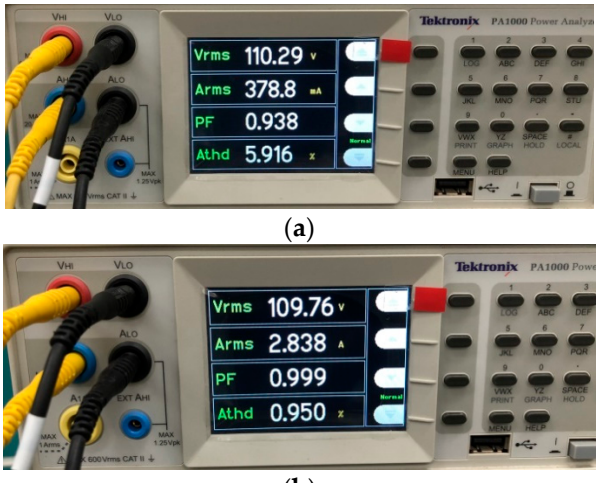

Figure 9. At an input voltage of 110 V_{rms}, the boost PFC input line current THDi with (**a**) output power of 40 W and (**b**) output power of 300 W.

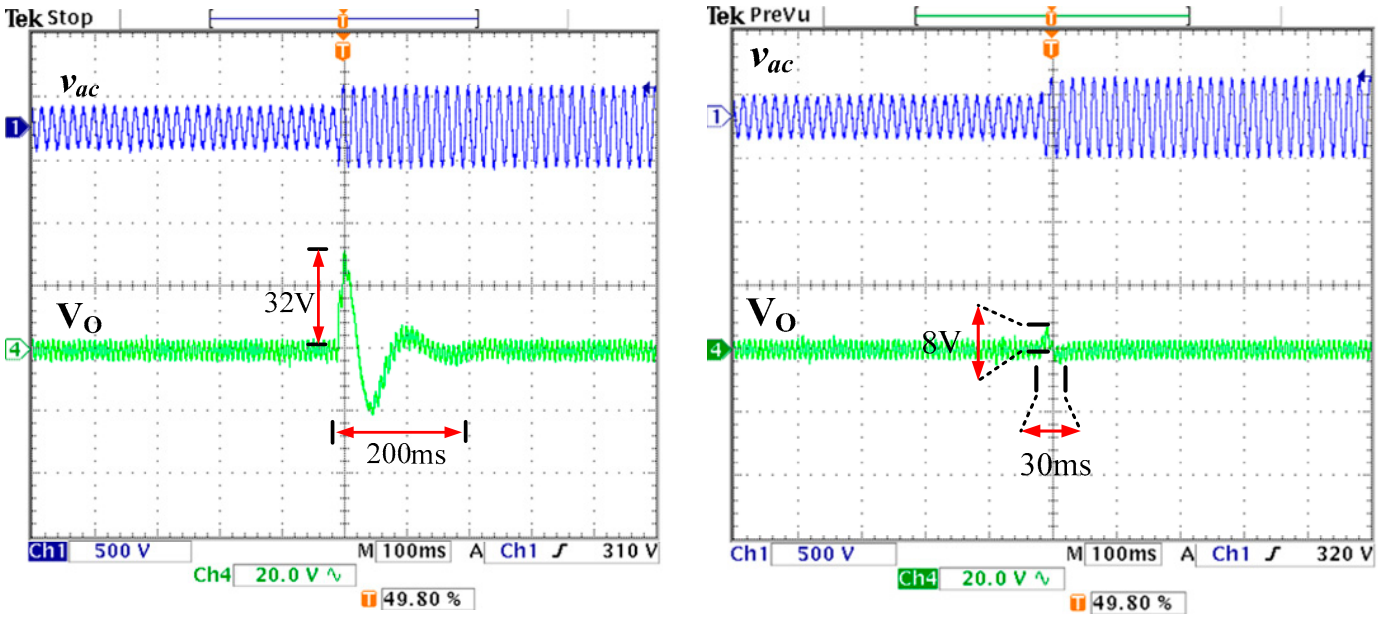

Figure 10. Transient response waveform of an input voltage change from 110 to 220 V_{rms} based on PFC with the use of (**a**) the conventional control strategy and (**b**) the new control strategy (V_{ac}: 500 V/div., v_O: 20 V/div., time: 100 ms/div.).

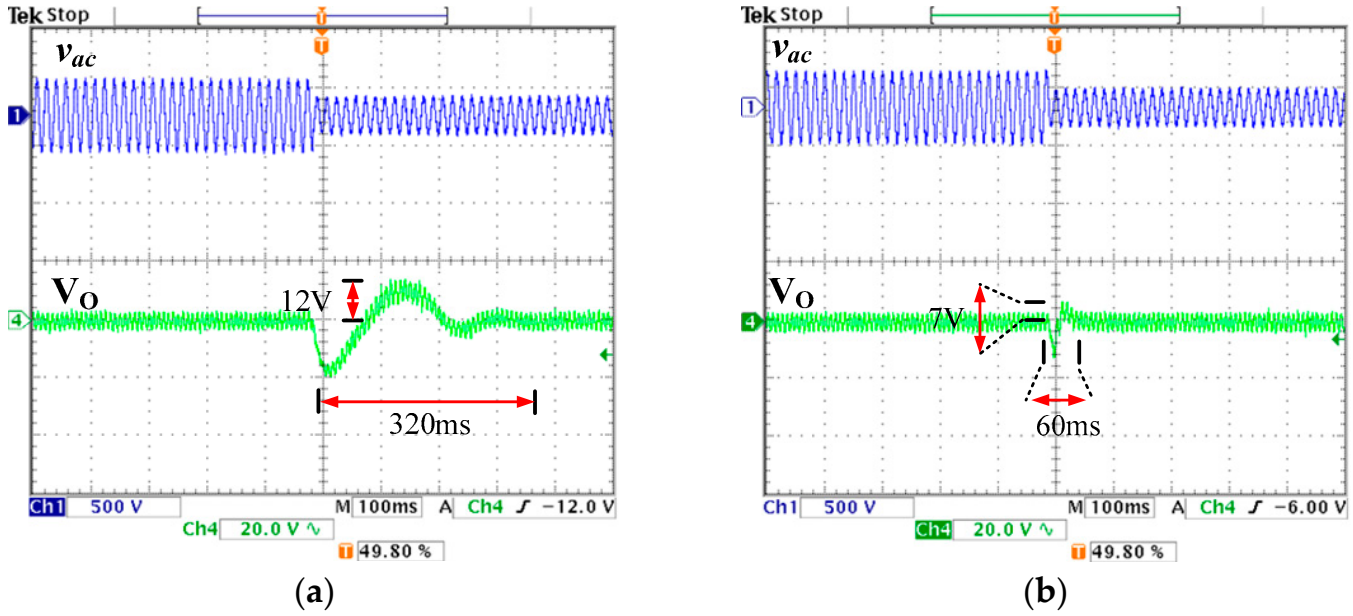

Figure 11. Transient response waveform of an input voltage change from 220 to 110 V_{rms} based on PFC with the use of (**a**) the conventional control strategy and (**b**) the new control strategy (V_{ac}: 500 V/div., v_O: 20 V/div., time: 100 ms/div.).

The output voltage transient responses for PFC with the use of conventional and proposed methods were compared. Figure 12a depicts the conventional PFC output voltage transient response (for output power conditions of light load 40 W and heavy load 300 W); Figure 12b depicts the new control strategy–based PFC output voltage transient response. The experimental data revealed that the conventional PFC output voltage transient response required approximately 400 ms to achieve a steady state, whereas the new PFC required approximately 200 ms. The proposed PFC was superior to the conventional one. The experimental data verified that the proposed method reduced input voltage and load transient response time.

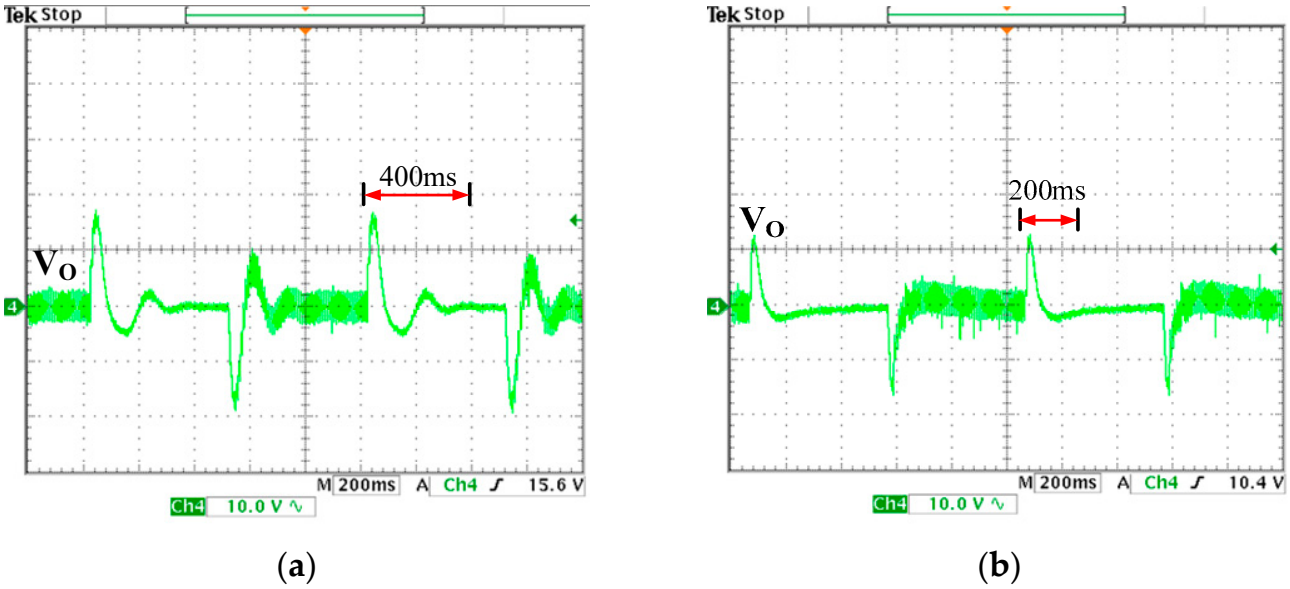

Figure 12. Output transient response waveform based on PFC with the use of (**a**) the conventional control strategy and (**b**) the new control strategy (V_{ac}: 500 V/div., v_O: 10 V/div., time: 200 ms/div).

Table 3 demonstrates the relevant PFC measurement data yielded by the new control technique, including the PF value and input current THDi. The optimal input current THDi was approximately 0.9%. Finally, the testing condition was set for 110 V input voltage and 300 W output power. The standard of IEC 61000-3-2 (Class-D) was applied to compare with the proposed scheme, as shown in Figure 13. From this figure, the current harmonic for odd-harmonic of the proposed structure was much lower than the standard. Hence, the proposed scheme of this paper is feasible.

Table 3. Newly structured pf value and Thdi.

V_{in} (Vrms)	V_O (V)	I_O (A)	PF (%)	THDi (%)
110	385	0.100	0.939	5.91
110	385	0.175	0.977	3.24
110	385	0.260	0.989	1.92
110	385	0.340	0.993	1.37
110	385	0.420	0.996	1.14
110	385	0.500	0.997	1.06
110	385	0.573	0.998	1.01
110	385	0.650	0.999	0.97
110	385	0.723	0.999	0.98

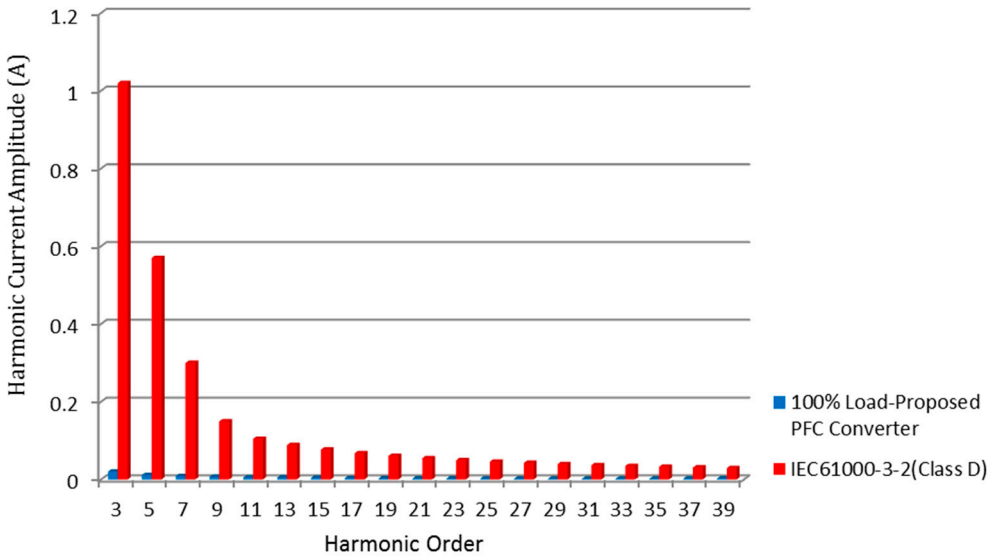

Figure 13. Comparison of current harmonic between the proposed structure and the standard of IEC61000-3-2 (Class-D) under the input voltage 110 V and output power 300 W.

6. Conclusions

The paper proposed a control technique for PFC regulator operated in average current mode. The operation principle of the control technique has been discussed in detailed. A control technique for a 300 W Boost PFC regulator was developed, and it also performed very well. The paper has two advantages from the proposed control techniques. The first is that two sets of ADC and digital potential meter are placed at the feed forward voltage loop and the output voltage loop, respectively. There is no need to place extra multiplier and square circuit for lowering the complexity. The second is that the peak voltage detector and S/H circuit can sample the average value from the feed forward voltage loop and the output voltage loop; hence, there is no influence for 120 H_Z ripple voltage. It helps to reduce the input current harmonic distortion. After that, a low frequency bandwidth filter is unnecessary. This will speed up the transient response from input voltage to the output load.

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