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A New Cost-Efficient Design of a Reversible Gate Based on a Nano-Scale Quantum-Dot Cellular Automata Technology

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Abstract: Quantum-dot cellular automata (QCA) nanotechnology is a practical suggestion for replacing present silicon-based technologies. It provides many benefits, such as low power usage, high velocity, and an extreme density of logic functions on a chip. In contrast, designing circuits with no waste of information (reversible circuits) may further reduce energy losses. The Feynman gate has been recognized as one of the most famous QCA-based gates for this purpose. Since reversible gates are significant, this paper develops a new optimized reversible double Feynman gate that uses efficient arithmetic elements as its key structural blocks. Additionally, we used several modeling principles to make it consistent and more robust against noise. Moreover, we examined the suggested model and compared it to the previous models regarding the complexity, clocking, number of cells, and latency. Furthermore, we applied QCADesigner to monitor the outline and performance of the proposed gate. The results show an acceptable improvement via the designed double Feynman gate in comparison to the existing designs. Finally, the temperature and cost analysis indicated the efficiency of the proposed nan-scale gate.

Keywords: nano-electronic; temperature; cost; quantum-dot cellular automata; double Feynman gate; reversible logic

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1. Introduction

Over the last 20 years, scholars have always used silicon-based procedures to meet the necessary dimension scaling for executing high-velocity, high-density, and low-energy VLSI devices [1]. Nevertheless, an aggressive scaling such as that certainly has numerous challenges, including high power density, high leakage current, and expensive lithography. Scholars have forecasted that the above challenges will lead to the end of the CMOS revolution in the coming years [2–4]. The abovementioned background brings about the necessity of researching new nano-scale technologies to introduce reliable alternatives [5]. Quantum-dot cellular automata (QCA) addresses the related nano-scale issues and provides a novel technique for processing and transforming the information [6–8]. It has ultra-low feature size and power usage [9]. The researchers asserted that it is possible to make nano-scale QCA cells by means of molecular execution, using a self-assembly procedure [10–13].

Nanotechnology has become the core of many recent high-level technologies, and the QCA can be a revolutionary method for nano-processing [14]. Parallel and reversible logic is becoming a noticeable technology that improves QCA technology performance [15]. Scholars have reported several works on reversible logic gates and their execution [16–21].

Numerous reversible logic gates exist [22,23]; they are essential for their reversibility features, and the Feynman gate is a crucial one. This paper proposes a new double Feynman gate circuit using the reversible gate [15]. We have applied a set of reversible logic gates in which each input has a one-to-one relationship with each output [24]. Additionally, the number of the input and output gates is equal. Since reversible circuits can identify and modify the output faults, identifying and modifying faults would be easier than simple designs [16,25]. There is no info loss in a reversible circuit [22]. Then, it provides the highest output information and makes error identification possible. We applied the Feynman gate to generate a new reversible gate in QCA technology in the current study. Briefly, the present article contributes to the following:

- Introducing a coplanar structure for a reversible double Feynman gate with a lower usage space and cell count;
- Comparing the proposed model to existing ones regarding cell counts, delay, layer, cost, and average output polarization.

The article structure is described below. Section 2 summarizes the previous studies. Section 3 proposes a new double Feynman gate in the QCA. Section 4 shows the simulation outcomes of the suggested scheme. Ultimately, the last section concludes the work and gives some suggestions for future work.

2. Related Work

Scholars have presented various designs for the reversible gate and circuit [26]. Here, we summarize and compare the major reversible models and circuits in QCA technology. The reversible gates can be considered as construction parts of the reversible logic. The researchers offered exclusive mapping among the vectors of output and input. Thus, the input count should be similar to the output amount. Figure 1 indicates some block diagrams of the major reversible gates proposed in the past.

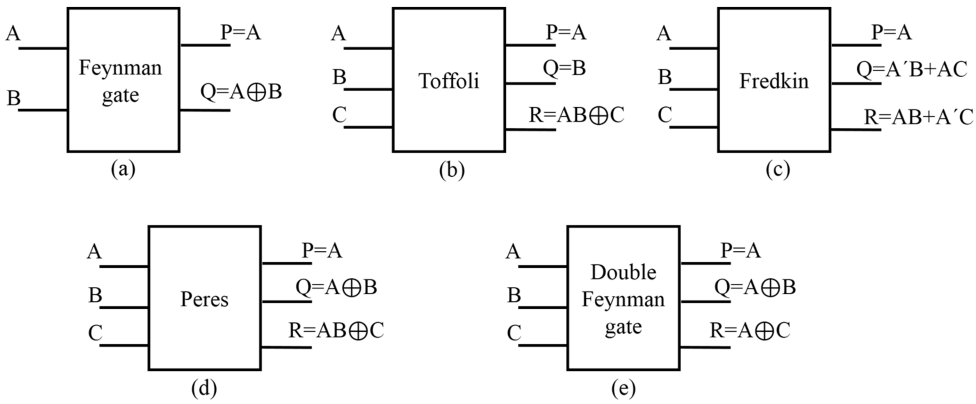

Figure 1. The block diagrams of the reversible gates: (**a**) the Feynman [26], (**b**) the Toffoli [27], (**c**) the Fredkin [28], (**d**) the Peres [29], and (**e**) the double Feynman gate [30].

Figure 1a indicates the Feynman gate's block diagram, and Figure 2 indicates its implementation based on QCA. Figure 3a indicates the block diagram of the double Feynman gate, and Figure 3b indicates its QCA. The output vector is O (R, P, and Q), and the input vector is I (B, C, A). R = A ⊕ C, Q = A ⊕ B, P = A specify the output. The truth table of the gate is illustrated in Table 1.

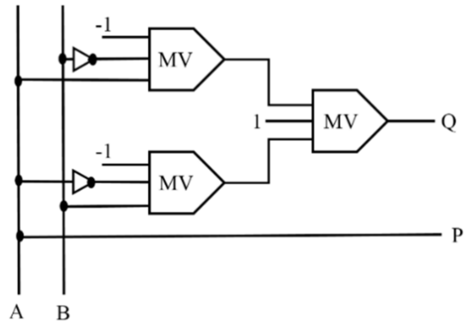

Figure 2. The diagram of the Feynman gate in the QCA [26].

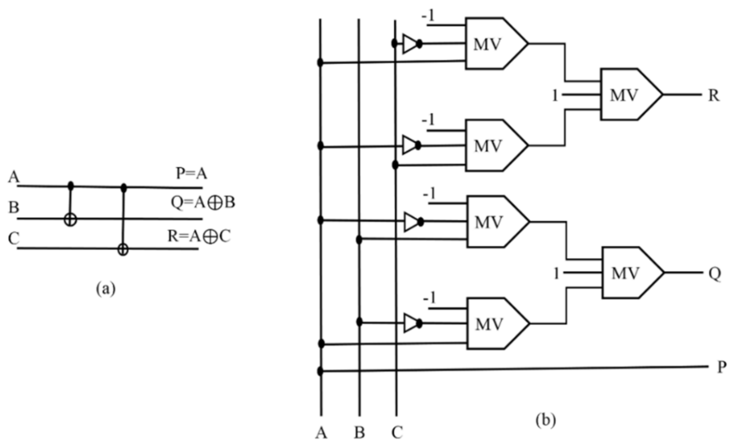

Figure 3. (**a**) The logical diagram of the double Feynman gate, and (**b**) the QCA-based diagram of the double Feynman gate [16].

Table 1. The truth table of the double Feynman gate.

Input			**Output**		
A	**B**	**C**	**P**	**Q**	**R**
0	0	0	0	0	0
0	0	1	0	0	1
0	1	0	0	1	0
0	1	1	0	1	1
1	0	0	1	1	1
1	0	1	1	1	0
1	1	0	1	0	1
1	1	1	1	0	0

Researchers have proposed numerous reversible gates. The NOT and BUFFER are the simplest ones (“1×1”). The Feynman gate is the famous “2×2” reversible gate [26]. It can be applied to have more fan-out. Figure 1a indicates the symbol of the Feynman gate. The Toffoli [27] (Figure 1b), Peres [29] (Figure 1d), and Fredkin [28] (Figure 1c) gates are the famous “3×3” reversible gates. The Toffoli gate works similarly to the Feynman gate; its single variance is that it has two control input lines. The universal gate means that we can synthesize all digital gates using it. The self-compliment gate means that if we use two Toffoli gates serially, the output of the second one would be identical to the input of the first one. Figure 1e indicates the double Feynman gate, plotting inputs (A, B, C) to outputs ($Q = A \oplus B$, $R = A \oplus C$, $P = A$) [30].

Bahar, Waheed [16] proposed two new methods for modeling a double Feynman gate (F2G) by QCA. They simulated them by QCADesigner and examined them regarding the intricacy (cell count) and space. The outcomes indicated that the introduced circuits have proper functionality. The first circuit has 51 cells arranged in a 0.06 μm^2 space; they obtained its results after three cycles delay. The second circuit has 96 cells arranged in a 0.93 μm^2 space. Figure 4a shows the layout of their first double Feynman gate, and Figure 4b shows their second double Feynman gate. The designs are promising for the upcoming processing methods, such as ultra-low-power quantum computers and digital circuits. They use three three-input majority and four inverter gates.

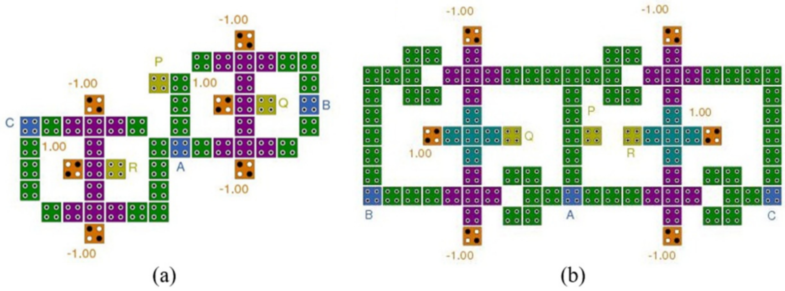

Figure 4. The layout of the double Feynman gates (proposed by Bahar, Waheed [16]): (**a**) the first design for double Feynman gates, and (**b**) the second design for double Feynman gates.

Furthermore, Sasamal, Singh [31] proposed an area-efficient and power-efficient reversible logic gate by the QCA. Using a two-input XOR gate, their models reached better functionality than NOT and BUFFER. They compared their functionality with those of the existing ones using the conventional metrics. Figure 5 shows the layout of their proposed gate. The number of QCA cells is less than other designs. Their proposed gate also reached 0.5 clock cycles delay. The power analysis verified that the introduced gate has a low energy dissipation. Thus, the introduced structure can improve the intricate nano-scale circuits' total functionality in the QCA. Figure 5 shows the double Feynman gate, plotting inputs (A, B, C) to outputs (Q = A ⊕ B, R = A ⊕ C, P = A). In this architecture, an extra gate is needed (for output *P*), while the two two-input XOR gates need the outputs *R* and *Q*. The introduced outline incorporates the XOR architecture with no necessity for three-input majority gates, in contrast with the existing models.

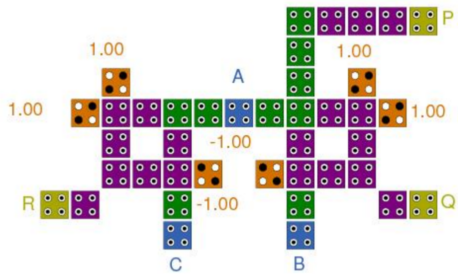

Figure 5. The layout of the double Feynman gate (proposed by Sasamal, Singh [31]).

Finally, Parhami [30] proposed a "Feynman double-gate". Figure 6 shows his proposed "Feynman double-gate". Considering the additional input and output and the control input A, he determined another controlled-NOT operation. His Feynman double-gate has its own inverse, as with the Feynman and the Fredkin. He introduced a QCA architecture for diverse reversible gates with a three-input majority gate as the primary unit. Still, a few outputs are not greatly polarized. For example, the output *P* is 8.63×10^{-3} and 5.80×10^{-3} for the Fredkin and Peres gates, respectively. Based on the results, the output misses the input signal above 14%, influencing model drivability.

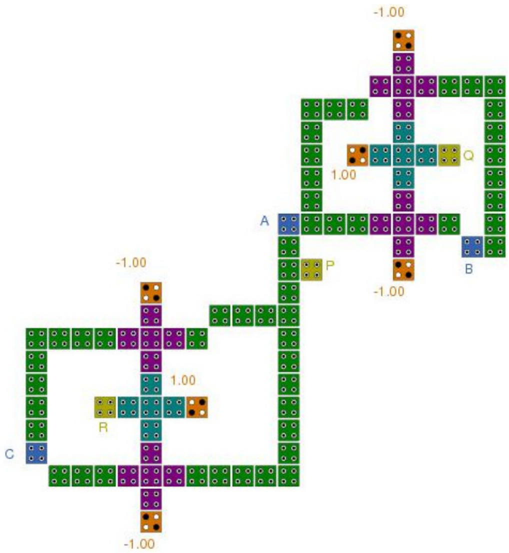

Figure 6. The layout of the Feynman double-gate (proposed by Parhami [30]).

3. Proposed Design

We propose a new reversible double Feynman gate in QCA technology implemented by the majority gates and XOR ones in the present study [32]. Our method converts multi-output irreversible functions into reversible ones. Hence, a reversible function has some characteristics listed below:

1. A unique mapping exists among the inputs and outputs.
2. Feedback is not acceptable.
3. Fan-out is not permitted.

However, according to [33,34], characteristics 2 and 3 are not essential for generating reversible functions in the QCA. Thus, we should create a one-to-one mapping among the inputs and outputs to convert the multi-output functions into reversible ones. We know numerous crucial reversible logic gates in the QCA technology. An n-input n-output logic device is a reversible logic gate with a unique mapping that specifies the outputs from the inputs and solely recovers the inputs. The Feynman gate has been considered to be a 2×2 gate; it is also known as controlled-NOT. O (P, Q) is known to be the output vector, while I (A, B) is considered the input vector. P = A, Q = A $\oplus$ B [Q = MV (MV (A′, B, -1), MV (A, B′, -1), 1] specifies the output.

A new optimized QCA-based double Feynman gate is presented utilizing three-input majority gates, along with the inverter gates. Figure 3 demonstrates mapping the inputs (A, B, C) to the outputs (R = A $\oplus$ C, Q = A $\oplus$ B, P = A) and the diagram of the introduced double Feynman gate. As shown in Figure 3, the primary logical figure for executing the double Feynman gate in the QCA has two key elements; six three-input majority gates and four inverter gates. This double Feynman gate was implemented in QCA technology with 46 cells and in an 0.05 μm^2 space, and simulated in the coplanar layer. Figure 7 indicates the QCA outline of the introduced double Feynman gate that operates in three clock zones, creates the two outputs R and Q in two clock zones, and establishes P output in one clock zone. In this double Feynman gate, the R and Q signals are supplied by three majority gates and two inverter ones.

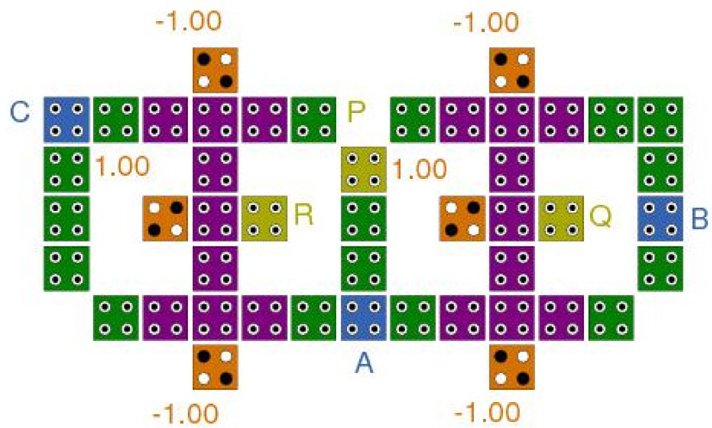

Figure 7. The proposed design of the double Feynman gate based on majority gates.

4. Results

In this part, the suggested QCA layout is evaluated and compared to current designs.

4.1. Simulation Tools

In the present study, the QCADesigner was used to build a quick and precise simulation and layout device for the QCA [35]. A key feature of the design is that the developers can easily simulate their designs in the QCADesigner. In addition, a standardized calling system and data formats make it simple to connect simulation engines into the QCADesigner. The existing version has two simulation engines [35–38]. In the QCADesigner, every single cell can be in one of four states (input, output, fixed, or normal). Figure 8 shows these modes.

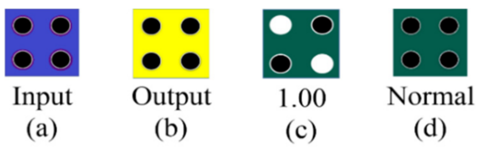

Figure 8. Cells in QCADesigner: (**a**) input cell, (**b**) output cell, (**c**) fixed and (**d**) normal [38].

4.2. Simulation Parameters

In the QCADesigner tool, the whole simulation computations and parameters have been adjusted to their default levels. Each cell's size is regulated to $18 \times 18\ \text{nm}^2$ with 5 nm diameter quantum dots. Bistable approximation factors have been set to 12.9 relative permittivity, 0.001 convergence tolerance, 9.8×10^{-22} J clock high, 3.8×10^{-23} J clock low, 11.5 nm layer separation, and 100 iterations per sample. The defined parameters in Table 2 were used for "Coherence Vector" and "Bistable Approximation" engines [35,39]. In this study, the simulation engine was set to "Bistable Approximation" and "Coherence Vector," and we used both of them to simulate the proposed circuit.

Table 2. QCADesigner parameters for "Coherence Vector" and "Bistable Approximation".

Parameter	Bistable Approximation Engine	Coherence Vector Engine
Cell size	$18 * 18\ \text{nm}^2$	$18 * 18\ \text{nm}^2$
Radius of effect	65 nm	80 nm
Relative permittivity	12.9000000	12.9000000
Clock high	9.8×10^{-22} J	9.8×10^{-22} J
Clock low	3.8×10^{-23} J	3.8×10^{-23} J

Table 2. *Cont.*

Parameter	Bistable Approximation Engine	Coherence Vector Engine
Clock amplitude factor	2.000000	2.000000
Clock shift	0.000000	0.000000
Layer separation	11.5000 nm	11.5000 nm
Maximum iterations per sample	100	-
Number of samples	12,800	-
Convergence tolerance	0.001000	-

4.3. Accuracy Analysis

This section demonstrates the results for the introduced circuits and compared them to those of the other circuits. Figure 9 shows the simulation results based on all combinations of A, B, and C inputs. The simulation outcomes confirmed that the suggested gate conducts well and designates the relevant production. In our model, A, B, and C are identified as inputs and P, Q, and R as the output cells. For example, Figure 9 demonstrates the right outputs of the proposed gate for inputs A = 1, B = 1, and C = 0, which are P = 1, Q = 0, and R = 1. The first significant waveform from P was produced at clock one. This design is coplanar. The desired outputs were collected from the coplanar layer. Based on Figure 9, we can understand the forceful polarization of the majority gates' output cell.

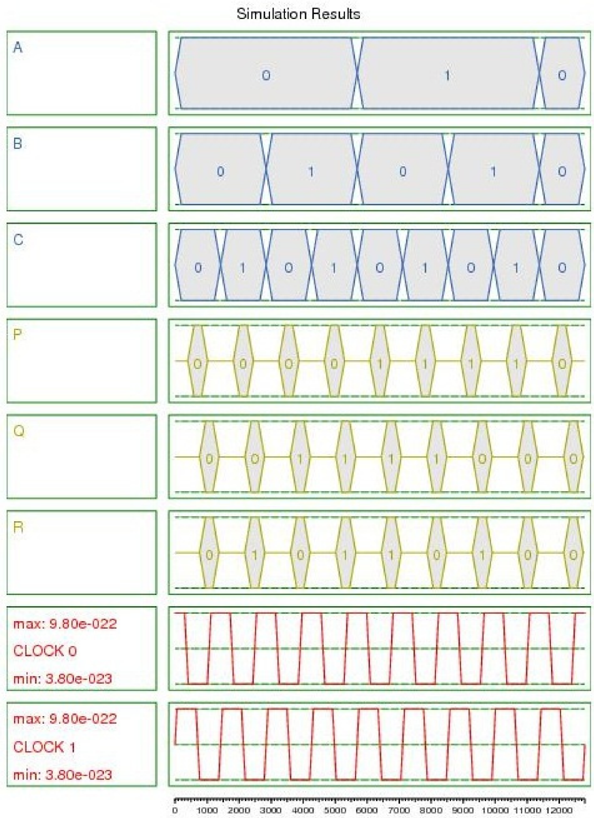

Figure 9. Simulation outcomes of the proposed double Feynman gate.

4.4. Comparisons

The simulation outcomes showed the correct operation of the proposed gate. Additionally, Table 3 demonstrates the comparison between the suggested double Feynman gate and the best existing gates. The comparison shows that the proposed method outperformed or is similar to the other ones regarding reducing the required space and cell counts. It has a compact architecture and lower cell counts than the best previous designs. When compared to the best-presented QCA double Feynman gate design with the majority gate, our designs result in a 10% increase in cell counts. Additionally, as indicated in Equations (1) and (2), significant design measurements such as the area latency product (ALP) and cost function can assess the efficiency of the QCA designs [40]:

$$\text{ALP} = \text{Area} \times \text{Latency} \tag{1}$$

$$\text{Cost} = \text{ALP} \times \text{Cell count} \tag{2}$$

Table 3. Comparison among the proposed and previous models.

Designs	Area (μm^2)	Cells	Delay	Layer(s)	Used Gates	ALP	ALP-Baased Cost
Our proposed model	0.05 μm^2	46	2 clock phase	1	Majority	0.1	4.6
Bahar, Waheed [16] (1)	0.06 μm^2	51	2 clock phase	1	Majority	0.12	6.12
Bahar, Waheed [16] (2)	0.09 μm^2	96	3 clock phase	1	Majority	0.27	25.92
Parhami [30]	0.19 μm^2	93	2 clock phase	1	Majority	0.38	35.34
Sasamal, Singh [31]	0.05 μm^2	40	2 clock phase	1	XOR	0.1	4

Table 3 compares the proposed design in terms of ALP and cost to the other state-of-the-art designs.

Furthermore, we can use another cost function named the QCA cost function to measure the proposed double Feynman gate's complexity. The QCA cost function (for majority gate-based circuits) is expressed as follows [41]:

$$Cost_{QCA} = \left(M^k + I + C^l\right) \times T^p,\ 1 \leq k, l, p \tag{3}$$

where I is the number of inverters, M is the number of majority gates, T is the circuit's delay, and C is the number of crossovers. Additionally, k, l, p are the weights for majority gate, crossover, and delay, respectively. In this part, different values (between 1 and 4) are considered for these weights to compare them better. As shown in Table 4, the suggested double Feynman gate is among the best circuits offered in terms of cost. The proposed design cost in four different types of experiment is better than the proposed designs in [16,30].

Table 4. QCA cost for the proposed reversible double Feynman gate and other layouts.

Designs	Cost$_{QCA}$ Mode 1 K, L, P = 1	Mode 2 K, L, P = 2	Mode 3 K, L, P = 3	Mode 4 K, L, P = 4
The proposed model	18	156	1752	20,784
Bahar, Waheed [16] (1)	20	160	1760	20,800
Bahar, Waheed [16] (2)	20	160	1760	20,800
Parhami [30]	30	360	5940	105,300
Sasamal, Singh [31]	14	108	1016	10,032

The temperature influence on the output cell polarization of the reversible gate is also very important. To test the average output polarization (AOP), QCADesigner can also be applied with a coherent vector stimulation device [42]. The AOP function is expressed as follows [43]:

$$AOP : \frac{Maximum - Minimum}{2} \tag{4}$$

Table 5 demonstrates the AOPs for each output cell of the suggested gate and novel schemes. In a range of 1–7 K (a typical temperature range in this technology), the suggested circuit performs efficiently, and the AOP is changed very slightly. These outcomes illustrate that the suggested model outperforms previous designs regarding stability in a diverse temperature range. As a result, the suggested design is extremely stable when the temperature is changed.

Table 5. AOP for the proposed reversible double Feynman gate.

Designs	Outputs	Temperature (K)						
		1	2	3	4	5	6	7
The proposed model	P	9.77	9.77	9.77	9.76	9.76	9.75	9.75
	Q	9.01	9.02	9.06	8.99	8.95	8.82	8.65
	R	9.06	9.04	9.02	8.97	8.89	8.80	8.73
Bahar, Waheed [16] (1)	P	9.27	9.27	9.27	9.25	9.22	9.05	9.00
	Q	9.06	9.06	9.06	9.02	8.95	8.72	8.65
	R	8.99	8.99	8.99	8.92	8.87	8.80	8.72
Bahar, Waheed [16] (2)	P	8.62	8.61	8.61	8.43	8.40	7.91	7.88
	Q	9.53	9.53	9.53	9.52	9.51	9.44	9.42
	R	9.53	9.53	9.53	9.52	9.52	9.49	9.42
Parhami [30]	P	8.71	8.70	8.70	8.60	8.52	8.10	8.03
	Q	9.53	9.53	9.53	9.52	9.52	9.48	9.42
	R	9.53	9.53	9.53	9.52	9.52	9.46	9.42
Sasamal, Singh [31]	P	9.54	9.54	9.54	9.53	9.53	9.49	9.44
	Q	9.50	9.50	9.50	9.48	9.48	9.40	9.37
	R	9.50	9.50	9.50	9.49	9.48	9.41	9.37

5. Conclusions and Future Work

High velocity, low power utilization, and high density make the QCA an appropriate nano-scale substitute for the CMOS. In contrast, the reversible double Feynman gate is a crucial circuit in logical processes. We proposed a new QCA architecture for a reversible double Feynman gate and simulated it by means of the QCAdesigner. The outcomes indicated that the introduced circuit in the present study generated a precise output. Thus, it has suitable functionality and performed better regarding cell counts, space, and time delay than previous designs. The simulation outcomes indicated that the model meaningfully reduced the required latency and cell number. The proposed coplanar double Feynman gate outperformed the other models (single-layer with coplanar application of a majority gate) regarding the number of cells and latency.

Based on the obtained results, we confirmed the efficiency of the proposed design. It can be useful for designing more intricate and better reversible QCA circuits. We can also use it as a useful construction block for bigger units to plan a reversible circuit. Finally, an n-bit Feynman gate can be designed by linking the proposed double Feynman gates in order to use less hardware.

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