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TEI-DTA: Optimizing a Vehicular Sensor Network Operating with Ultra-Low Power System-on-Chips

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Abstract: In the era of the Internet of Things (IoT), the interest and demand for embedded systems have been explosively increasing. In particular, vehicular sensor networks are one of the fields where IoT-oriented embedded devices (also known as IoT devices) are being actively used. These IoT devices are widely deployed in and out of the vehicle to check vehicle conditions, prevent accidents, and support autonomous driving, forming a vehicular sensor network. In particular, such sensor networks mainly consist of third-party devices that operate independently of the vehicle and run on their own batteries. After all, like all battery-powered embedded devices, the IoT devices for the vehicular sensor network also suffer from limited power sources, and thus research on how to design/operate them energy-efficiently is drawing attention from both academia and industry. This paper notes that the vehicular sensor network may be the best application for ultra-low power system on-chips (ULP SoCs). The ULP SoCs are mainly designed based on ultra-low voltage operating (ULV) circuits, and this paper aims to realize the energy-optimized driving of the network by applying state of the art (SoA) low-power techniques exploiting the unique characteristics of ULV circuits to the IoT devices in the vehicular sensor network. To this end, this paper proposes an optimal task assignment algorithm that can achieve the best energy-efficient drive of the target network by fully utilizing the SoA low power techniques for ULV circuits. Along with a detailed description of the proposed algorithm, this paper demonstrates the effectiveness of the proposed method by providing an in-depth evaluation process and experimental results for the proposed algorithm.

Keywords: optimal task assignment algorithm; vehicular sensor network; ultra-low power design; ultra-low voltage; temperature effect inversion; system-on-chip

Citation: Lee, S.-Y.; Lee, J.-H.; Lee, J.; Lee, W. TEI-DTA: Optimizing a Vehicular Sensor Network Operating with Ultra-Low Power System-on-Chips. *Electronics* **2021**, *10*, 1789. https://doi.org/10.3390/electronics10151789

Academic Editor: Nicu Bizon

Received: 21 June 2021
Accepted: 24 July 2021
Published: 26 July 2021

1. Introduction

As Internet of Things (IoT) has grown significantly, numerous sensors and embedded systems have been developed explosively and are being released as IoT devices [1–3]. One of the areas where IoT market trends are most prominent is the automotive industry. Vehicles that are transforming into a second main living space following customers' homes are using various auxiliary systems for safety and security as well as various conveniences. Some of these auxiliary systems have been produced by vehicle manufacturers and are already deployed to the vehicle during the vehicle manufacturing phase. Unfortunately, however, vehicle manufacturers cannot satisfy all the needs of a wide variety of customers, so a variety of third-party products are emerging to meet them.

Third-party IoT devices for vehicles are fitted to various places in the vehicle for various purposes, forming a single independent sensor network. These devices operate separately from the vehicle's engine control unit (ECU) and are powered by their own internal battery rather than by the power source in a vehicle. Therefore, they cannot be free from the inconvenience of charging, the biggest issue of battery-powered devices, which means how long they can be used on a single charge is the most important factor in determining their usefulness.

In this study, we conducted a study on the development of an ultra-efficient sensor network consisting of third-party IoT devices for vehicles. Of the various vehicular sensor networks, we targeted a network consisting of sensing units (called motes) that collect data through sensors and devices (called processing nodes) that receive and process data from the motes and send them to a base station, as shown in Figure 1. In particular, we studied how to develop the most energy-efficient processing nodes, as nodes may be the most power-hungry devices in the network. To this end, we first focused on ultra-low power (ULP) system-on-chips (SoCs). The ULP SoCs are designed primarily based on ultra-low voltage (ULV) operating circuits and consume up to tens of times less power than conventional SoCs operating with nominal supply voltage [4–8]. Of course, these ULP SoCs have the disadvantage of significant performance degradation compared to conventional SoCs (i.e., their clock frequency may be less than just tens of MHz [9]). However, considering that the computing capability required by our target processing nodes for the in-vehicle sensor network is not that high, and ULP SoC ultra-low power can significantly increase the life of the device, utilizing such ULP SoCs for the processing nodes may be the most suitable solution.

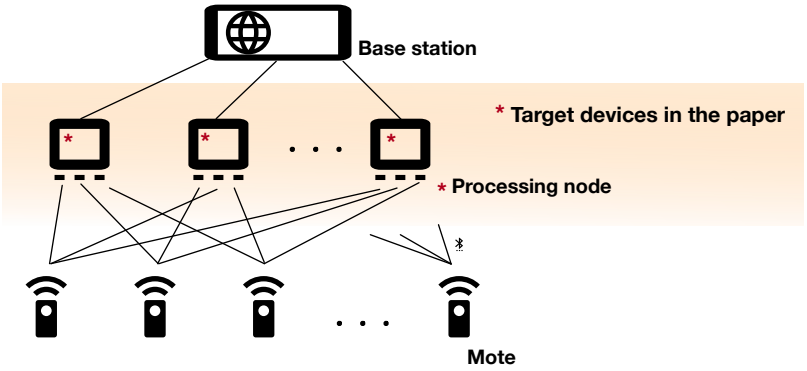

Figure 1. The target vehicular sensor network: the motes collect data and send them to the processing nodes. Each processing node processes the tasks assigned from the motes and sends the result to the base station. It is supposed that both the motes and processing nodes are distributed in different locations on the vehicle.

Next, we turned our attention to the recent studies that have shown that the ULP SoCs have very specific characteristics compared to nominal voltage operating SoCs: the ULP SoCs speed up as temperatures rise [10,11]. This phenomenon is called temperature effect inversion (TEI) [12], and a variety of state of the art low-power techniques have been published exploiting it [9,12–22]. More precisely, TEI-aware voltage scaling (TEI-VS) techniques saved power without performance degradation of SoCs [9,12–15], TEI-aware frequency upscaling (TEI-FS) showed that SoCs can operate in turbo mode with a linear increase in power consumption (and thus a very small increase in power consumption compared to the existing one) [16,17,23], and TEI-aware body biasing (TEI-BB) demonstrated that the low power potential utilizing the TEI phenomenon can be realized by further complementing TEI-VS and FS techniques [18,19]. In addition, recent research has confirmed the effectiveness of these methods on fabricated system-on-chips (SoCs) [9,20–22].

We then investigated the temperature distribution of various parts of a vehicle to determine whether our target environment is suitable for utilizing the TEI-aware low power techniques. Figure 2 shows the temperature distribution for each part of our target SUV vehicle. Since the processing nodes are distributed in various places in the vehicle, the sensor network we are targeting can be expected to have different temperatures depending on the location where the devices are attached. That is, since the processing nodes have different temperatures, they have different performance and power consumption/energy efficiency. Considering that this condition is the environment where the effectiveness of the TEI-aware low power techniques is expected the most, we decided to actively utilize

TEI-aware low power techniques. Then, to determine which of the various TEI-aware low power techniques will be most viable for our target system, we focused on the other important design factors of the target devices, design complexity and fabrication cost. TEI-VS and TEI-BB require a DC–DC converter and a body biasing controller, respectively, which increases the chip area and development cost of the SoC. By contrast, TEI-FS requires only the addition of a simple phase-locked loop (PLL) logic, which is advantageous in terms of area and cost. Therefore, we determined that TEI-FS is the most appropriate method for our target application, and decided to utilize this technique in this paper.

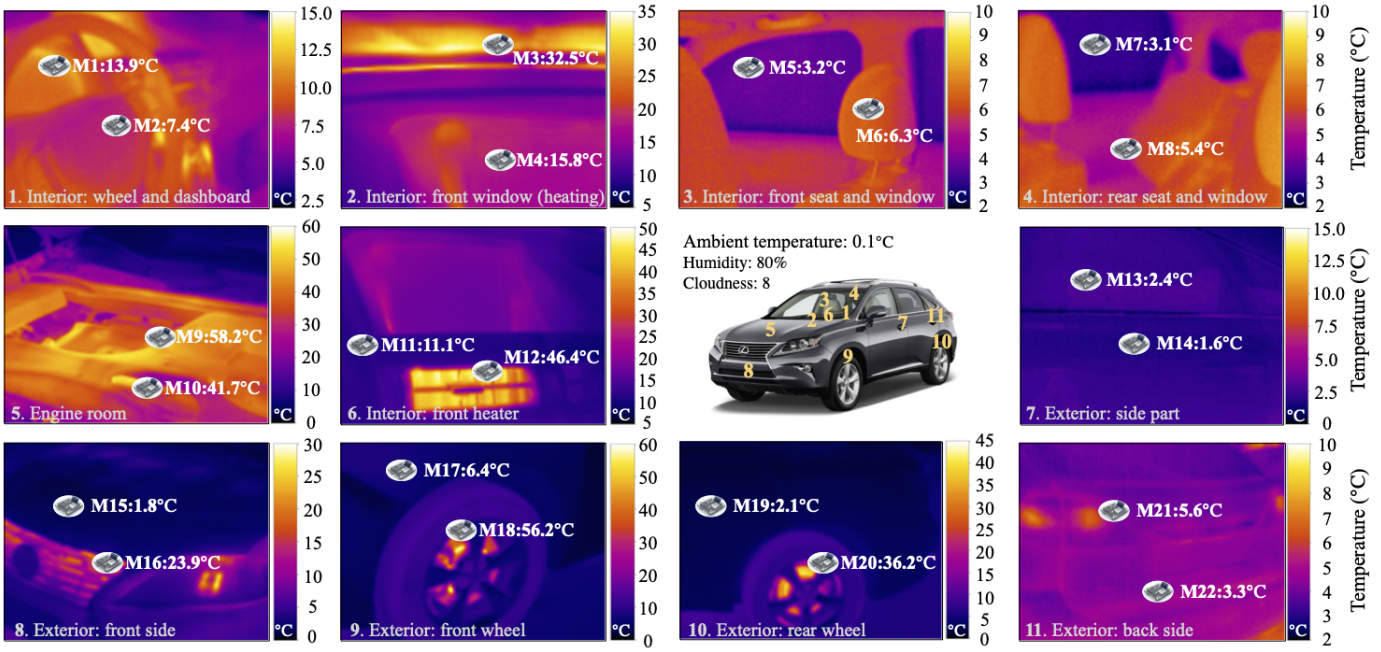

Figure 2. An example of the thermal distribution of a car: the car is divided into 11 parts and each thermal image of the part is taken with an infrared camera. The weather condition is reported in the middle of the figure, and each image includes the temperature information of two specific spots.

Finally, to realize the most energy-efficient operation of the sensor network of the vehicle configured with ULP SoC-based processing nodes, we defined the following problem: There are processing nodes that vary in energy efficiency depending on temperature, which share and process tasks given by motes. Then, we ask: Which processing node each task is assigned to, and at what speed each processing node operates, is the most energy-efficient way to finish all tasks in a given time? To solve this problem, we propose an optimization algorithm that can perform optimal task distribution while leveraging TEI-FS. In addition, in this paper, we demonstrate the superiority of algorithms based on real SoCs by performing performance evaluations of algorithms using the IoT devices built with the ULP SoCs.

The remainder of this paper is organized as follows. Section 2 elucidates the details of the TEI phenomenon and existing TEI-aware low power techniques including TEI-FS. Section 3 introduces the proposed task distribution algorithm utilizing TEI-FS for the vehicular sensor network. Next in Section 4, we perform the evaluation by using the ULP SoC that we made. Finally, Section 5 concludes the paper.

2. TEI-Aware Low Power Techniques: A Preliminary

The delay of a transistor τ_D in a circuit is directly affected by the on-current of the transistor I_{on} such that $\tau_D = \frac{C \cdot V_{dd}}{2 \cdot I_{on}}$, where C denotes the load capacitance of the transistor, and V_{dd} is the supply voltage. As I_{on} increases, the transistor switches faster, and vice versa.

Therefore, to analyze the TEI phenomenon, we first explore the theoretical model of I_{on}. $I_{on}(T)$ as a function of the circuit temperature T can be expressed as:

$$I_{on}(T) \propto \begin{cases} \mu(T) \cdot (V_{gs} - V_{th}(T))^{\beta} & : \text{if } V_{gs} > V_{th}, \quad (1) \\ \mu(T) \cdot e^{\frac{V_{gs} - V_{th}(T)}{S(T)}} & : \text{otherwise}, \quad (2) \end{cases}$$

where V_{gs} is the gate-source voltage, S denotes the subthreshold swing coefficient (also known as the body effect coefficient), μ is the carrier mobility, and β represents the velocity saturation effect factor (a typical value for β is 1.45.) S, μ, and V_{th} are temperature-dependent device parameters. When we first consider a transistors whereby T increases, μ and V_{th} both decrease while S increases. In (1), when the transistor operates in the super-threshold voltage regime (i.e., $V_{gs} > V_{th}$), I_{on} is mainly affected by μ (although V_{th} somewhat mitigates the effect of μ changes). Consequently, I_{on} decreases as T rises, which is the well-known negative relationship between I_{on} and T. Therefore, the worst-case timing corner for the commercial CMOS standard cell libraries operating in the superthreshold voltage regime occurs at the highest operating temperature. On the other hand, in (2), when the transistor operates in the ULV regime, V_{th} and S have an exponential and dominant influence on I_{on}, and the combined effect shows a significantly increased I_{on} as T rises [10]. This is called the TEI phenomenon [12]. In other words, circuits containing ULV operating transistors tend to become faster at higher temperatures. Figure 3 shows the TEI phenomenon in both CMOS and FinFET-based circuits. The figure is generated based on circuit simulations performed with a 55 nm DDC technology library and 20 nm/14 nm FinFET PTM libraries [24], each of which clearly shows that the delay decreases with rising temperature.

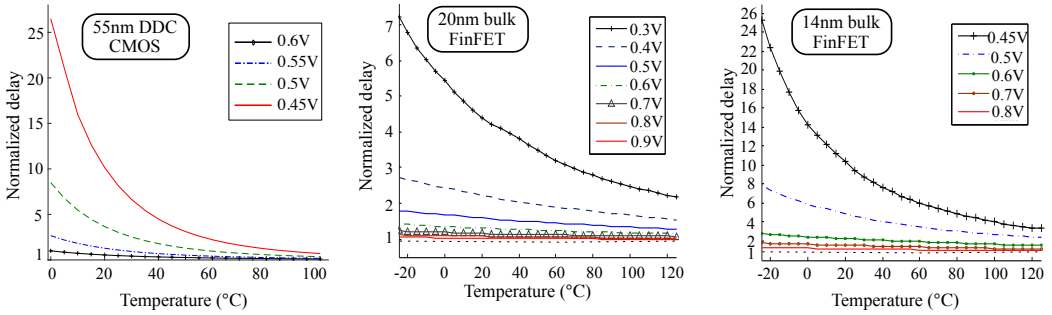

Figure 3. TEI phenomenons in 55 nm CMOS-based circuit and 20 nm/14 nm FinFET-based circuits.

The TEI-aware low power techniques actively exploit the TEI phenomenon to achieve the energy-efficient improvements. To theoretically analyze the characteristics and effects of each of these techniques, we first describe the power consumption of a circuit as follows [12,16]:

$$P_{dyn} = \alpha \cdot C \cdot V_{dd}^2 \cdot f, \qquad P_{lkg} = V_{dd} \cdot I_{off}, \quad (3)$$

where α, V_{dd}, f and I_{off} are the activity factor, supply voltage, operating frequency, and off-current of the circuit, respectively. Now, we focus on the best known TEI-aware low power technique, TEI-VS, that is based on the fact that the reference V_{dd} and f of the circuit are determined at the lowest temperature at which the worst case corner of the ULV operating circuit is. TEI-VS supplies circuits with the lowest V_{dd} that satisfies the target f at a given temperature, based on the idea that a voltage lower than the reference voltage (due to the TEI phenomenon) can be used. As in (3), lowering V_{dd} has great effects on both P_{dyn} and P_{lkg}. Figure 4 illustrates the effectiveness of TEI-VS. For example, Figure 4a shows the TEI phenomenon from the simulation with FO4 inverter chain based on CMOS 40n LP technology, while Figure 4b shows the resulting power consumption of the circuit with various V_{dd} and T. Note that the values in both figures are normalized. As seen from the

figures, when the target f is determined by a 0.5 V supply at −15 °C, V_{dd} can be reduced to 0.45, 0.40, and 0.35 V as the higher T's, which in turn saves power.

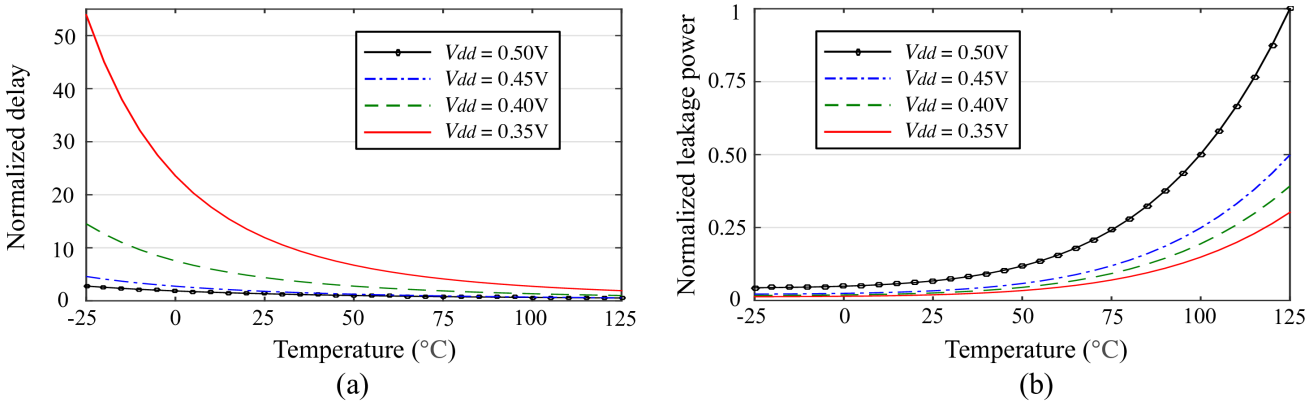

Figure 4. Simulation results of the FO4 inverter chain based on CMOS 40n LP process library: (**a**) normalized delay and (**b**) normalized leakage power consumption under a wide range of temperature values. The normalizations were carried out based on V_{dd} = 0.50 V at 125 °C.

TEI-BB is a technique used to change the threshold voltage (V_{th}) by adjusting the body voltage of the transistors and control the speed and power consumption of the circuit through this. Compared to TEI-VS, TEI-BB has the same principle of achieving power saving, except that the latter changes Vdd and the former changes the body voltage.

Meanwhile, TEI-FS focuses on f values that can scale up without V_{dd} upscaling at the high T. Compared to the conventional turbo-mode, where V_{dd} upscaling is required to operate the circuit at a higher frequency than reference f, thereby P_{dyn} in (3) cubically increases, TEI-FS can only increase f without V_{dd} upscaling at a given T, resulting in a linear increase in P_{dyn} and no change in P_{lkg}. Compared to the TEI-VS and TEI-BB that require a DC–DC converter(s) inducing area and cost overheads [17,25,26], TEI-FS requires a simple PLL controller that is relatively easy to develop and has a small form factor on the chip. Therefore, considering that our target SoCs for the vehicular sensor network need to be simple, economical, and easy to develop, in this paper we attempt to use TEI-FS for the target application.

3. TEI-Aware Task Assignment

As noticed in (3), when the frequency is scaled according to voltage scaling, P_{dyn} behaves as a cubic function of V_{dd}. However, P_{lkg} becomes a nearly linear function of V_{dd}, because other effects, such as drain induced barrier lower (DIBL), are very insignificant [27,28]. As V_{dd} becomes smaller into the ULV regime, P_{lkg} becomes a major contributor to the total power consumption of ULP devices (i.e., the processing nodes in this paper). Motivated by this fact, we focus on the power-gating (PG) technique, which saves power by shutting down power when the circuit is not working. This technique is one of the most powerful dynamic power management techniques used to reduce leakage power, and may be particularly effective in ULP SoCs, where leakage power accounts for a very large proportion of the total power consumption.

We then propose an idea that utilizes TEI-FS. More in detail, we propose a power gating and frequency upscaling (PGFS) technique that upscales the frequency (i.e., turbo-mode) of a device (i.e., processing node) at a certain high temperature and turns off some devices at low temperature. From this PGFS technique, the performance of the network can be maintained because the turbo-mode device takes over the tasks that were originally assigned to the turned-off devices and processes them in time. At the same time, the total power consumption of the network can be saved from the turned-off devices. More precisely, the amount of power saving from the power gated devices may be greater than

the amount of power increase due to the frequency upscaled devices. Again, this can be achieved, because TEI-FS does not need to scale up V_{dd} but increases P_{dyn} linearly.

To elaborate on the proposed idea, we consider situations in which there are three devices and three tasks in the vehicular sensor network. Each device operates at the default frequency $f_{default}$ that is determined by the worst-case corner (i.e., the lowest temperature) of the device. In other words, all of the devices should operate at least at $f_{default}$ to guarantee the normal operation. When we suppose that $f_{default}$ is 100 MHz, the required frequencies of the devices to complete the given tasks in time are 25, 30, and 50 MHz. In this situation, the conventional task assignment policy that evenly distributes the tasks to the three devices must not be optimal from the power saving perspective. Instead, using two devices and turning off one device, for instance, by assigning 25 and 30 MHz to one device and 50 MHz to another device, should be better to save power. Then, we are faced with the problem of which device to turn off. If TEI-FS is not enabled in the devices, the device at the highest temperature among the three devices must be turned off, because it consumes the highest leakage power (i.e., P_{lkg} is a function of temperature).

Then, when TEI-FS is taken into account, the optimal solution of the given situation must be changed. For example, assuming that one of the devices is at 50 °C, and this device can thus operate up to 200 MHz without voltage scaling, it would be better to assign all of the tasks to the device at the highest temperature, make it operate at 105 MHz, and turn off the others. Next, if we assume there is another device at 40 °C, thereby it can operate up to 150 MHz, it should be better to assign all of the tasks to this device and make its frequency 105 MHz, instead of using the device at 50 °C.

Although the above example is straightforward, assigning tasks to the devices at various temperatures and applying the proposed PGFS technique to the devices is combinatorially very challenging. To address this problem, we focus on the dynamic task assignment of the target vehicular sensor network, which aims to optimally configure the network between the tasks and devices for each certain time period D, so that the total power consumption of the devices should be minimized for D. Then, we assume that there are N devices, each of which has its own range of the operating frequency f. According to the given temperature T, the possible frequency range can be expressed as $f_{default} \leq f \leq f_{max}$, where $f_{default}$ is same for all devices, whereas f_{max} is the maximum possible frequency of the device that is determined at the current temperature of the device. In addition, we assume that there are M tasks with the required operating frequencies, $r_1,\ldots,r_M$. Finally, we face a combinatorial problem with the objective to minimize the overall power consumption of the devices by optimally assigning the tasks to the devices, determining the frequency of each device, and turning off the devices that do not have any assigned tasks. We formally describe the problem as follows:

$$
\begin{aligned}
&\text{Find } f_i \text{ and } x_{ij}.\\
&\text{Minimize } \; P_{total} = \sum_{i=1}^{N} P_i(f_i) \cdot x_{ij}\\
&\text{subject to } \; \sum_{j \in F_i} r_j \leq f_i \leq f_{max}(T_i), \;\; \forall i \in \{1,\ldots,N\}\\
&\qquad\qquad F_1 \cup \cdots \cup F_N = \{1,2,\ldots,M\}, \; F_i \cap F_k = \phi, \; \forall i \neq k\\
&\qquad\qquad x_{ij} \in \{0,1\}, \;\; \forall i \in \{1,\ldots,N\}, \;\; \forall j \in \{1,\ldots,M\}\\
&\qquad\qquad x_{ij} = 1, \; j^{th} \text{ mote is put into } i^{th} \text{ processing node.}
\end{aligned}
$$

where P_i and f_i are the power consumption and operating frequency of the i^{th} device, respectively; r_j is the required frequency of the processing node of the j^{th} task to complete the task in a given time, and F_i is the set of tasks that are assigned to the i^{th} device, whereby $F_1,\ldots,F_N$ are mutually exclusive. In the problem, we set assumptions as follows: (i) D is set to be longer enough relative to the breakeven-time in the power gating, so that the

energy loss from the power gating becomes negligible, and (ii) T_i is not changed in D (i.e., in general, device temperature changes very slowly).

The problem is NP-hard. To prove the NP hardness of the problem, we can reduce the problem by setting $f_i = f_{max}(T_i)$; then the problem is transformed to a *variable bin packing problem*. However, setting f_i to $f_{max}(T_i)$ can cause critical errors in the original problem in that devices with $f_{max}(T_i) > \sum_{j \in F_i} r_j$ always waste computing power. Therefore, we cannot fix f_i to $f_{max}(T_i)$ and apply algorithms for the variable bin packing problem.

To solve the problem, we propose an algorithm described in Algorithm 1: TEI-aware dynamic task assignment (TEI-DTA). In the algorithm, we first pay attention to the fact that if all the devices operate at $f_{default}$, using the devices in the low temperature regime should be preferred because such devices consume less P_{lkg}. We therefore fix all f_i to $f_{default}$ and assign the tasks to the devices in ascending order of T_i (cf. lines 2 to 5 in Algorithm 1). The *First-Fit-Decreasing* (FFD) algorithm for a bin packing problem is used in this task assignment. We sort all r_js in descending order (cf. lines at 6 in Algorithm 1), and perform the first-fit function, DO_FF, to initially assign the tasks to the devices (cf. line 10 in Algorithm 1). The details of DO_FF are elucidated in Algorithm 2, whereby it returns the ordered set of the used devices $\langle F_1, \ldots, F_k \rangle$. Note that we define such a set of the used devices F^* and an ordered set of its index K, and k is the maximum value of K (cf. lines at 7 and 8 in Algorithm 1).

Next, we try to consolidate $F^* = \langle F_1, .., F_k \rangle$ to the smaller number of devices that are in a high temperature regime, so as to exploit the PGFS technique to save power. In other words, if there are devices that can operate with $f_i \geq f_{default} + r_M$, so that these devices may be affordable to take over and process any task assigned to another devices, we apply these devices to a set of consolidation acceptors, $S_{acceptor}$, in the ascending order of the temperature (cf. line at 11 in Algorithm 1). Then, we investigate whether the consolidation to the device results in power saving. If $S_{acceptor}$ is empty, each device does not have space to expropriate the task from the other devices. Hence, there is no more work to proceed. Otherwise, the task reallocation is possible and the algorithm goes to the next step for comparing the power consumption saving (cf. line at 12 in Algorithm 1). To do that, let us define F_t to denote the target device with t in $S_{acceptor}$ and $PS(F_i)$ to denote the potential power savings of F_i from being consolidated to F_t. Note that $PS(F_i)$ equals to $P_{dyn}(f_i - \sum_{j \in F_i} r_j) + P_{lkg}(T_i)$ as shown in lines 9 in Algorithm 1.

As we treat $PS(F_i)$ and $\sum_{j \in F_i} r_j$, $F_{\forall i} \in F^*$ as value and weight, respectively, the problem to select F_is to maximize $\sum_{\text{selected } F_i} PS(F_i)$ while satisfying $\sum_{\text{selected } F_i} \sum_{j \in F_i} r_j \leq f_{max}(T_t)$ can be transformed into a 0–1 *knapsack problem*. We adopt a dynamic programming algorithm that is a well-known solution of the 0-1 knapsack problem. In line 17 in Algorithm 1, we perform a function DO_DP that is based on the dynamic programming algorithm. The details of the function DO_DP are described in Algorithm 3, whereby this function returns the maximum power saving values, the sum of the required frequency for processing tasks, and the list of the consolidated devices, each of which are saved in P_{save}, r_{sum}, and $Items$, respectively, in Algorithm 1. Finally, the comparison between P_{save} and the increasing power from the reallocated list of tasks that consists of both dynamic power and leakage power is performed, as shown in line 18 in Algorithm 1. If the former is larger than the latter, which means the consolidation saves power, we should set f_t to be $r_{sum} + \sum_{j \in F_t} r_j$, and F_t to be $F_t \cup F_{\forall i \in Item}$, and then set $F_{\forall i \in Item}$ to be $\emptyset$ and update F^* by adding F_s and deleting $F_{\forall i \in Item}$. Then, obviously, we should refresh K through the reallocated F^* and update $S_{acceptor}$ by adding $Item$ (cf. line at 19 to 22 in Algorithm 1). Otherwise, we do not perform any consolidation to F_t. Additionally, in line 23 in Algorithm 1, $S_{acceptor}$ is extended by adding $Item$ at the last sequentially to reinforce our procedure, which means repeating the proceeds of the loop (i.e., lines 14 to 24 in Algorithm 1) only for consolidated devices.

Algorithm 1 TEI-aware dynamic task assignment algorithm.

1: **procedure** DO_TEI_AWARE_TASK_ASSINGMENT
2: **for** $i = 1$; $i \leq N$; $i++$ **do**
3: $F_i = \phi$, $f_i = f_{default}$ ▷ Initialization
4: **end for**
5: **Sort** $F_i, \forall i \in \{1, \ldots, N\}$ in ascending order of the corresponding T_i using Counting Sort, so that $T_1 \leq \ldots \leq T_N$.
6: **Sort** $r_j, \forall j \in \{1, \ldots, M\}$ in descending order using Counting Sort, so that $r_1 \geq \ldots \geq r_M$.
7: **Define** $F^* = \langle F_1, \ldots, F_k \rangle$ is the ordered set of the processing nodes that are used, and P^* is the associate total power $P(F^*)$.
8: **Define** $K = \{1, \ldots, k\}$ is the ordered set of $i, \forall F_i \in F^*$ and k is the maximum value of K.
9: **Define** $PS(F_i)$ is the potential power saving of F_i, whereby $PS(F_i) = P_{dyn}(f_i - \sum_{j \in F_i} r_j) + P_{lkg}(T_i)$. P_{dyn} and P_{lkg} can be estimated from a power model based on (3) or pre-measured data in a LUT.
10: $F^* =$ **Do_FF**$(\langle F_1, \ldots, F_N \rangle, \{1, \ldots, M\}, M, N)$ ▷ Do_FF is presented in Algorithm 2.
11: $S_{acceptor}$ is the ascending ordered set of t satisfying $f_{max}(T_t) - \sum_{j \in F_t} r_j \geq r_M$.
12: If $S_{acceptor}$ empty, stop the procedure. Otherwise, go to the next.
13: **for** $t \in S_{acceptor}$ **do**
14: $v = [PS(F_1), \ldots, PS(F_k), \ldots, PS(F_N)]$
15: $w = [\sum_{j \in F_1} r_j, .., \sum_{j \in F_k} r_j, \ldots, \sum_{j \in F_N} r_j]$
16: $W = f_{max}(T_t) - \sum_{j \in F_t} r_j$
17: $\{P_{save}, r_{sum}, Item\} =$**DO_DP**$(v, w, t, K, W)$ ▷ Do_DP is presented in Algorithm 3.
18: **if** $P_{save} > P_{over}(f_t, r_{sum}, T_t)$ **then**
19: $f_t = r_{sum} + \sum_{j \in F_t} r_j$ ▷ Increase f_t by r_{sum}.
20: $f_i = 0, \forall i \in Item$ ▷ Update f_i.
21: $F_t = F_t \cup F_{\forall i \in Item}$, $F_{\forall i \in Item} = \phi$ ▷ Consolidation.
22: Add F_t to F^*. Delete F_i's $(\forall i \in Item)$ from F^*. Update K from F^*. ▷ Update F^* and K.
23: Add $Item$ to $S_{acceptor}$ at the last sequentially. ▷ Extend $S_{acceptor}$.
24: **end if**
25: **end for**
26: **end procedure**

The above consolidation procedure is performed for all devices that can accept an additional task (i.e., $\{\forall F_s,\ t \leq s \leq N\}$) and the accompanying f_is are kept updated until the end of the procedure. Finally, the final F^* provides the information regarding which devices should be turned on or off, where to assign the task of each device, and how to set up the frequency of each turned-on device. Additionally, P^* defined in line 7 in Algorithm 1 yields the total power consumption of the final F^*.

Algorithm 2 First-fit algorithm for the initial packing.

function DO_FF(Set_{device}, Set_{task}, M, N)
  f_i is the corresponding frequency of F_i in Set_{device}.
  r_j is the corresponding frequency of j motes in Set_{task}.
  for $j = 1;\ j \leq M;\ j++$ **do**
    for $i = 1;\ i \leq N;\ i++$ **do**
      if $r_j \leq f_i$ **then** ▷ if r_j fits in i^{th} device,
        $F_i = F_i \cup \{j\}$, $f_i = f_i - r_j$ ▷ Assign j in i.
        Break ▷ Break the loop and pack the next.
      end if
    end for
  end for
  return an ordered set of F_k's, if $F_k \neq \phi$, $\forall k \in \{1, \ldots, N\}$
end function

Algorithm 3 Dynamic programing for the consolidation.

function DO_DP(v,w,s,K,W)
  for $j = 1;\ j \leq W;\ j++$ **do** $m[0, j] = 0$
  end for
  for $i = 1;\ i \leq k;\ i++$ **do**
    for $j = 1;\ j \leq W;\ j++$ **do**
      if $w[i] \leq j$ *and* $i \in \{K \setminus \{s\}\}$ **then**
        $m[i, j] = \max(m[i-1, j], m[i-1, j-w[i]] + v[i])$
      else $m[i, j] = m[i-1, j]$
      end if
    end for
  end for ▷ $m[n, W]$ is the maximum value.
  $i = k, j = W, S = \phi$
  while $i, j > 0$ **do** ▷ This is to find the used items.
    if $m[i, j] \neq m[i-1, j]$ **then**
      $S = S \cup \{i\},\ j = j - w[i],\ i = i - 1$
    else $i = i - 1$
    end if
  end while
  return $m[n, W]$, $\sum_{i \in S} w[i]$, S
end function

Applying the proposed algorithm to a device, i.e., a processing node in this paper, may require additional hardware support. For example, a temperature sensor to check the temperature changes in the device [29] or a ring-oscillator-based performance monitoring logic to determine the circuit speed [30] may be necessary to perform the frequency scaling at runtime. In addition, since the algorithm utilizes P_{dyn} and P_{lkg}, there should be a way to estimate these values. To this end, as a software-based approach, a power model based on (3) can be exploited [31], or as a hardware-based approach, a look-up table (LUT) storing pre-measured P_{dyn} and P_{lkg} values for all cases can be adopted [32]. In this study, we mounted an on-board temperature sensor on the prototype of the processing node and measured the power consumption of this prototype device at various temperatures through experiments. However, the functionality and effectiveness verification of the proposed

algorithm was derived through simulations using the measured above data. A detailed description of the experimental work is provided in the following chapter.

4. Experimental work

4.1. Experimental Setup

To evaluate the effectiveness of the proposed TEI-DTA algorithm, we first attempted to acquire TEI-FS data measured from the target IoT devices. To do that, we utilized our TEI-inspired SoC platform (TIP) [8] and the TIP prototyping SoC operating with 50 MHz operating frequency at 0.7 V supply [9]. More in detail, the TIP is configured with dual RISC-V (ORCA) cores, micro network-on-chip (NoC), and peripherals, with a detailed architecture illustrated in Figure 5. Based on the TIP, the ULP SoC prototype was fabricated using 28 nm FDSOI technology, and the die photo of this SoC prototype is shown in Figure 6a. Then, by embedding the SoC prototype into the test board that has an on-board temperature sensor and a programmable oscillator to enable adjustment of the of the chip clock frequency at run time, the processing node prototype for the target sensor network was established, which is described in Figure 6b. Finally, we placed this prototype in an environmental test chamber, as shown in Figure 7, and measured the TEI-FS effect of the devices by changing the temperature of the devices. From this experimental work, we first checked that in room temperature (25 °C), the device can maintain its operating frequency (50 MHz) at a 0.48 V supply, which is much lower than the nominal voltage of 0.7 V, and from this, we confirmed that the TEI phenomenon is evident on this device. Next, using that condition as a reference, we measured the maximum operating frequency for each temperature of the device when the supply voltage was fixed at 0.48 V, and the result is shown in Figure 8. From these experiments, we obtained data that the target device operated at 20 MHz at −10 °C, but with increasing temperatures, it operated at 40 MHz at 10 °C, 60 MHz at 45 °C, and 75 MHz at 80 °C without any change in supply voltage. These data and the corresponding power consumption measured at each circumstance point, as also shown in Figure 8, were utilized as resources during the TEI-DTA algorithm evaluation process.

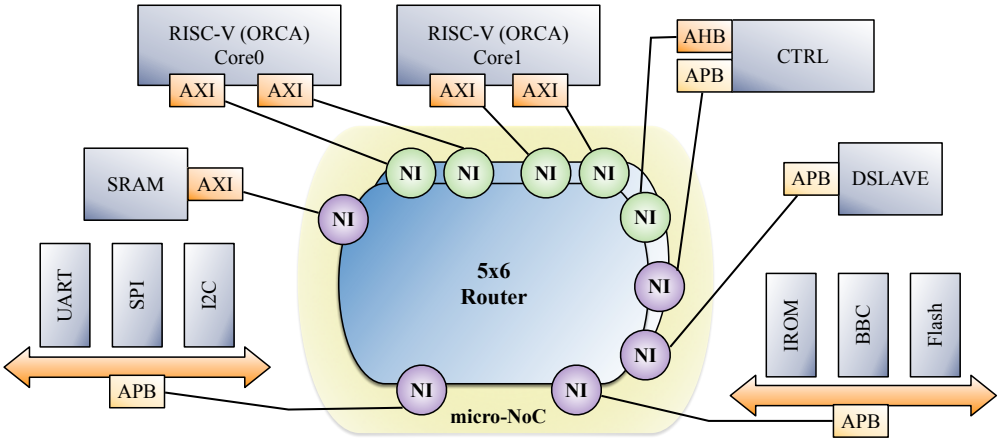

Figure 5. Architecture of the TEI-inspired SoC platform used for our target ULP SoC. In the figure, APB, AHB, and AXI are AMBA protocols, NI, and CTRL, respectively, representing the network interface and controller, and the rest are typical peripherals.

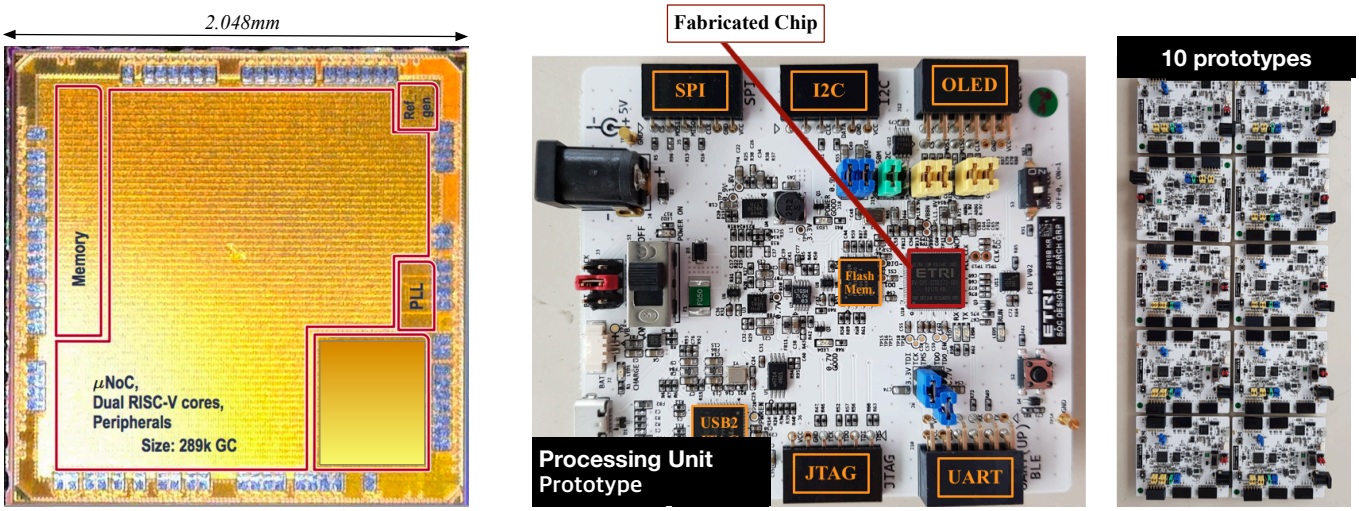

Figure 6. (**a**) Silicon Die photo of the prototyping SoC, and (**b**) the IoT device boards with the prototyping SoCs (sourced from [9]).

Figure 7. The experimental environment used to test the TEI phenomenon of the devices (sourced from [9]).

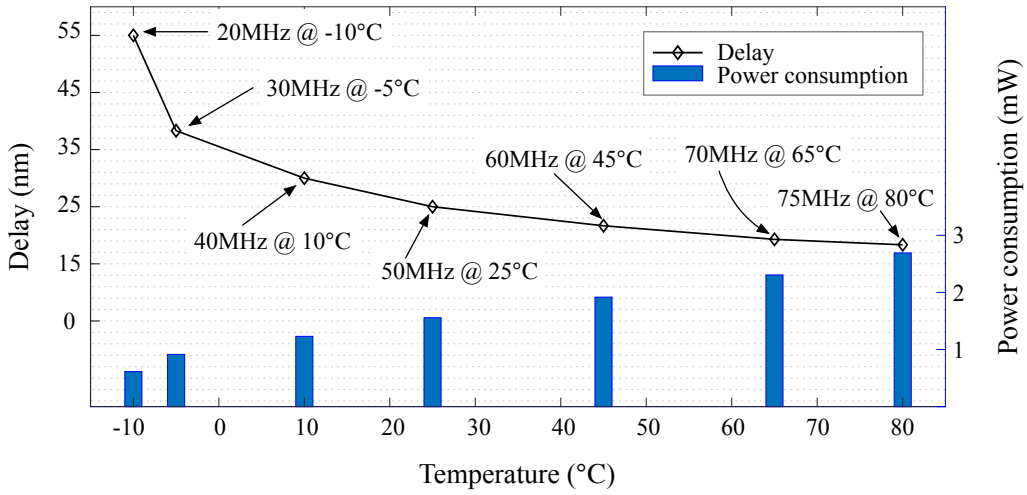

Figure 8. Measured result of scalable frequency and corresponding power consumption of the prototyping processing unit at each temperature point when TEI-FS is employed and V_{dd} = 0.48 V.

4.2. Evaluation of the TEI-DTA Algorithm

To demonstrate the superiority of the proposed TEI-DTA algorithm, we first defined a metric that represents how much power consumption improves when TEI-DTA is applied over the total power consumption of the existing sensor network, which is:

$$P_{gain} = \frac{P_{original} - P_{TEI-DTA}}{P_{original}}, \tag{4}$$

where P_{gain} is the power saving ratio, and $P_{original}$ and $P_{TEI-DTA}$ are the power consumed when task assignment is not specifically configured and after configuration with TEI-DTA, respectively. Then, we set both M and N in the TEI-DTA algorithm to 22, which is based on the target sensor network configuration described in Figure 2. During the evaluations, the power consumption of each processing unit was derived based on data measured by placing the processing unit prototype in a chamber and varying the temperature and operating frequency.

For the initial evaluation of the proposed TEI-DTA in the vehicular sensor networks, we set the operating temperature range of devices from −15 to 80 °C. We also defined $f_{default}$, which is a minimum operating frequency that ensures that the required frequency of the processing unit for the task is limited to less than this frequency. Then, we carried out a Monte Carlo simulation with five different group of tasks, each of whose required frequency average of the tasks is 30%, 40%, 50%, 60%, and 70% for $f_{default}$, as described in Figure 9. As shown in the figures and the following Table 1 that reports the results in detail, the TEI-DTA algorithm achieved power savings in every condition of the simulation. When the required frequency was 30%, the average power saving ratio achieved up to 76.5%, and when the required frequency was reduced, it decreased to 65.7%, 56.5%, 46.3%, and 37.9%, respectively. These results imply that the smaller the sizes of tasks, the greater the power gain of our method. This is due to the fact that the smaller the task, the more tasks can occupy one device, which increases the number of power-gated devices, resulting in a lower total leakage power in the network.

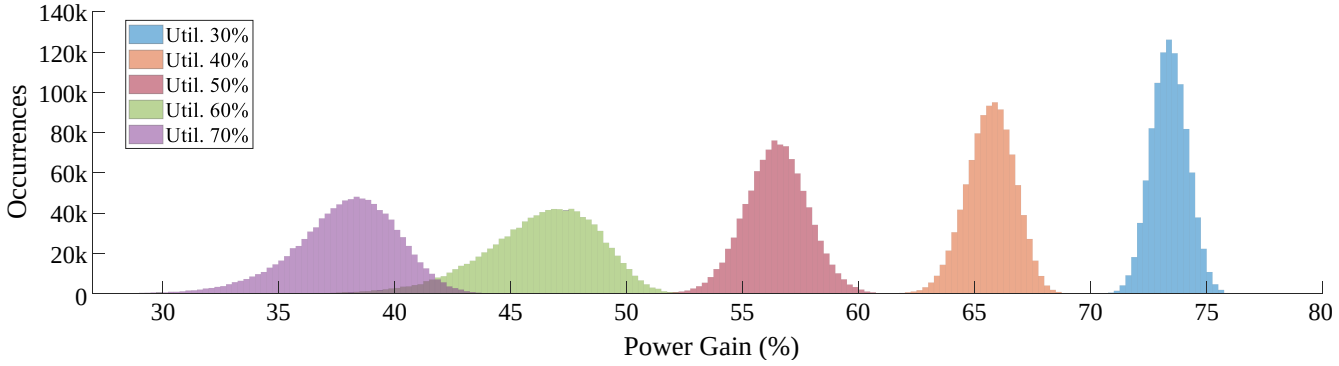

Figure 9. Monte Carlo simulation results of the power gain for each required frequency.

Table 1. Average and extreme values of P_{gain} for each required frequency.

Frequency			**70%**		**60%**		**50%**		**40%**		**30%**	
P_{gain} (%)	Average		37.9		46.3		56.5		65.7		73.4	
	Min.	Max.	23.0	45.3	30.0	53.8	49.7	61.8	60.3	69.3	70.4	76.5

We demonstrated through initial experiments that TEI-DTA can save power at a wide range of operating temperatures, followed by experiments to demonstrate the effectiveness of TEI-DTA in more practical situations. To this end, we conducted five real-world case studies, including the real-world vehicle environment in Figure 2. We have already analyzed the impact of the required frequency average of the tasks on power saving through

previous experiments, so in these case studies, we fixed the required frequency average of the tasks at 70%. For Case #1, the measured conditions in cold weather in Figure 2 were utilized. Case #2 represents a hot weather device operating environment, which is the opposite of Case #1. In addition, we set Cases #3, #4, and #5 to be under operating environments at low ($-10 \sim 10$ °C), middle ($20 \sim 40$ °C), and high ($60 \sim 80$ °C) temperature ranges, respectively.

100,000 Monte Carlo simulations were performed by applying the proposed TEI-DTA for each case, and finally Table 2 reports the average result value (P_{gain}) for each case. As can be seen from the table, the effectiveness of TEI-DTA in Case #1 achieved a 52.5% power consumption improvement, and that in Case #2 increased further to 55.8%. In addition, by analyzing the results in Cases #3, #4, and #5, we could confirm that the P_{gain} of the TEI-DTA grows when devices in the network are in a high-temperature environment (the average P_{gain} reached up to 61.6%), while P_{gain} is relatively low at low temperature, but the effect remains excellent (49%).

Table 2. Average P_{gain} results for the case studies.

Case	**#1**	**#2**	**#3**	**#4**	**#5**
Temperature	Cold weather	Hot weather	Low ($-10 \sim 10$ °C)	Middle ($20 \sim 40$°C)	High ($60 \sim 80$ °C)
P_{gain} (%)	52.5	55.8	49.0	53.0	61.6

5. Conclusions

In this paper, we noted that while the demand for vehicular sensor networks based on third-party IoT devices is continuously increasing, development is being delayed due to the limitation that these IoT devices must be operated with limited power sources. To address this problem, we focused on the ULP SoCs based on ULV operating circuits, which are best suited for energy-efficient vehicle sensor networks. In particular, we paid attention to the special characteristics of these ULP SoCs, i.e., operating speed increases as the temperature rises due to the TEI phenomenon, and explored the latest low-power techniques, i.e., TEI-aware low power techniques, exploiting these characteristics. Among the various TEI-aware low-power techniques, we determined that TEI-FS is the most suitable for the target sensor network, and devised a method to drive the sensor network with the highest energy efficiency by unleashing the full potential of TEI-FS. To this end, we proposed an optimal task assignment algorithm called TEI-DTA. Along with the detailed description of the proposed algorithm, an in-depth evaluation process for the fabricated SoC and intensive experimental work based on the measured data were performed to evaluate the effectiveness of this algorithm. As a result, the proposed algorithm achieved a significant power consumption reduction effect in the target vehicular sensor network. We expect that the proposed algorithm and demonstration will be utilized as a low-power technology in IoT applications with distinct temperature distribution such as the vehicular sensor network targeted in this paper.

Author Contributions: S.-Y.L., J.-H.L., J.L. and W.L. were the main researchers who initiated and organized research reported in the paper, and all authors were responsible for analyzing the simulation results and writing the paper. All authors have read and agreed to the published version of the manuscript.

Funding: This research was partially supported by the Chung-Ang University Research Scholarship Grants in 2019, and partially supported by the National R&D Program through the National Research Foundation of Korea (NRF) funded by Ministry of Science and ICT (2021M3H2A1038042).

Data Availability Statement: The data presented in this study are available on request from the corresponding author.

Conflicts of Interest: The authors declare no conflict of interest.

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