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An 87% Power-Efficiency Hybrid of Voltage- and Current-Mode Line Driver with an Adaptive Amplitude Tuning

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Abstract: This brief presents a hybrid of voltage- and current-mode line drivers for the turbo controller area network (CAN). The current-mode scheme prevents signal attenuation caused by source termination resistors, and it enhances signal power efficiency. On top of that, an adaptive amplitude tuning is implemented to mitigate non-linearity and closed-loop gain variations against load impedance variations. The proposed line driver achieves 87.0% power-efficiency and total harmonic distortion, plus noise (THD+N) of -49.0 dB at an input frequency of 40 MHz and output swing of 2.8 V_{PP} differential. The adaptive amplitude tuning allows load impedance variations from 80 Ω to 160 Ω. The total power consumption is 37.6 mW with a 1.8 V supply voltage in 180 nm CMOS, and it occupies 0.377 mm².

Keywords: adaptive amplitude tuning; bus lines; current mode; line driver; turbo controller area network



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Citation: Park, C.; Lee, M. An 87% Power-Efficiency Hybrid of Voltage- and Current-Mode Line Driver with an Adaptive Amplitude Tuning. *Electronics* **2021**, *10*, 1785. <https://doi.org/10.3390/electronics10151785>

Academic Editor: Davide De Caro

Received: 25 June 2021

Accepted: 18 July 2021

Published: 26 July 2021

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1. Introduction

Line drivers (LDs) have been widely used in various wire-lined channels, such as integrated service digital network (ISDN) transceivers, digital subscriber line (DSL), and cable modems [1]. The LD acts as an analog buffer, which transmits sufficient output current to drive the low-load impedances. The LD's significant design aspects are high output swing, low distortion, high signal power efficiency (η_{power}), and appropriate impedance matchings for line impedance variations over process variations [1]. Voltage-mode line drivers (VMLDs) [2–4], Ref. [5] have been widely used due to their excellent linearity and power consumption since they source fewer currents to the load than current-mode line drivers (CMLDs) [6]. A fully differential difference VMLD with a dual common-mode feedback (CMFB) circuit [7] allows a faster transient response, which results in an improved linearity. Another VMLD assisted with an active termination circuit and dynamic power supply control circuit [3] allows enhanced power efficiency. However, the series source termination in the VMLDs attenuates the total signal power delivered to the channel lines [8], as shown in Figure 1. In addition, the VMLD topologies typically require a 1-to-N transformer to increase its signal swings on the channel lines. Therefore, the VMLD architecture features low η_{power} and typically requires extra passive components.

On the other hand, CMLDs [8–10] consist of parallel source termination, and the signal does not suffer from matching attenuation, which leads to higher η_{power} . The higher signal swing also guarantees improved robustness against external noise and electromagnetic interference (EMI). The output stage of a current-mode H-bridge cascode, assisted with local auxiliary loops [8], enhances mirroring accuracy to alleviate the signal linearity. However, it requires additional circuits and power consumption for the auxiliary amplifiers, and the cascode topology reduces the allowable output signal swings. Current-mirroring topologies with an adaptive termination tuning [1,5,9] mitigate closed-loop variations and unmatched termination against the transmission line variations. However, the tuning

technique reduces the output signal swing due to the small series resistance between the supply and the output nodes.

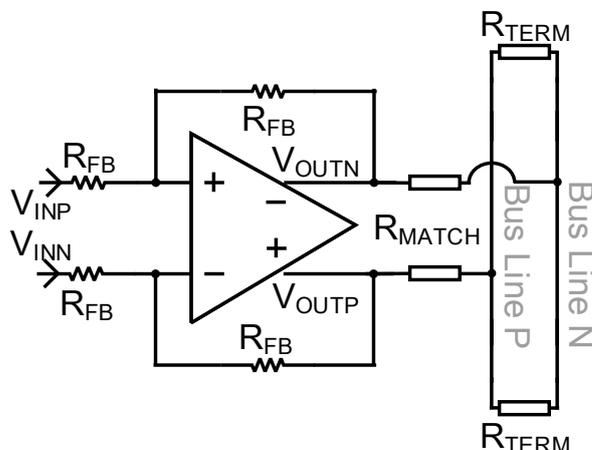


Figure 1. Architecture of a voltage-mode line driver.

This paper presents a hybrid of closed-loop voltage-mode using an operational amplifier (OPAMP) and open-loop current-mode class-AB current replica cells with a digital-based adaptive amplitude tuning (AAT). The AAT controls the current replica cells' sizes to prevent the closed-loop voltage gain and the signal linearity variations against the load impedance variations in a range of 80Ω to 160Ω with a 32-bit tuning step. The tuning circuit reduces the two variations without degrading the η_{power} and the output signal swings. The proposed hybrid of a VMLD and CMLD achieves total harmonic distortion plus noise (THD+N) of -49.0 dB at an input frequency of 40 MHz and an output swing of $2.8 V_{PP}$ differential. The proposed LD is designed for a turbo controller area network (CAN) [11] for in-vehicle networks, as shown in Figure 2. The turbo CAN process modulates analog data rather than binary signals to boost the data transmission speed from 10 Mbps to over 100 Mbps. Each end of the bus lines is terminated with 120Ω .

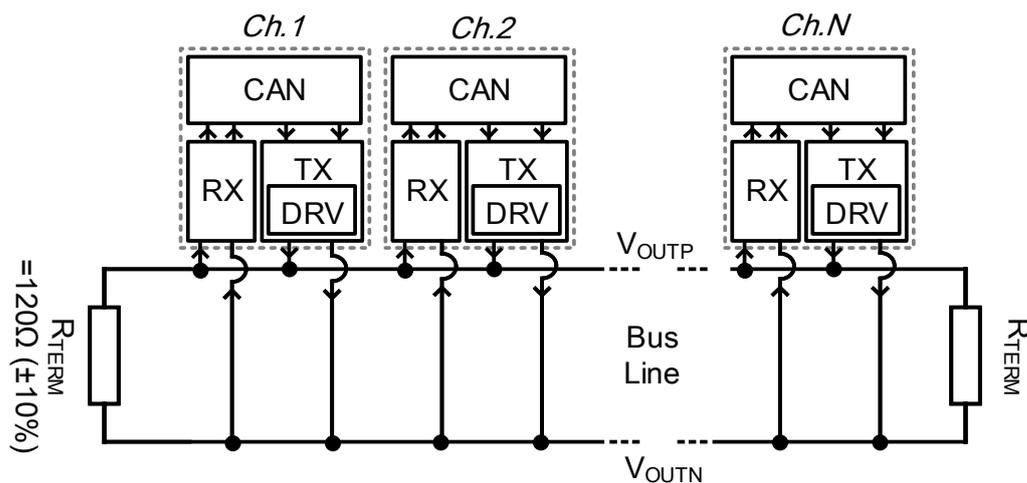


Figure 2. Block diagram of controller area network (CAN).

This paper is organized as follows. Section 2 introduces the architecture and analysis of the proposed LD. Section 3 describes the analysis of the proposed AAT. Section 4 delivers the measurement results of the driver, and Section 5 draws the conclusions.

2. Proposed Hybrid of Voltage- and Current-Mode Line Driver

2.1. Architecture of the Hybrid of a Voltage- and a Current-Mode Line Driver

Figure 3 displays the overall block diagram of the proposed hybrid of a VMLD and CMLD, including an AAT. The proposed LD consists of two different blocks: a unity-gain closed-loop OPAMP and class-AB current replica cells. The unity-gain OPAMP converts input differential voltage signals to currents. The signal currents flow through the OPAMP’s output stage (M_{PO} , M_{NO}), and are replicated to the current replica cells (M_{POR} , M_{NOR} , M_{PORV} , and M_{NORV}). The mirroring ratio N represents the replication ratio between $M_{P(N)O}$ and $M_{P(N)OR} + M_{P(N)ORV}$. The floating batteries $M_{PBa,b}$ and $M_{NBa,b}$ in Figure 4 define the shared gate-to-source voltage (V_{GS}) of the OPAMP’s output stage and the replica cells. The V_{GS} is defined with V_{FBP} , V_{FBN} , and the supply in Figure 3. The feedback resistor R_{FB} should be set according to the mirroring ratio N and the output impedance R_L , the impedance seen at termination resistor R_{TERM} and the impedance matching resistor R_{MATCH} in Figure 3. The OPAMP can drive the appropriate amount of signal currents by matching the R_{FB} value to the equivalent load impedance (R_L). The required value of R_{FB} can be derived with the LD’s ideal closed-loop voltage gain (A_V) as in Equation (1):

$$A_V = \frac{V_{OUTP} - V_{OUTN}}{V_{INP} - V_{INN}} = -\frac{N}{2R_{FB}} \left(\frac{R_{TERM} \cdot R_{MATCH}}{R_{TERM} + 2R_{MATCH}} \right). \quad (1)$$

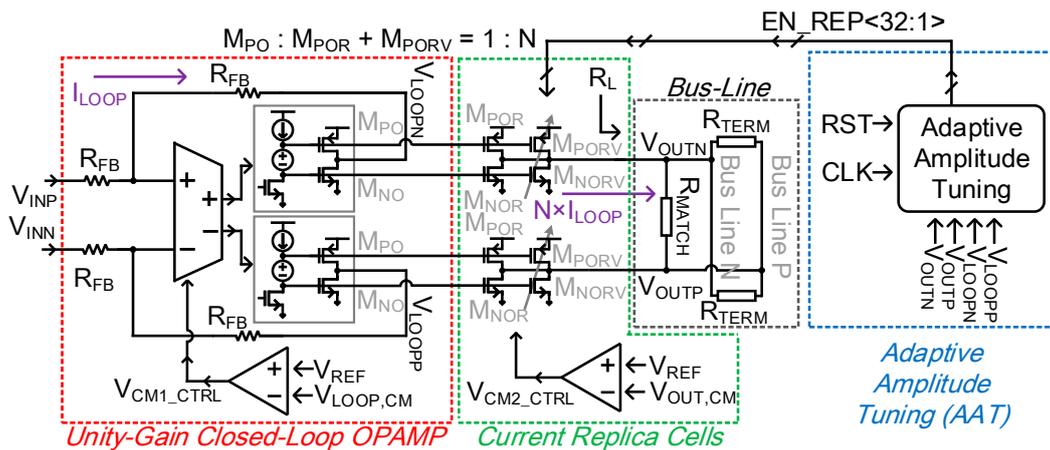


Figure 3. Block diagram of the proposed current-mode line driver with an adaptive amplitude tuning.

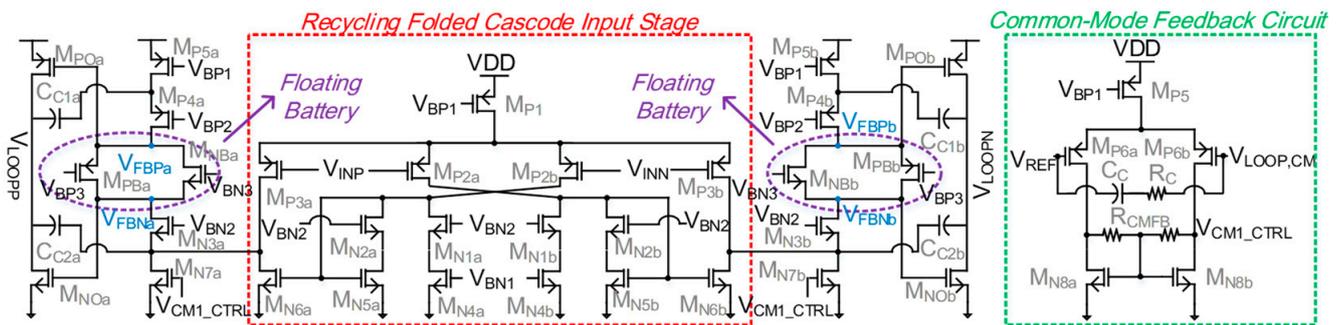


Figure 4. Schematic of the rail-to-rail output two-stage recycling folded cascode OPAMP including the CMFB circuit (bias circuit is omitted for simplicity).

If $N = 4$, then R_{FB} should be 60Ω to guarantee a unity-gain ($A_V = -1$) since $R_{TERM} = 120 \Omega$ and $R_{MATCH} = 60 \Omega$.

2.2. Architecture of the Operational Amplifier

Figure 4 describes the schematic of the OPAMP and its CMFB circuit. The two-stage OPAMP is designed with a recycling folded cascode architecture for the first input

stage. Compared to the conventional folded cascode architecture, the recycling folded cascode can further improve slew-rate and input equivalent trans-conductance [12]. The improvements result in enhanced loop-gain and unity-gain frequency (UGF). In addition, the class-AB output stage with floating batteries guarantees better power-efficiency for the output stage. The CMFB is designed with local CMFB resistors R_{CMFB} and null-resistor compensation. The null-resistor R_C generates a left-half-plane (LHP) zero, which guarantees an enhanced common-mode phase margin (PM) [13]. In addition, two different CMFB loops are implemented in the proposed hybrid LD to set appropriate common-mode levels for both the closed-loop OPAMP and the current replica cells. $V_{LOOP,CM}$ and $V_{OUT,CM}$ are the common-mode voltages of the closed-loop OPAMP and the bus line voltages, respectively. The dual CMFB topology also allows a faster transient common-mode signal response, which results in enhanced signal linearity [5]. The OPAMP achieves differential-mode (DM) DC loop-gain, PM, and UGF of 64.1 dB, 57.2 degrees, and 517 MHz, respectively, in the nominal case. Table 1 displays the summary of the OPAMP's DM AC performances over PVT variations and device mismatches.

Table 1. The OPAMP's AC Performances over PVT Variations and 1000-Run Monte-Carlo Simulation Results over Device Mismatches.

	Process Variations				
	TT	SS	FF	SF	FS
Loop Gain at DC [dB]	64.1	68	61.3	64.9	63.4
Phase Margin [deg.]	57.2	57.2	57.9	55.1	59.3
Unity-Gain Frequency [MHz]	517	468	568	530	501
	Temperature Variations [°C]				
	−40	27		125	
Loop Gain at DC [dB]	67.4	64.1		59.5	
Phase Margin [deg.]	54.3	57.2		60.1	
Unity-Gain Frequency [MHz]	622	517		395	
	Supply Voltage Variations [V]				
	1.62		1.8		1.98
Loop Gain at DC [dB]	62.4		64.1		65.2
Phase Margin [deg.]	57.6		57.2		55.9
Unity-Gain Frequency [MHz]	457		517		562
	1000-Run Monte-Carlo Mismatch Simulation				
	Mean		Standard Deviation		
Loop Gain at DC [dB]	64.1		0.808		
Phase Margin [deg.]	57.3		1.13		
Unity-Gain Frequency [MHz]	516		16.0		

3. Adaptive Amplitude Tuning for Load Impedance Variations

3.1. Effect of Load Impedance Variations on the Line Driver's Performances

The OPAMP's output stage and the current replica cells should ideally have equal input (V_{gs}) and output (V_{ds}) voltages to guarantee an accurate mirroring ratio N for the signal currents and the enhanced signal linearity [8]. However, the equivalent load impedance (R_L) in Figure 3 is vulnerable to process, temperature, the number of turned-on receivers, the input impedance of the receivers, and line lengths [1]. Figure 5 describes the small-signal model of the current replica cells and the bus lines including those variations. ΔR_1 , ΔR_2 , and ΔR_3 represent the variations in R_{MATCH} and each R_{TERM} , respectively. The equivalent load variations generate different drain voltages between V_{LOOP} and V_{OUT} since the sizes of the signal currents replicated to the replica cells are defined by the feedback resistor R_{FB} in the unity-gain closed-loop OPAMP block. Therefore, the variations result in a degraded linearity and non-unity closed-loop voltage gain.

Another conventional LD technique [8] is shown in Figure 6b. A differential transconductance stage drives the differential class-AB output stage with slave current mirrors $M_{1,4,5,8,9,13,12,16}$. The LD's signal linearity is enhanced with cascode MOSFETs $M_{2-3,6-7,10-11,14-15}$ and auxiliary operational transconductance amplifiers OTA_{1-4} by effectively shielding the slave current mirrors' drain nodes [8]. Although the techniques can further improve the signal linearity by boosting the LD's output resistances, the cascode MOSFETs limit the LD's maximum output voltage level. In addition, the linearity enhancement techniques increase the quiescent current consumption due to the auxiliary amplifiers and the cascode stage's extra bias circuit branches.

3.3. Proposed Signal Linearity Enhancement and Signal Gain Control Technique

The two major problems of the conventional LD's linearity enhancement and signal gain control techniques are output voltage range limitation and extra quiescent power consumption. A digital-based adaptive amplitude tuning (AAT) technique is proposed to guarantee robust signal linearity and closed-loop gain variations against the load variations without limiting the LD's maximum output voltage level and without adding extra quiescent current consumption. Figure 7 displays the connection between the OPAMP's cascode stage, the OPAMP's output stage, and current replica cells. The replica cells consist of two different class-AB current source/sink stages. $M_{P(N)ORV}$ represents a variable-size stage while $M_{P(N)OR}$ is a fixed-size stage. The number of turned-on variable replica cells is denoted as N in Figure 5. The closed-loop voltage gain can be controlled by controlling the sizes of the variable replica cells M_{PORV} and M_{NORV} . When the load impedance increases ($=\Delta R_{2,3}$ is positive), then the output voltage increases without the AAT function since the loop current (I_{LOOP}) (in Figure 3) stays unchanged. However, the AAT turns off some of the variable current replica cells ($=$ decrease N) to deliver a reduced I_{LOOP} to the bus lines. When the load impedance decreases ($=\Delta R_{2,3}$ is negative), the N increases, and vice versa, to sustain the unity gain ($A_V = -1$) as in Equation (2):

$$A_V = -\frac{N}{2R_{FB}} [r_o || (R_{MATCH} + \Delta R_1) || (R_{TERM} + \Delta R_2) || (R_{TERM} + \Delta R_3)] \quad (2)$$

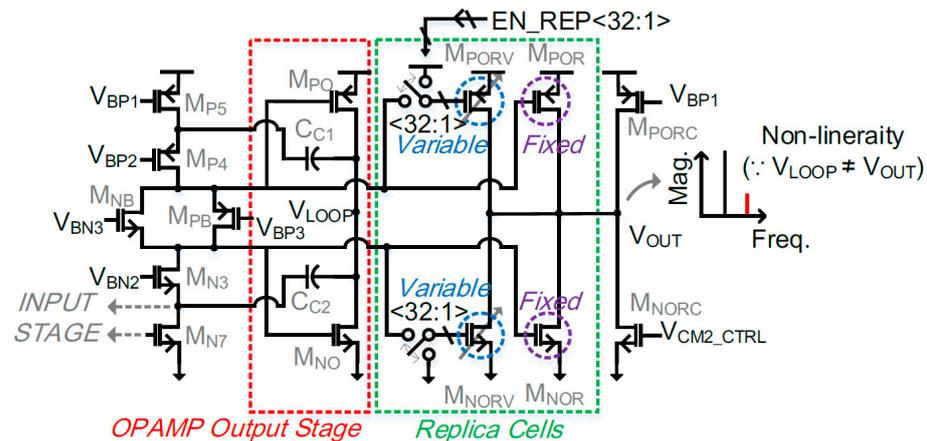


Figure 7. Schematic of the OPAMP's output stage and current replica cell.

The replica cells' output impedance r_o is approximately a few mega-ohms, which is comparably negligible in Equation (2). The unity-gain property not only mitigates the close-loop gain variations, but also alleviates signal linearity variations since the proposed AAT keeps the output voltages V_{LOOP} and V_{OUT} the same. In addition, the current replica cells prevent the OPAMP's stability, bandwidth and loop-gain variations against the R_L variations since the current replica cells act as buffers between the OPAMP and the bus lines. The 32-bit thermometer digital code EN_REP controls the number of turned-on variable replica cells. In this design, the number of gate fingers for $M_{P(N)O}$, $M_{P(N)ORV}$, and

$M_{P(N)OR}$ are 32, 32, and 112, respectively, with an identical unit finger MOSFET size. The mirroring ratio N is set at 4 when EN_REP is set at mid-code.

The overall block diagram of the proposed AAT is shown in Figure 8. One peak-to-peak detector determines the peak of the OPAMP loop voltage V_{PK1} with the loop voltages V_{LOOPP} and V_{LOOPN} . Another peak-to-peak detector determines the peak of the channel voltage V_{PK2} with two line output voltages V_{OUTP} and V_{OUTN} . A double-tail dynamic comparator called COMP then compares the two peaks. The differential output of the comparator passes through a set–reset (SR) latch and enables each binary datum in the thermometer-based bi-directional shift register (BDSR). Each flip-flop (FF) in the BDSR is reset with an RST signal in the beginning. A decrease in the load impedance implies $V_{PK1} < V_{PK2}$. The output of the comparator then becomes low, and the BDSR outputs (EN_REP) increase; this increases V_{PK1} and V_{OUT} . When $V_{PK1} > V_{PK2}$, the comparator’s output becomes high and EN_REP decreases. Afterward, the comparator’s output repeats low and high since V_{PK1} and V_{PK2} are crossing each other in the settled calibration region. The time-domain waveform is demonstrated in Figure 9 with a clock frequency of 5 MHz. In addition, the comparator features 6.32 mV for maximum offset voltage according to 1000-run mismatch Monte Carlo simulation. According to simulation results, the offset induces 1–2 bit errors in the BDSR output EN_REP , which results in approximately 0.7 dB THD degradation. The offset issue can be further alleviated with an offset calibration.

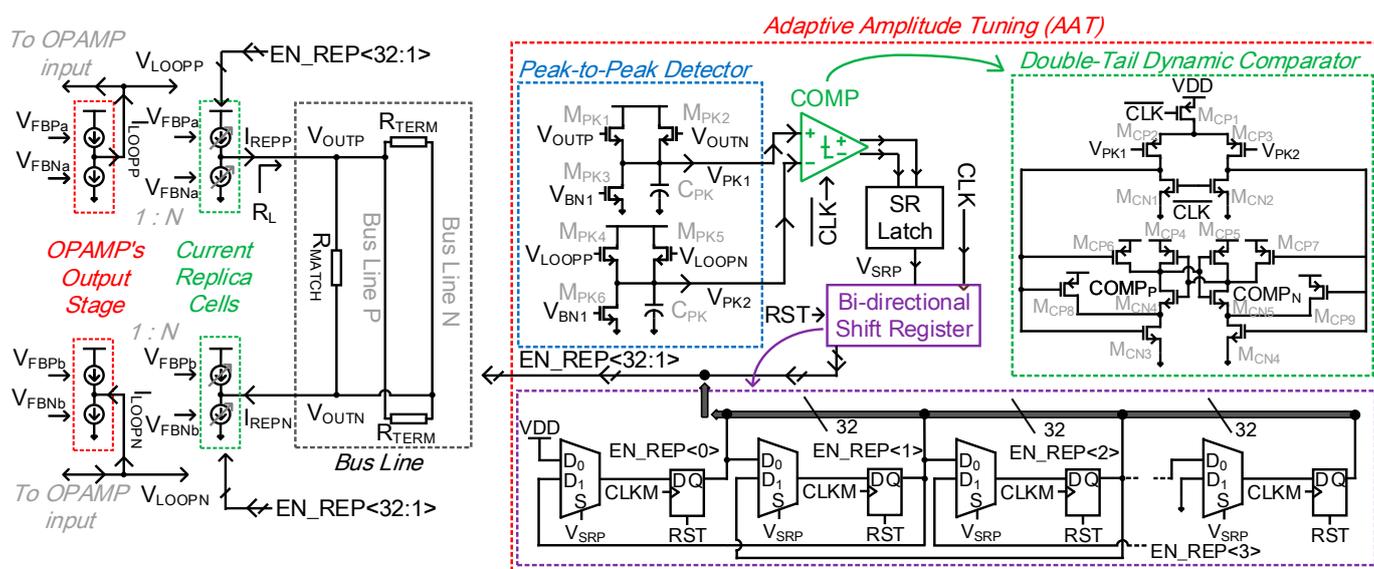


Figure 8. Block diagram of adaptive amplitude tuning with the OPAMP class-AB output stage and current replica cell with bus lines.

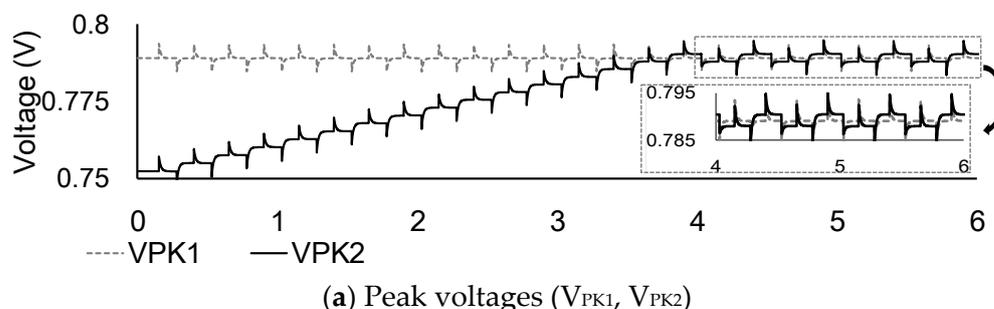


Figure 9. Cont.

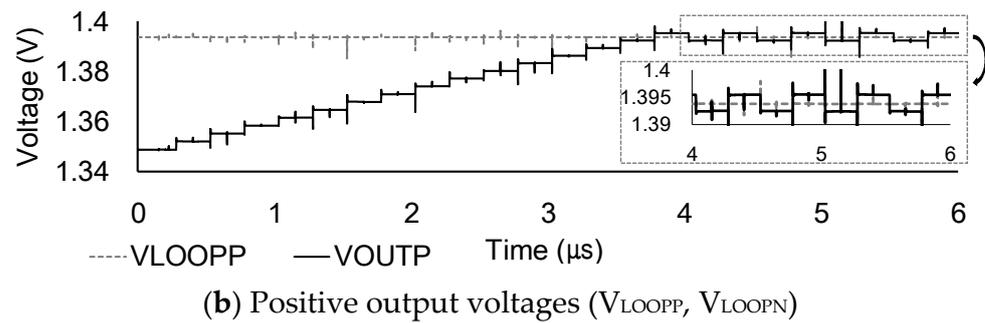
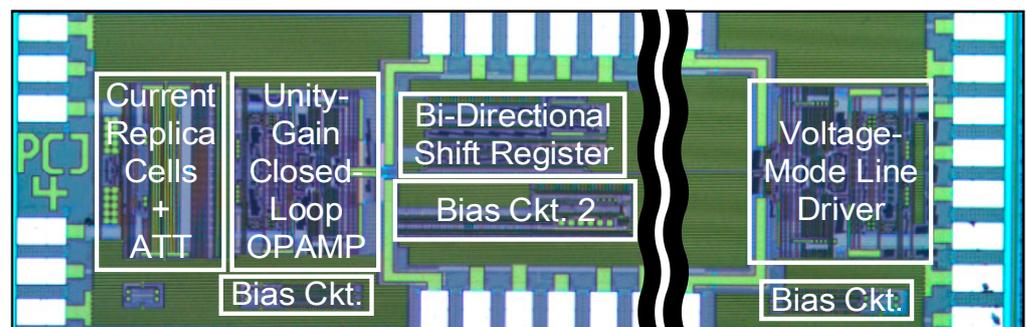


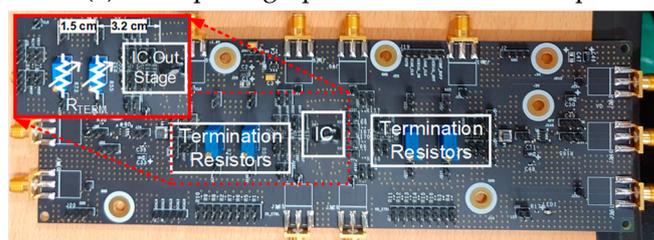
Figure 9. Simulated waveform of the proposed adaptive amplitude tuning at DC.

4. Measurement Results

The proposed hybrid of a VMLD and CMLD, and a conventional VMLD were fabricated in CMOS 180 nm to compare their performances. The microphotograph of the manufactured chip is shown in Figure 10a. The drivers are measured with a 1:1 impedance transformer to convert the differential output to single-ended for a signal analyzer [5]. A low-distortion high-speed analog buffer (OPA653) is implemented to prevent the chip's load condition from being distorted with a signal analyzer's (Keysight N9010A) 50 Ω input resistance. A vector signal generator (Agilent N5182A) generates an input signal. Figure 10b displays the manufactured printed circuit board (PCB) for testing the fabricated integrated circuits (ICs). The left and right sides of the PCB are designed to test the hybrid LD and VMLD, respectively. Each termination resistor is realized with discrete variable components (R_{TERM} in Figure 10b) to alter its value to validate how well the ATT block prevents the proposed line driver's performance from the channel load impedance variations. The channel lines are designed differentially, and they are designed to have the same line width and length on the positive and negative channels. The output stages of the proposed drivers are matched with the channel lines using series and parallel matching resistors for the VMLD and the hybrid LD, respectively.



(a) Microphotograph of the fabricated chip



(b) Picture of the PCB for measuring the fabricated IC's performance

Figure 10. Microphotograph and test board of the fabricated chip.

The VMLD is designed with the conventional topology in Figure 2. The VMLD's OPAMP architecture is the same as the one in Figure 4 for a fair comparison. The sizes of both class-AB output stages in both topologies are designed identically. Figure 11 displays

the FFT of the proposed hybrid LD, and it achieves THD+N of -49.0 dB with an input frequency of 40 MHz and the maximum allowable output swing of 2.8 V_{pp} differential. The hybrid LD achieves a competitive THD+N of -59.2 dB against the VMLD, which achieves -62.4 dB THD+N with the same supply voltage of 1.8 V, as shown in Figure 12. They are measured with the same input frequency of 40 MHz and 930 mV_{pp} differential signal swing on the bus lines, which is the maximum allowable channel swing for the VMLD. The VMLD features slightly enhanced linearity because the equivalent load (eq. R_{LOAD}) for the hybrid LD is 30 Ω while the VMLD has 60 Ω due to the series source terminations. Lower load impedance requires a better current driving capability to source a larger amount of currents. However, the VMLD suffers from the series matching signal attenuation; therefore, the hybrid LD allows enhanced signal power to be delivered to the load with the same power supply voltage. The proposed LD achieves η_{power} of 87.0% , while the VMLD achieves η_{power} of only 7.22% .

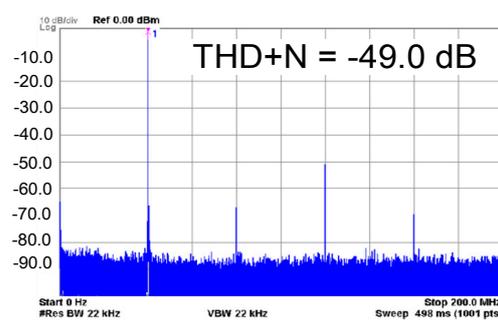


Figure 11. Measured FFT and THD+N of the proposed hybrid line driver at $F_{IN} = 40$ MHz and output swing of 2.8 V_{PP} differential.

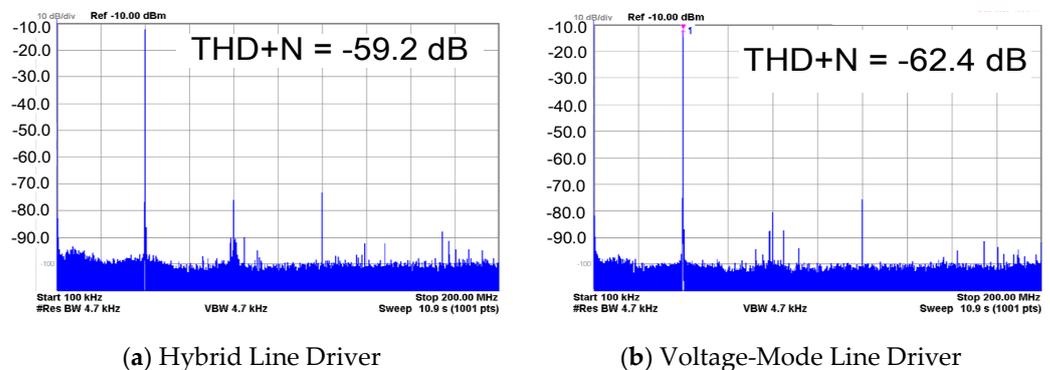


Figure 12. Measured THD+N of the proposed hybrid line driver, and the conventional voltage-mode line driver at $F_{IN} = 40$ MHz and 930 mV_{PP} differential of signal swing on the bus lines.

Figure 13a describes the measured closed-loop voltage gain against the equivalent load impedance variations according to both simulation and measurement results. The load impedance variations change the closed-loop gain since the feedback resistors define the proposed hybrid LD's output signal current levels. Without the ATT, the closed-loop gain varies from -1.87 dB to 1.21 dB. On the other hand, the calibration allows reduced closed-loop gain variations, which range from -0.38 dB to 0.05 dB. The calibration logic also prevents the driver's linearity variations against the load variations, as shown in Figure 13b. The THD+N varies from -37.2 dB to -49.2 dB without the AAT. However, the AAT mitigates the THD+N variations from -45.2 dB to -49.0 dB by adjusting the variable replica cells in a range of 80 – 160 Ω load impedance variations. The AAT consumes 12.6 μ W at $F_{CLK} = 5$ MHz, which is almost negligible compared to the hybrid LD's power consumption. This dynamic power can be further reduced by decreasing the clock frequency since the AAT does not have to operate quickly, depending on the required maximum calibration time.

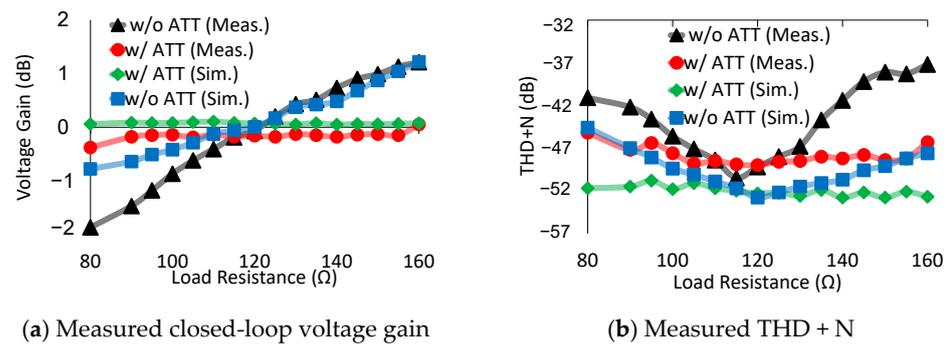


Figure 13. Simulated and measured closed-loop voltage gain (A_V) and THD + N of the hybrid line driver against load resistance variations at $F_{IN} = 40\text{MHz}$ and output swing of $2.8 V_{PP}$ differential.

Table 2 compares the proposed LD with the prior arts. The comparison table is filled with the prior arts that are tested with similar megahertz bandwidth levels and resistive load conditions to keep the fairness against the signal bandwidth and the load condition. The proposed hybrid LD features the best η_{power} , which stands for a ratio between the signal power delivered to the load (P_L) compared to the consumed quiescent power (P_Q). This is because the current mode prevents signal attenuation with the parallel termination impedance matching. The proposed hybrid LD and VMLD consume 37.6 mW and 25.2 mW while delivering P_L of 32.7 mW and 1.82 mW , respectively. A figure of merit (FoM) from reference [14] is used to evaluate the line drivers' performances as follows in Equation (3):

$$\text{FoM} = \frac{P_L}{P_Q \times (\text{THD} + \text{N}[\%])} \quad (3)$$

Table 2. Proposed Line Driver's Performance Comparison with Prior Art.

	This Work (Hybrid LD)	This Work (VMLD)	[1]	[7]	[9]	[10]
Process	180 nm	180 nm	500 nm	180 nm	350 nm	180 nm
Supply [V]	1.8	1.8	± 1.65	2.5	3.3	1.8
$V_{OUT} [V_{PP,rms}]$	0.99	0.33	0.85	1.06	1.41	1.24
Eq. $R_{LOAD} [\Omega]$	30	60	75	75	75	100
P_Q [mW]	37.6	25.2	26.4	130	155	38.6
Driving Mode ¹	I+V	V	I	V	I	I
P_L [mW]	32.7	1.82	19.2	15.6	26.6	30.6
η_{power} [%]	87.0	7.22	36.5	12	17.2	39.8
THD+N [dB]	-49.0	-62.4	-42	-51.2	-42	-48
THD+N [%]	0.55	0.0759	0.794	0.275	0.794	0.398
F_{IN} [MHz]	40	40	5	10	30	100
Area [mm^2]	0.377	0.133	0.22	0.094	0.210	0.48
FoM	1.58	0.95	0.46	0.42	0.22	1.00

¹ I: current-mode LD, V: voltage-mode LD, I + V: hybrid of voltage- and current-mode LD.

The FoM features the power efficiency and signal linearity of the line driver. The hybrid LD in this work achieves an FoM of 1.58, which is the best FoM among the table. The VMLD features a lower FoM of 0.95. The proposed hybrid LD allows a wide output swing on the output channels, and features the best η_{power} . The comparably large area consumption is one of the noticeable weaknesses of the proposed hybrid line driver. Fortunately, this issue can be alleviated by using more recent short-channel technologies. This is because the AAT logic is digital, whose area decreases as the technology shrinks, while the previous analog mechanisms typically do not.

5. Discussion and Conclusions

In this paper, a hybrid of a voltage-mode and a current-mode line driver with adaptive amplitude tuning for a turbo controller area network is presented. The hybrid line driver consists of a unity-gain closed-loop OPAMP and class-AB current replica cells. The proposed line driver prevents the signals from impedance matching attenuation by

implementing parallel source termination. In addition, the adaptive amplitude tuning controls the sizes of the current replica cells to alleviate closed-loop voltage gain and signal distortion variations against the load impedance variations. The proposed tuning mechanism does not cause any extra quiescent current consumption but rather a small amount of dynamic power, and it also does not degrade the maximum allowable output voltage range, which are major problems on conventional signal linearity enhancement and voltage gain control techniques. The proposed hybrid driver is manufactured in CMOS 180 nm, and it achieves -49.0 dB THD+N at an input frequency of 40 MHz and 0.99 peak-to-peak rms output voltage with 32.7 mW power consumption from 1.8 V supply voltage. The conventional voltage-mode driver is also manufactured with the same technology, and it features -62.4 dB THD+N at the same input frequency and 1/3 attenuated output rms voltage range with 25.2 mW power consumption from the same 1.8 V supply voltage. In the manner of signal linearity, power consumption, output signal swing, and the resistive load condition, the proposed hybrid driver achieves 1.58 figure-of-merit (FoM) while the conventional voltage-mode driver and the best FoM among prior arts are 0.95 and 0.46, respectively.

Author Contributions: Conceptualization, C.P.; methodology, C.P.; software, C.P.; validation, C.P.; formal analysis, C.P.; investigation, C.P.; resources, C.P.; data curation, C.P.; writing—original draft preparation, C.P.; writing—review and editing, C.P.; visualization, C.P.; supervision, M.L.; project administration, M.L.; funding acquisition, M.L. All authors have read and agreed to the published version of the manuscript.

Funding: This work was supported in part by the Institute of Information & Communications Technology Planning & Evaluation (IITP) grant funded by the Korea government (MSIT) [No. 2019-0-01348, High-speed, high-reliability, and intelligent IVN (In-Vehicle Network) semi-conductor development]. The EDA tool was supported by the IC Design Education Center (IDEC), Korea.

Conflicts of Interest: The authors declare no conflict of interest.

References

1. Ramachandran, N.; Dinc, H.; Karsilayan, A. A 3.3-V CMOS adaptive analog video line driver with low distortion performance. *IEEE J. Solid-State Circuits* **2003**, *38*, 1051–1058. [[CrossRef](#)]
2. Babanezhad, J.N. A 100-MHz, 50- Ω , -45 -dB distortion, 3.3-V CMOS line driver for Ethernet and fast Ethernet net-working applications. *IEEE J. Solid-State Circuits* **1999**, *34*, 1044–1050. [[CrossRef](#)]
3. Ara, B.; Kim, C.-S.; Lee, S.-S. A CMOS line driver for ADSL central office applications. *IEEE J. Solid-State Circuits* **2003**, *38*, 2201–2208.
4. Liu, P.-K.; Hung, S.-Y.; Liu, C.-Y.; Hsieh, M.-H.; Chen, C.C.-P. A 52 dBc MTPR line driver for powerline communication HomePlug AV standard in 0.18- μ m CMOS technology. In Proceedings of the 2013 IEEE International Symposium on Circuits and Systems (ISCAS2013), Beijing, China, 19–23 May 2013; pp. 1404–1407. [[CrossRef](#)]
5. Zhu, Z.; Wang, J. A Compact High-Performance Programmable-Gain Analog Front End for HomePlug AV2 Communication in 0.18 μ m CMOS. *IEEE Trans. Circuits Syst. I Regul. Pap.* **2017**, *64*, 1–13. [[CrossRef](#)]
6. Johns, D.; Essig, D. Integrated circuits for data transmission over twisted-pair channels. *IEEE J. Solid-State Circuits* **1997**, *32*, 398–406. [[CrossRef](#)]
7. Hadidi, K.; Oshima, H.; Sasaki, M.; Matsumoto, T. A highly linear fully differential low power CMOS line driver. In Proceedings of the ESSCIRC 2004—29th European Solid-State Circuits Conference (IEEE Cat. No.03EX705), Estoril, Portugal, 16–18 September 2004; pp. 541–544. [[CrossRef](#)]
8. Pan, H.; Yao, Y.; Hammad, M.; Tan, J.; Abdelhalim, K.; Wang, E.W.; Hsu, R.C.J.; Tam, D.; Fujimori, I. A Full-Duplex Line Driver for Gigabit Ethernet with Rail-to-Rail Class-AB Output Stage in 28 nm CMOS. *IEEE J. Solid-State Circuits* **2014**, *49*, 3141–3155. [[CrossRef](#)]
9. Mahadevan, R.; Johns, D. A differential 160-MHz self-terminating adaptive CMOS line driver. *IEEE J. Solid-State Circuits* **2000**, *35*, 1889–1894. [[CrossRef](#)]
10. Sung, G.-M.; Chou, W.-D.; Yu, C.-P. A 10-bit 1.8 V 45 mW 100 MHz CMOS transmitter chip for use in an XDSL modem in a home network. *Analog. Integr. Circuits Signal Process.* **2014**, *81*, 515–527. [[CrossRef](#)]
11. Kang, S.; Han, S.; Cho, S.; Jang, D.; Choi, H.; Choi, J.-W. High speed CAN transmission scheme supporting data rate of over 100 Mb/s. *IEEE Commun. Mag.* **2016**, *54*, 128–135. [[CrossRef](#)]

12. Rida, S.A.; Silva-Martinez, J. The recycling folded cascode: A general enhancement of the folded cascode amplifier. *IEEE J. Solid-State Circuits* **2009**, *44*, 2535–2542.
13. Dasgupta, U. Low voltage 2-stage and 3-stage push-pull output amplifiers in 65-nm CMOS technology. In Proceedings of the 2016 International Symposium on Integrated Circuits (ISIC), Singapore, 12–14 December 2016; pp. 1–4. [[CrossRef](#)]
14. Nandish, M.; Huijsing, J.H.; Stojanović, V. A 1-mW Class-AB Amplifier With –101 dB THD+N for High-Fidelity 16 Ω Headphones in 65-nm CMOS. *IEEE J. Solid-State Circuits* **2019**, *54*, 948–958.