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A 56–161 GHz Common-Emitter Amplifier with 16.5 dB Gain Based on InP DHBT Process

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Abstract: This paper presents a broadband amplifier MMIC based on 0.5 μm InP double-heterojunction bipolar transistor (DHBT) technology. The proposed common-emitter amplifier contains five stages, and bias circuits are used in the matching network to obtain stable high gain in a broadband range. The measurement results demonstrate a peak gain of 19.5 dB at 146 GHz and a 3 dB bandwidth of 56–161 GHz (relative bandwidth of 96.8%). The saturation output power achieves 5.9 and 6.5 dBm at 94 and 140 GHz, respectively. The 1 dB compression output power is -4.7 dBm with an input power of -23 dBm at 94 GHz. The proposed amplifier has a compact chip size of $1.2 \times 0.7 \text{ mm}^2$, including DC and RF pads.

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1. Introduction

Broadband amplifiers play an important role in high-resolution radar systems, high-data-rate communication systems, and measuring instruments. With the advancement of technology, the requirements for system performance and frequency are increasing in number, and the demand for broadband amplifiers is also increasing.

The traveling wave amplifier is common in broadband amplifier design, and is also known as a distributed amplifier (DA) [1–6]. The bandwidth, flatness, and output power of DAs are outstanding among broadband amplifiers. The main limitation of DAs is that their maximum gain does not exceed the transistor, which limits their high-frequency applications because the transistor gain is inversely proportional to the operating frequency. The cascode structure is another commonly used topology for designing broadband amplifiers, and it is often used as a basic unit to form a DA to increase its gain [3]. Because of the narrow-band characteristics of the matching network, the common-emitter (CE) structure is considered unsuitable for broadband amplifier design [7–9].

This paper presents a five-stage wideband common-emitter amplifier that incorporates the bias circuit into the matching network and finally obtains a maximum gain of 19.5 dB at 146 GHz with a 3 dB bandwidth of 56–161 GHz. To the best of the authors' knowledge, the proposed common-emitter amplifier has the highest relative bandwidth (RB) in this frequency band based on the 0.5 μm InP DHBT process.

2. InP DHBT Technology

The amplifier was fabricated using a 0.5 μm InP DHBT process. The emitter contact is 500 nm wide and 5 μm long, and the base contacts are 300 nm wide at both sides of the

emitter. An InGaAsP composite collector was used to eliminate the current blocking effect caused by the B-C heterojunction conduction band spike [10]. The composite collector area consists of an InGaAs setback layer, a step-graded InGaAsP layer, and a δ -doping layer; all of the layer structures are listed in [11,12]. The f_t/f_{max} values of the transistor are 350 and 535 GHz, respectively, as shown in Figure 1. Current gain (H_{21}), maximum available power gain (MAG), and maximum stable power gain (MSG) can be obtained by Formulas (1)–(5), where k is the stability factor. The process provides three wiring metal layers and compact interconnect vias between them. Metal-Insulator-Metal (MIM) capacitors with $0.26 \text{ fF}/\mu\text{m}^2$ capacitance density and $25 \Omega/\text{square}$ TaN TFR are also available [13,14].

$$H_{21} = \frac{Y_{21}}{Y_{11}} = \frac{-2S_{21}}{(1 - S_{11})(1 + S_{22}) + S_{12}S_{21}} \quad (1)$$

$$\text{MAG} = \frac{|S_{21}|}{|S_{12}|} \left(k - \sqrt{k^2 - 1} \right) \quad k > 1 \quad (2)$$

$$\text{MSG} = \frac{|S_{21}|}{|S_{12}|} \quad k < 1 \quad (3)$$

$$k = \frac{1 - |S_{11}|^2 - |S_{22}|^2 + |S_{11}S_{22} - S_{12}S_{21}|^2}{2|S_{12}S_{21}|} \quad (4)$$

$$U = \frac{|z_{12} - z_{21}|^2}{4(\text{Re}(z_{11}) \cdot \text{Re}(z_{22}) - \text{Re}(z_{12}) \cdot \text{Re}(z_{21}))} \quad (5)$$

Figure 1. The extracted f_t/f_{max} of the $0.5 \times 5 \mu\text{m}^2$ device.

Figure 2 shows a cross-section of the back end of the $0.5 \mu\text{m}$ InP DHBT MMIC process used in this paper. This process includes thin-film resistors (TFR), MIM capacitors, and three layers of interconnected metal (M1-M3). A benzocyclobutene (BCB) spin-on dielectric is used as the interlayer dielectric (ILD) with $2 \mu\text{m}$ (M1-M2) and $3 \mu\text{m}$ (M2-M3) ILD

spacing between the metal layer. Electroplated Au-based interconnects are used for the metallization layers, where M1 has a thickness of 1 μm , and M2 and M3 have a thickness of 2 μm . In this design, thin-film micro-strip lines (TFMLs) can be realized with M1 as the ground and M3 as the signal line [14].

Figure 2. Cross-sectional view of the 0.5 μm indium phosphide double-heterojunction bipolar transistor (InP DHBT) technology.

2.1. Parasitic Substrate Mode Suppression

In a multi-layer integrated circuit, thin-film microstrip lines (TFMLs) are usually used to transmit signals [15]. To achieve integration with an active circuit, a bulk substrate needs to be added under the TFML. This structure requires interlayer interconnection and, therefore, a defective structure on M1, such as a connection to transistors below the ground plane, thin-film resistors (TFRs), and series capacitors. In addition, a typical RF pad uses a coplanar ground–signal–ground (GSG) layout with ground slots. All of these ground plane fenestrations may excite the bulk substrate parasitic modes.

To eliminate the parasitic modes, it is feasible to set a number of metallized backside-vias or insert a dielectric insertion layer above the bulk substrate [16]. However, the backside via occupies a large amount of the chip area and reduces integration. The method of inserting a substrate insertion layer has a limited suppression effect on the parasitic mode, and the realization of the process is difficult.

To study the resonance phenomena caused by the parasitic modes, the HFSS model is established by taking the series capacitor as an example, as shown in Figure 3. In this model, the size of the substrate InP is $1.06 \times 1 \times 0.1 \text{ mm}^3$ ($l \times w \times h$), and the size of the capacitance is $55 \times 55 \mu\text{m}^2$, and the window size is $60 \times 60 \mu\text{m}^2$; all conductors are made of gold.

Mode indices of the main resonances are shown in Figure 3a. The insertion loss increases as frequency increases; simultaneously, several resonant frequencies are observed in the figure, indicating that energy is coupled into the substrate through the opening window in the ground plane. The parasitic modes bounce at the edge of the substrate due to the limited substrate volume and create resonance at certain frequencies. The resonant frequency can be approximated as:

$$f_{mnp} = \frac{c}{2\sqrt{\epsilon_r}} \sqrt{\left(\frac{m}{l}\right)^2 + \left(\frac{n}{w}\right)^2 + \left(\frac{p}{h}\right)^2} \quad (6)$$

where l , w , and h are the length, width, and height of the dielectric substrate, respectively, and m , n , and p are resonance mode indices, which are equivalent to the half-wavelength number of the corresponding dimension. The magnitude of the electric field in the InP substrate is shown in Figure 3b, where the resonant frequency is 180 GHz. It can be clearly seen that the electric field maximum distribution is equal to the mode indices

$(m, n, p) = (3, 3, 0)$, which is in agreement with $f_{3,3,0}$ in Equation (6). Because the thickness of the chip is only 100 μm , there is no vertical resonance below 424 GHz ($m, n, p = 0, 0, 1$); that is, $p = 0$ below 424 GHz.

Figure 3. Simulation S-parameters of a series capacitor with an opening window in the ground plane. (a) S-parameters of a series capacitor with an opening window in the ground plane; (b) magnitude plot of the electric field in the InP substrate observed at $f_{3,3,0} = 180$ GHz.

Because the electromagnetic waves leaking into the InP dielectric substrate need to form a stable standing wave and then resonate, the addition of backside vias can prevent the generation of standing waves and eliminate resonance. Figure 4 shows a two-backside via capacitor photo and its simulation and measurement results. This backside via arrangement with the purpose of breaking standing waves can eliminate the resonance generated by the parasitic mode, and this achievement is applied to the design of the proposed amplifier.

Figure 4. (a) Capacitance photo, equivalent circuit model, and (b) S-parameters.

2.2. Equivalent Circuit Model of Capacitor

In addition to building the HFSS capacitor model, we also establish an equivalent circuit model of the capacitor to achieve accurate matching network analysis. Figure 4 shows the equivalent circuit model of the series capacitor model and its simulation results based on measurement results. This model adds two parallel capacitors C_p on the basis of the LCL model to be equivalent to the grounding capacitance caused by defects. As the defect gap spacing is constant, the parallel capacitance values in the equivalent circuit are equal. The simulation results show that the MIM capacitor density is $0.26 \text{ fF}/\mu\text{m}^2$.

The comparison of S-parameters in Figure 4b shows that the equivalent circuit is consistent with the measured results, which is beneficial to the design of the matching circuit.

2.3. Equivalent Circuit Model of Transistor

The equivalent circuit model is the base of the transistor. As the frequency increases, the parasitic parameters have a significant impact on the device. Due to the use of devices of different sizes under the same process, we use the method of 3D simulation to extract parasitic parameters described in [17]. The equivalent circuit is shown in Figure 5.

Figure 5. Small-signal equivalent-circuit model of (a) InP DHBT and (b) the internal device [17].

Figure 5a shows the small-signal equivalent-circuit model of the device. Nine parameters are used to ensure equivalence to the inter-electrode impedance effect. The inductors and resistances of electrode contacts and posts are represented by L_{bxi} , L_{cxi} , and L_{exi} , and R_{bxi} , R_{cxi} , and R_{exi} , respectively. Figure 5b shows the simplified Agilent HBT model, which is used for the internal device equivalent circuit. The extraction method of each parameter is described in detail in [18]. Parameters biased under $V_c = 1.5 \text{ V}$ and $I_b = 200 \mu\text{A}$ are extracted according to the above method and are listed in Table 1. A comparison between the model and the measured results is shown in Figure 6. The large-signal model is carried out completely in accordance with the steps in [18]; the description is not repeated here.

Table 1. Small-signal equivalent circuit elements.

R_{bi} (Ω)	R_e (Ω)	R_c (Ω)	R_{be} (Ω)	C_{bc} (fF)	R_{bc} (k Ω)	G_{m0} (mS)	τ (pS)	C_{be} (fF)
42	3	42.7	67	2.4	34.4	652	0.7	512
C_{bexi} (fF)	C_{cexi} (fF)	C_{bcxi} (fF)	L_{exi} (pH)	L_{bxi} (pH)	L_{cxi} (pH)	R_{exi} (Ω)	R_{bxi} (Ω)	R_{cxi} (Ω)
4.5	24.2	15.5	10.5	9.5	11.1	0.87	1.35	0.78

Figure 6. Measured and simulated S-parameters of $0.5 \times 5 \mu\text{m}$ InP DHBT: (a) real S11 and its image; (b) real S12 and its image; (c) real S21 and its image; (d) real S22 and its image.

3. Amplifier Design

Figure 7 shows the schematic diagram of the proposed amplifier. The amplifier adopts a five-stage cascaded CE topology, and the values of bias voltage, series resistance, and parallel capacitance of all bases are uniform; this also applies to collectors with different values. Generally, the length of the DC bias line is constant, usually $\lambda/4$ at operating frequency, and forms an open-circuit converter with the parallel capacitor. In this case, the bias circuit can be ignored in the design of the matching network. However, the electrical length of the transmission line is inversely proportional to the operating frequency; therefore, this quarter-wavelength bias circuit is only suitable for narrow-band amplifier designs.

The DC bias circuit is incorporated into the matching network in this design. All bias lines have the same width, and their length is adjusted according to matching requirements.

Table 2 shows the input/output impedance and output power of each transistor derived from source-pull and load-pull simulation when the Q1 input power is -7 dBm at 140 GHz. The input power of the latter stage is the output power of the previous stage. For example, the input power of Q2, -1.39 dBm, is the output power of Q1.

Figure 7. Schematic diagram of the amplifier. The characteristic impedance and electrical length of the bias line are calculated at 140 GHz.

Table 2. Input/output impedance and output power of transistors.

	Q1	Q2	Q3	Q4	Q5
Z_s (Ω)	$18.7 + j14.3$	$21.4 + j10.4$	$21.3 + j4.7$	$20.5 + j0.6$	$20.2 + j0.3$
Z_l (Ω)	$21.1 + j32.3$	$33.4 + j29.7$	$33.9 + j30.1$	$33.6 + j30.0$	$33.6 + j30.0$
P_{out} (dBm)	−1.39	3.65	6.38	7.07	7.2

Figure 8 compares the effect of different bias lines' lengths on circuit performance. In Figure 8a, the input impedance $Z_0 = 50 \Omega$ is the characteristic impedance of the transmission line, and the output impedance Z_{s1} is $18.7 - j14.3$, which is the conjugate Z_s of Q1. It is clear that, although a bias circuit with a $\lambda/4$ bias line (red dotted line) is theoretically equivalent to an open circuit, it is still different from a true open circuit (green dashed line). As shown in Figure 8a, the bias line we used reduces the insertion loss of the matching network above 80 GHz. The slope of the inflection point and its vicinity in Figure 8a is carefully designed, and Figure 8b shows a comparison of the maximum gain of Q1 under the matching network with different bias line lengths. It can be clearly observed that the gain is flat in the 70–95 GHz range, and this is only the boost effect of the input matching network.

Adjusting the length of the bias line between Q1 and Q2, and Q2 and Q3, can reduce the loss of the matching network, thereby increasing the gain of the transistor that follows it, as shown in Figure 8c,d. The matching network between Q3 and Q4 can make the gain of Q4 stay flat above 100 GHz, as shown in Figure 8e. Because Q2 and Q3 are used to increase the gain, which affects the gain flatness of the amplifier, Q5 needs to be supplemented to balance the high gain at the 120 GHz range, as shown in Figure 8f. After the matching networks are individually designed, they are fine-tuned again in the complete circuit to obtain the best performance. Under the combined effect of multiple matching networks, the amplifier maintains a constant gain in the broadband range, as shown in Figure 9. The chip size is $1.2 \times 0.7 \text{ mm}^2$, including DC and RF pads, as shown in Figure 10.

Figure 8. Comparison of matching network insertion loss and transistor gain under different bias lines. (a) Input matching network insertion loss; (b) Q1 gain; (c) Q2 gain; (d) Q3 gain; (e) Q4 gain; (f) Q5 gain.

Figure 9. Simulation S-parameters of the amplifier.

Figure 10. Chip photograph of the amplifier MMIC. Size: $1.2 \times 0.7 \text{ mm}^2$.

4. On-Wafer Measurement Results

The on-wafer measurements were performed using a Keysight PNA-X N5247B network analyzer with Keysight N5293AX01 (0~110 GHz) frequency extenders (Keysight Technologies, Santa Rosa, CA, USA) and a Rohde & Schwarz ZVA50 network analyzer with Rohde & Schwarz ZC170 (110~170 GHz) frequency extenders (Rohde & Schwarz, Munich, Germany). The measurement results are shown in Figure 11.

Figure 11. Comparison of measured and simulated results. The biases for all tests are $V_C = 1.5$ V and $V_B = 0.9$ V. (a) Small-signal S-parameter; (b) large-signal output power and gain at 94 GHz; (c) large-signal output power and gain at 140 GHz.

The measured S-parameter results displayed in Figure 11a show that the maximum gain of the amplifier is 19.5 dB at 146 GHz, and the 3 dB bandwidth is 56~161 GHz (relative bandwidth of 96.8%). The reflection parameter S_{11} is below -5 dB in the range of 62~160 GHz, and S_{22} is below -5 dB in the range of 45~170 GHz. The amplifier provides saturation output power of 6.5 and 5.9 dBm at 94 and 140 GHz, respectively, as shown in Figure 11b,c. The 1 dB compression output power of the PA is -4.7 dBm at 94 GHz when the input power is -23 dBm. The amplifier starts to gain compression at a low input power; thus, it is more suitable for driving stages. The DC power consumption is 33.3 mW.

Table 3 shows the performance comparison of several InP HBT amplifiers. It is clear that the CE amplifier has a higher gain, while the DA bandwidth is wider. The proposed amplifier has excellent bandwidth performance compared with that of other CE cascaded amplifiers, because the DC bias circuit is incorporated into the matching network, and the bandwidth of the amplifier can be expanded by adjusting the length of the bias lines. Due to the cascaded topology, the proposed amplifier has a higher gain than that of DAs. Each transistor in this amplifier provides the highest gain and output power with minimal DC power consumption. This design has the advantages of the high gain of CE amplifiers and the wide bandwidth of DAs, but the output power is low due to the lack of power synthesis.

Table 3. Comparison of broadband amplifiers based on the InP HBT process.

Ref.	Freq. (GHz)	RB (%)	Technology (ft/ f_{max} GHz)	Gain (dB)	Topology /Devices/Stages	P_{DC} (mW)	P_{sat} (dBm)	Chip-Size (mm ²)
[3]	40–222	138.9	250 nm InP HBT (375/650)	10	DA $\times$ 2 $\times$ 4	105	8.5	0.5×0.6
[4]	40–185	128.9	500 nm InP DHBT (350/400)	10	DA $\times$ 2 $\times$ 5	96	10	0.8×0.75
[5]	DC–170	200	500 nm InP DHBT (360/490)	12	DA $\times$ 3 $\times$ 5	180	10	1.5×0.65
[6]	DC–110	200	500 nm InP DHBT (400/400)	13	DA $\times$ 2 $\times$ 5	129	11.5	1.7×0.8
[8]	55–135	84.2	250 nm InP HBT (350/600)	27.3	CE $\times$ 2 $\times$ 4	1420	21.4	1.86×0.64
[9]	115–150	26.4	250 nm InP HBT (350/600)	29.5	CE $\times$ 2 $\times$ 5	1540	21.8	1.78×0.42
This work	56–161	96.8	500 nm InP DHBT (350/535)	19.5	CE $\times$ 5	33.3	5.9	1.2×0.7

5. Conclusions

A five-stage broadband common-emitter amplifier is presented based on 0.5 μm InP DHBT technology. The measurement results show that the PA provides a maximum gain of 19.5 dB at 146 GHz with a 3 dB bandwidth of 56–161 GHz; P_{sat} values are 5.9 and 6.5 dBm at 94 and 140 GHz, respectively. The proposed broadband amplifier is suitable for the driver stage of the broadband system.

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