electronics

MDPI

Article

A Novel OTA Architecture Exploiting Current Gain Stages to Boost Bandwidth and Slew-Rate

Francesco Centurelli, Riccardo Della Sala, Pietro Monsurrò *, Giuseppe Scotti and Alessandro Trifiletti

Department of Information, Electronics and Telecommunication Engineering, Sapienza University of Rome, 00184 Rome, Italy; francesco.centurelli@uniroma1.it (F.C.); riccardo.dellasala@uniroma1.it (R.D.S.); giuseppe.scotti@uniroma1.it (G.S.); alessandro.trifiletti@uniroma1.it (A.T.)

* Correspondence: pietro.monsurro@uniroma1.it

Abstract: A novel architecture and design approach which make it possible to boost the bandwidth and slew-rate performance of operational transconductance amplifiers (OTAs) are proposed and employed to design a low-power OTA with top-of-class small-signal and large-signal figures of merit (FOMs). The proposed approach makes it possible to enhance the gain, bandwidth and slew-rate for a given power consumption and capacitive load, achieving more than an order of magnitude better performance than a comparable conventional folded cascode amplifier. Current mirrors with gain and a push–pull topology are exploited to achieve symmetrical sinking and sourcing output currents, and hence class-AB behavior. The resulting OTA was implemented using the 130 nm STMicroelectronics process, with a supply voltage of 1 V and a power consumption of only 1 µW. Simulations with a 200 pF load capacitance showed a gain of 92 dB, a unity-gain frequency of 141 kHz, and a peak slew-rate of 30 V/ms, with a phase margin of 80°, and good noise, PSRR and CMRR performance. The small-signal and large-signal current and power FOMs are the highest reported in the literature for comparable amplifiers. Extensive parametric and Monte Carlo simulations show that the OTA is robust against process, supply voltage and temperature (PVT) variations, as well as against mismatches.

Keywords: OTA; CMOS; low-power; low-voltage; analog integrated circuits

Citation: Centurelli, F.; Della Sala, R.; Monsurrò, P.; Scotti, G.; Trifiletti, A. A Novel OTA Architecture Exploiting Current Gain Stages to Boost Bandwidth and Slew-Rate. *Electronics* **2021**, *10*, 1638. https://doi.org/10.3390/electronics10141638

Academic Editors: Gianluca Traversi

Received: 8 June 2021
Accepted: 7 July 2021
Published: 9 July 2021

1. Introduction

Nowadays, society is reliant on portable and lightweight devices. Biomedical and Internet-of-Things (IoT) applications are among the most relevant topics in the research community [1–3]. A large variety of biomedical products have been proposed for monitoring people's health [4–8]. Many of these devices require lightweight building blocks able to operate with low supply voltages (LV) and low power (LP) consumption, to improve battery life in portable devices and allow the use of energy harvesting techniques [9–11].

In this scenario, one of the most useful, and challenging, building blocks is the operational transconductance amplifier (OTA) [12]. Many ideas have been proposed in the literature to develop LV-LP amplifiers with supply voltages of 1 V or less. Besides new architectures, new operating regions, notably sub-threshold and deep sub-threshold operation, have been considered. Indeed, the strong inversion region is not a good choice in energy-harvested systems, because it requires higher supply voltages than weak inversion operation, which is considered the best solution for power consumption optimization, showing good gain and appropriate bandwidth for IoT and biomedical applications [13,14].

In References [13–17], several techniques to enhance low-voltage OTA performance were analyzed. In Reference [18], Algueta Miguel et al. presented an OTA with floating gate and quasi floating-gate techniques. Moreover, OTAs with class-AB behavior were presented in [19,20], showing significant improvement in both common-mode rejection ratio (CMRR) and slew-rate performance. By reducing the supply voltages, one of the most challenging aspects of OTA design is the CMRR. Thus, in [21–23], new approaches

to attain high CMRR were advocated, considering low-voltage restrictions. Additionally, threshold lowering techniques have been investigated to obtain a significant reduction of minimum supply voltages [24–26]. Supply voltages lower than 0.6 V set stringent constraints in terms of the maximum available voltage for each transistor. At such scanty voltages, the trend is to replace tail generators, setting the current with body-biasing or gate-biasing techniques. As a result, gate-driven (GD) OTAs cannot ensure a well-defined bias point, since the body terminal has insufficient signal swing to control the biasing point. Thus, body-driven (BD) OTAs have become more popular over the years. Indeed, BD amplifiers employ the bulk as an input terminal to achieve rail-to-rail input common-mode range (ICMR) and at the same time a well-defined bias point, thanks to gate biasing [27–34]. However, BD-OTAs aren't suitable for switching applications, due to their input impedance. Furthermore, a variety of ultra low voltage (ULV) and ultra low power (ULP) inverter-based amplifiers have been proposed in the literature [35,36]. Moreover, body-driven configurations show lower bandwidth than gate-driven ones, and therefore their usage is limited to sub-kHz applications (such as brain–computer interfaces, electrocardiograms and so on) [34]. Finally, many dc-dc converters used in IoT devices, including smartwatches and earbuds, require low-drop-out regulators (LDO) [37–39] which employ OTAs with high drive capabilities and bandwidth [39]. LV-LP OTAs are often based on multiple-stage Miller compensation [39–41], and more recently on digital approaches to analog amplification [42–45].

In this paper, we present a novel architecture and design approach that enable the bandwidth, slew-rate and DC gain performance of LV-LP OTAs to be boosted. The technique is based on current mirrors with gain, which improve gain and bandwidth without creating low-frequency poles. Unlike conventional multi-stage amplifiers, the proposed architecture makes it possible to achieve multi-stage gain without the need for Miller compensation, as only low-impedance nodes are added. Furthermore, a noticeable improvement of slew-rate performance is achieved by combining the proposed technique with a complementary push–pull topology. As a result, for the same capacitive load and power consumption, the amplifier shows an approximately symmetrical class-AB behavior on both edges, improved DC gain, and higher bandwidth. The class-AB architecture is required to fully exploit the benefits of the novel technique, as it also allows boosting the peak slew-rate. Analysis of biasing, small-signal, slew-rate and noise performance were carried out, showing that the improvement can be of greater than one order of magnitude for the same load and power consumption. The technique is used in conjunction with other low-power techniques, such as class-AB and sub-threshold biasing, but is independent of them, since the performance improvement occurs for the same technology node and biasing point. As analytically demonstrated in the manuscript, by employing current mirrors with gain as intermediate stages, the proposed OTA architecture allows increasing gain, bandwidth and slew-rate by a factor that is polynomial in the current mirrors' gain and number of intermediate stages. To the authors' knowledge, no similar OTA architecture has previously been proposed in the technical literature.

An amplifier exploiting these techniques was designed in the STMicroelectronics 130 nm technology to validate the idea. The resulting amplifier is robust to process, supply voltage and temperature (PVT) variations, as well as to mismatches; it exhibits good noise performance, good power-supply rejection ratio (PSRR) and CMRR performance; and has top-of-class small-signal and large-signal figures-of-merit (FOMs) with respect to comparable amplifiers from the literature.

The paper is organized as follows: Section 2 explains the theoretical idea behind the proposed amplifier, and shows how gain, bandwidth and slew-rate performance can be improved for a given power consumption and capacitive load; Section 3 summarizes the design process of the amplifier; Section 4 summarizes the simulation results; Section 5 concludes and shows a comparison with the relevant literature.

2. Proposed Architecture and Design Approach

This section describes the theoretical idea behind the proposed OTA architecture and design approach. Small-signal, slew-rate, and noise analyses are performed to highlight the advantages of the technique.

A simplified schematic of the proposed OTA architecture is presented in Figure 1a together with a single-transistor, common-source amplifier, shown in Figure 1b. All the devices in Figure 1 are assumed to have a channel length L and a unit width W_X, with $X = N, P$ for NMOS and PMOS devices, respectively, and to be biased with a unit current I_B, set by the bias voltages V_{BX}. Unit devices are then scaled by the integer factors $K, H, S \geq 1$. The scaling factors can be implemented by placing more devices in parallel, to ensure maximum matching. With the above assumptions, the unit device has transconductance g_{mX}, input capacitance C_{GSX}, and output resistance r_{0X}. The scaling factors increase the transconductance and capacitance and lower the output resistance proportionally.

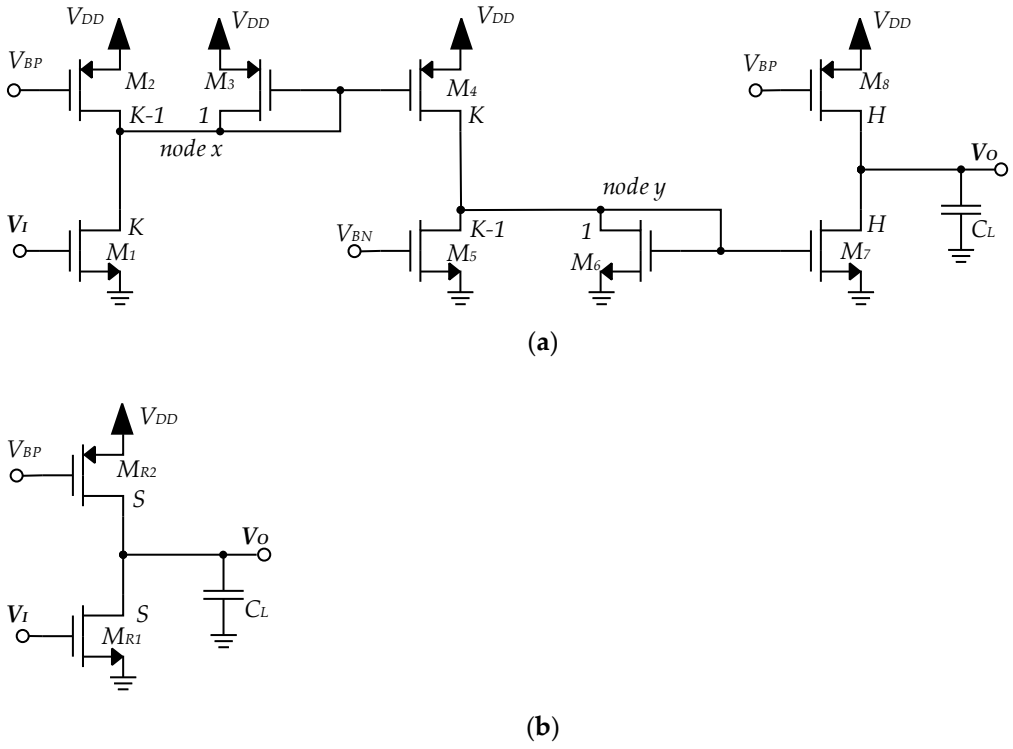

Figure 1. (**a**) Simplified topology of the amplifier, (**b**) conventional common-source amplifier.

The following analysis in this section proves that there is a clear advantage in gain, bandwidth, and slew-rate, and a moderate worsening of noise performance, for the circuit in Figure 1a with respect to the circuit in Figure 1b. This demonstrates that the use of current mirrors with gain allows excellent figures of merit to be achieved, as shown in the rest of this paper.

For the two circuits above to have the same power consumption, we set $S = 2K + H$ for the amplifier in Figure 1b. We also assume the two amplifiers to have the same load capacitance C_L. In the following, we compare these two topologies to explain how the topology in Figure 1a improves gain, bandwidth and slew-rate, with a slight penalty in noise performance. We will also show in Section 3 that this latter penalty is much lower in the actual (differential-input, push–pull output) amplifier.

2.1. Small-Signal Analysis

For the computation of DC gain, we assume that the output conductance $g_0 = r_0^{-1}$ of MOS devices is much lower than their transconductance g_m, so that the two current mirrors M_3–M_4 and M_6–M_7 in Figure 1a exhibit current gains of K and H, respectively. If

the output resistances were taken into account, the current gain would be slightly lower. However, in the actual implementation of the OTA architecture, cascode current mirrors can be used, and in this case, due to the increased output resistance ($g_m r_0^2$), the current mirrors will exhibit a current gain very close to the ideal one.

To simplify the calculations and to gain insight into circuit behavior, it is convenient to split the DC gain of the amplifier in Figure 1a as follows:

$$\frac{v_o}{v_i} = \frac{v_o}{v_y}\frac{v_y}{v_x}\frac{v_x}{v_i} \tag{1}$$

Hence, the proposed OTA can be seen as a three-stage amplifier, where the first two stages are loaded by a diode-connected MOS device. Since the diode-connected load transistors are smaller than the common-source devices which drive them, both the first and second stage exhibit a DC gain approximately equal to K. Starting from these assumptions and performing simple calculations, the expression of the DC gain of the proposed OTA in Figure 1a (*new*) is found to be:

$$A_{new} \approx \frac{K \cdot g_{mN}}{g_{mP}}\frac{K \cdot g_{mP}}{g_{mN}}\frac{H \cdot g_{mN}}{H \cdot g_{0N} + H \cdot g_{0P}} = \frac{K^2 g_{mN}}{g_{0N} + g_{0P}} \tag{2}$$

whereas the DC gain of the conventional common-source amplifier in Figure 1b (*CS*) can be expressed as:

$$A_{CS} = \frac{S \cdot g_{mN}}{S \cdot g_{0N} + S \cdot g_{0P}} = \frac{g_{mN}}{g_{0N} + g_{0P}} \tag{3}$$

From Equations (2) and (3) it is evident that the proposed architecture exhibits a DC gain which results in enhancement by a factor of K^2 with respect to the conventional common-source amplifier (about 20 dB higher gain can be achieved for factors K in the range of 3). The additional DC gain results in better feedback performance at low frequencies, such as for example higher linearity and more accurate closed-loop gain.

However, the two additional nodes x and y in Figure 1a complicate the frequency response of the amplifier. In fact, neglecting the output conductances and the gate-drain parasitic capacitances of MOS devices, it can be shown that the proposed OTA exhibits three poles: a dominant pole at the output node, also present in the conventional common-source amplifier, and two additional poles which arise at nodes x and y. Then, in order to compute the frequency response of the amplifier, we observe that the equivalent conductance and the equivalent capacitance at node x are g_{mP} and $(1+K)C_{GSP}$, respectively, whereas the conductance and capacitance at node y are g_{mN} and $(1+H)C_{GSN}$. Under these assumptions, the frequency response of the proposed architecture is:

$$F_{new}(s) \approx \frac{K^2 \cdot H \cdot g_{mN}}{sC_L}\frac{1}{1 + \frac{(1+K)sC_{GSP}}{g_{mP}}}\frac{1}{1 + \frac{(1+H)sC_{GSN}}{g_{mN}}} \tag{4}$$

whereas the frequency response of the conventional common-source amplifier is:

$$F_{CS}(s) = \frac{S \cdot g_{mN}}{sC_L} \tag{5}$$

Here we notice that the proposed amplifier has two additional poles, at frequencies f_{TP}/K and f_{TN}/H, where f_{TX} is the transition frequency of the NMOS ($X = N$) and PMOS ($X = P$) devices. This is the cost of using this topology.

However, there is a great advantage in terms of bandwidth, because the unity-gain frequencies of the two amplifiers are:

$$\omega_{U,new} = \frac{K^2 \cdot H \cdot g_{mN}}{C_L} \tag{6}$$

$$\omega_{U,CS} = \frac{S \cdot g_{mN}}{C_L} \tag{7}$$

These relations show another fundamental property of the proposed circuit. The condition for the two amplifiers to have the same biasing current and power consumption is $S = 2K + H$, which is a linear function of the scaling factors K and H. However, the bandwidth of the propsed amplifier increases by a factor K^2H, which is polynomial in the scaling factors. Hence, a very high bandwidth can be achieved for the same capacitive load and power consumption, by choosing $K, H \gg 1$.

For instance, for $K = 3$ and $H = 12$, and thus $S = 18$, the ratio between the bandwidth of the proposed and the reference single-transistor amplifier is:

$$\frac{\omega_{U,new}}{\omega_{U,CS}} = \frac{K^2 \cdot H}{S} = 6 \tag{8}$$

The proposed amplifier is thus (in this case) 6 times faster than a common-source amplifier implemented in the same technology, with the same load, biasing point, and power consumption. The disadvantage of the proposed topology is the presence of two additional poles. In this case, a well-behaved frequency response requires that the unity-gain frequency is lower than the two additional poles, which, however, are at fairly high frequencies, proportional to the transition frequency of the devices, with scaling factors K and H. Hence, the amplifier is compensated when the load capacitor is sufficiently large to push the unity-gain frequency at sufficiently low frequencies. The compensation technique is similar to that of cascode amplifiers, except for the presence of two additional poles instead of one, and at lower frequencies, owing to the scaling factors.

2.2. Slew-Rate Analysis

The circuit in Figure 1a is in class-A on the rising edge, owing to the current source at the output. A push–pull complementary structure is thus needed to implement class-AB behavior on both signal edges. In this subsection, we consider the circuits in Figure 1 to be half-circuits, and we only consider the falling edge, because the rising edge behaves similarly in the complementary push–pull architecture that has actually been implemented, and which will be detailed in Section 3.

We assume that the input stage is a differential pair, so that the current flowing in the transistors can vary from 0 to $2I_B$ (multiplied by the respective scaling factor). The slew-rate of the common-source amplifier is thus limited to:

$$SR_{CS} = \frac{2 \cdot S \cdot I_B}{C_L} \tag{9}$$

The slew-rate of the proposed amplifier (on the falling edge) can be computed by assuming that the current flowing in the input transistor is twice the biasing current, i.e., $2KI_B$. Because of the PMOS current source above, only $(K+1)I_B$ flows in the PMOS diode. The corresponding current mirror has a gain of K, bringing the current to $K(K+1)I_B$. The NMOS current source removes $(K-1)I_B$, so that the NMOS diode's current is $\left(K^2+1\right)I_B$. The gain of the second current mirror is H, and the final sinking current of the output stage is thus K^2HI_B, also considering the current sourced by the PMOS current source at the output. Hence:

$$SR_{new} = \frac{K^2 \cdot H \cdot I_B}{C_L} \tag{10}$$

Once again, we notice that the proposed amplifier has a much higher peak output current than the conventional common-source stage, for $K, H \gg 1$. For $K = 3$, $H = 12$, the slew-rate improvement is a factor of 3. Hence, for the same load and total power consumption, the proposed amplifier has a much larger slew-rate than the common-source amplifier.

We point out again that the above slew-rate analysis only holds true for the sinking output current, as the source output current is limited by the current generator. However, the complementary push–pull architecture, which will be detailed in Section 3, will have a symmetrical slew-rate behavior, and the slew-rate improvement will occur symmetrically on both the rising and falling signal edges.

2.3. Noise Analysis

While the gain, slew-rate and bandwidth performance of the proposed amplifier increase polynomially with the gain of the current mirrors, noise can be shown to increase linearly, as in the single-stage amplifier. For the two amplifiers in Figure 1, the proposed one has a higher noise power density by a (small) constant factor, as the noise in both amplifiers is approximately linear with the scaling factors.

To derive a simple formulation, we neglect the output resistance r_o of all MOS transistors and only consider white thermal noise, with a given excess noise factor $\gamma \geq 1$ for both NMOS and PMOS devices to consider short-channel effects. We further assume both PMOS and NMOS devices to have the same transconductance.

Under these hypotheses it is straightforward to compute the total input-referred voltage noise of the common-source amplifier in Figure 1b, considering the noise of both the main transistor and the active load:

$$\overline{v_{n,CS}^2} = \frac{8\gamma K_B T}{3g_m}\frac{2}{S}\left[\frac{V^2}{Hz}\right] \tag{11}$$

where K_B is the Boltzmann constant, and T denotes the absolute temperature.

To compute the equivalent input voltage noise for the proposed amplifier in Figure 1a, we refer to the simplified scheme shown in Figure 2, where we notice that the noise injected at node x is amplified by KH, the noise injected at node y is amplified by H, and the noise injected at the output is not amplified. Furthermore, the total transconductance of the stage is K^2Hg_m. Hence:

$$\overline{v_{n,new}^2} = \frac{\left(\overline{i_{D1}^2} + \overline{i_{D2}^2} + \overline{i_{D3}^2}\right)K^2H^2 + \left(\overline{i_{D4}^2} + \overline{i_{D5}^2} + \overline{i_{D6}^2}\right)H^2 + \left(\overline{i_{D7}^2} + \overline{i_{D8}^2}\right)}{K^4H^2g_m^2}. \tag{12a}$$

$$\overline{v_{n,new}^2} = \frac{8\gamma K_B T}{3g_m}\frac{2\left(1 + KH + K^3H\right)}{K^4H}\left[\frac{V^2}{Hz}\right] \tag{12b}$$

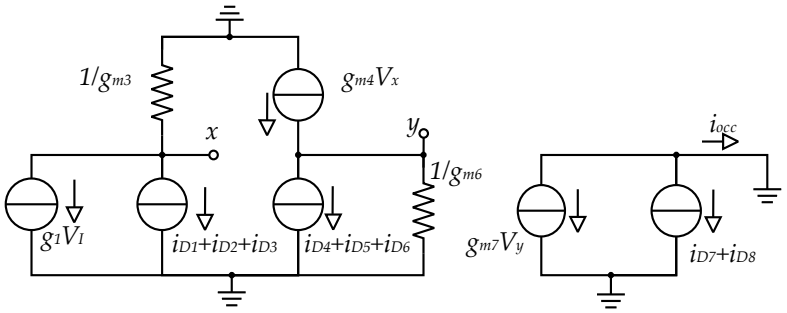

Figure 2. Simplified schematic for noise analysis.

For $K \gg 1$, Equation (12b) can be simplified as:

$$\overline{v_{n,new}^2} \approx \frac{8\gamma K_B T}{3g_m}\frac{2}{K}\left[\frac{V^2}{Hz}\right] \tag{12c}$$

Hence, the proposed amplifier has higher noise power density only because the first stage devices have a width K, which is lower than $S = 2K + H$ (for the same power consumption). This means that noise only increases linearly:

$$\frac{\overline{v_{n,new}^2}}{\overline{v_{n,CS}^2}} \approx \frac{S}{K} = \frac{2K+H}{K} = 2 + \frac{H}{K} \tag{12d}$$

However, this is a worst-case scenario, because we are comparing the baseline proposed amplifier with a single-transistor amplifier. As will be better shown in Section 3, the actual implementation of amplifiers in Figure 1 will have a differential input stage, so that more devices (and more power consumption) are required. Furthermore, to achieve sufficient gain, a folded cascode amplifier is usually employed in place of the conventional common-source stage, resulting in more current branches and thus a reduction in the value of S that is necessary to have the same power consumption.

3. Amplifier Design

The analysis in Section 2 showed that, by using current mirrors with gain, a potentially large increase in gain, bandwidth and slew-rate performance can be achieved, with at most a slight cost in terms of noise, and the creation of two high-frequency poles limiting stability for small capacitive loads.

In this section, we present the actual push–pull implementation of the novel OTA architecture analyzed in Section 2. The proposed implementation is based on a complementary-input push–pull topology with class-AB behavior and exploits input stages with current mirror active loads that improve the common-mode rejection ratio (CMRR). Finally, we compare this implementation against a conventional, class-A, folded cascode topology, with complementary inputs, which serves as reference for the simulations in Section 4.

Figure 3 shows the detailed schematic of the proposed OTA. It is made up of two input differential pairs with active load based on a current mirror. All current mirrors are realized as high-swing cascode current mirrors (HSCCMs) to boost the output resistance, increase the small-signal gain and improve the mirroring accuracy.

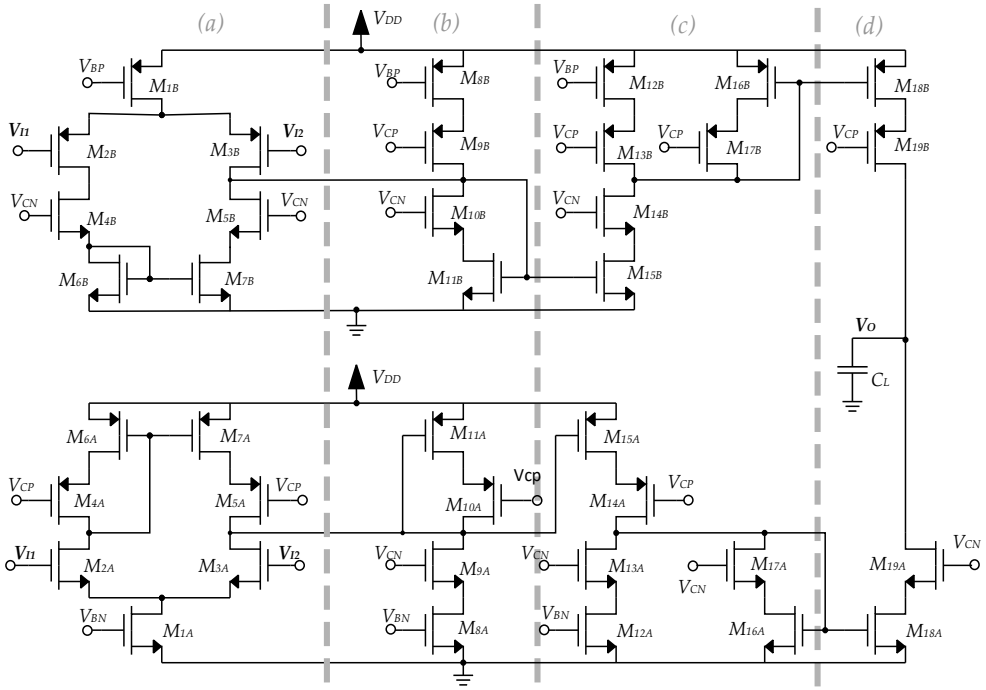

Figure 3. Topology of the proposed amplifier with differential input and single-ended output.

The devices in panel (*a*) form the input differential pairs, whose CMRR is boosted both by the use of tail current generators and by the active load, which cancels the common-mode current by mirroring it to the output with opposite signs (while the differential input is doubled). The devices in the differential pairs have size K. The devices in panel (*b*) are the load of the first stage, whose size is 1, and sets the gain for node x. Panel (*c*) shows the second stage, of size K, with current generators of size $K-1$ and diode loads of size 1, ending at node y. Finally, the output stage has size H and is shown in panel (*d*).

The use of complementary inputs allows rail-to-rail behavior, and improves gain, noise and bandwidth performance. The most important advantage, however, is that the slew-rate behavior is now approximately symmetric, so that both on the positive and negative edges the peak output currents will be very large.

The use of cascoding increases the gain to $K^2 g_m^2 r_0^2$, still K^2 times higher than that of a conventional folded cascode OTA. There will be further poles (also in the conventional cascode) due to the use of HSCCM mirrors, but the main high-frequency poles will still be those at nodes x and y, because they will be at frequencies $f_T/(K+1)$ and $f_T/(H+1)$, while the poles of the HSCCM are at frequencies f_T (f_T denotes the transition frequency of the MOS devices). The tail current generators of the input differential pairs were not cascoded, due to limitations in the voltage headroom.

Figure 4 shows the topology of the complementary-input folded cascode OTA assumed to be the actual implementation of the conventional common-source amplifier used as a reference in Section 2. It has to be noted that a telescopic (Arbel, for a complementary input) cascode is better than the folded cascode in terms of power efficiency, but it is hard to bias and has limited output signal swing; therefore, we consider the folded cascode to be the most appropriate reference for comparisons.

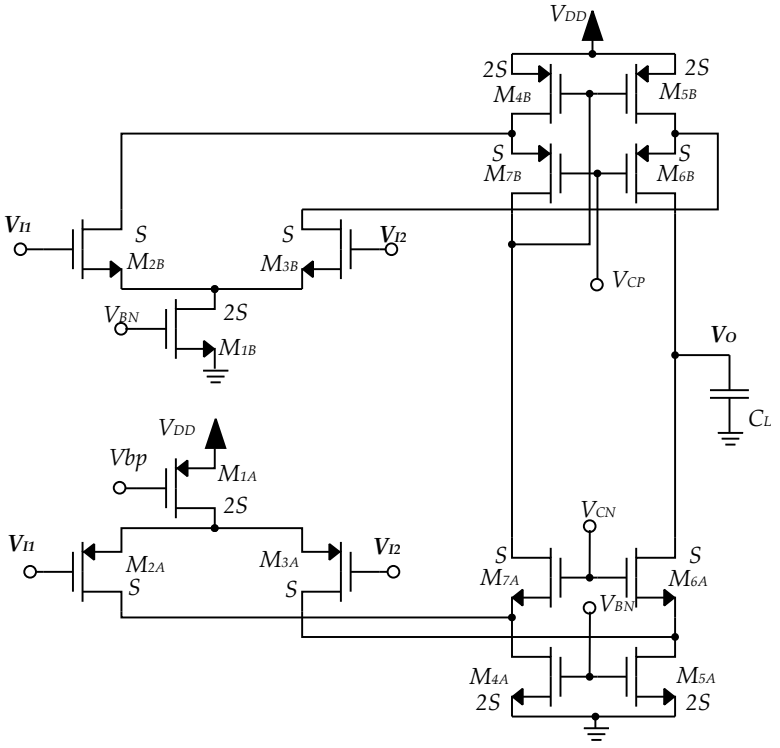

Figure 4. Topology of the implemented folded cascode amplifier used as reference.

V_{BN} and V_{BP} are the biasing voltages, which set the biasing currents across the amplifier, whereas V_{CN} and V_{CP} are the biasing voltages for the gates of the common-gate stages in the cascoded devices. They are generated by a straightforward biasing network (not shown), which can be common to both amplifiers, and is composed of HSCCM current mirrors (both NMOS and PMOS) and an ideal current source.

The total current consumption of the folded cascode in Figure 4 is $6SI_B$, while the total current consumption of the proposed amplifier in Figure 3 is $6K + H + 2$, and hence, to have the same current consumption:

$$S = \frac{6K + H + 2}{6} \tag{13}$$

For the design choice of $K = 3$, $H = 12$, we have $S = 16/3$. We chose $S = 6$ to have an integer scaling factor. Since the disadvantage in noise performance was mostly due to the large value of S (in Section 2.3), the much lower S for the actual amplifier will yield much better bandwidth and slew-rate performance, with a negligible penalty in noise performance, for the proposed amplifier.

4. OTA Design and Simulation Results

This section reports details about the OTA design and the simulation results. Simulations in typical conditions confirm the theoretical result that gain, bandwidth and peak slew-rate improve significantly for the same load and power consumption, while noise density increases slightly. The results of Monte Carlo and parametric simulations also show very good robustness to PVT variations and mismatches.

The proposed OTA, whose topology is shown in Figure 3, was designed in a commercial 130 nm CMOS technology from STMicroelectronics with a supply voltage of 1 V and a total power consumption of about 1 µW. Table 1 shows the sizing of the devices together with the main design parameters.

Table 1. Device sizing and design parameters.

Parameter	Value	Unit	Note
C_L	200	pF	Load capacitor
V_{DD}/V_{SS}	+0.5/−0.5	V	Dual supply voltage
I_B	30	nA	Per unit transistor
K	3	-	Current mirror gain, intermediate stage
H	12	-	Current mirror gain, output stage
L	1	µm	Device length, all devices
W_n	1	µm	Device unit width, NMOS
W_p	3	µm	Device unit width, PMOS

Several considerations need to be taken into account to minimize area occupation. The proposed architecture, as well as the folded cascode, employ stacked transistors. Using a single body-voltage for all NMOS and all PMOS devices, area occupation is minimized with respect to body-driven amplifiers, where separate wells are needed for each input device, requiring space for well isolation. The proposed architecture employs PMOS body terminals connected to V_{DD} and NMOS body terminals connected to $-V_{SS}$, further reducing area occupation.

We define the following Figures of Merit, which are often used in the literature to compare different amplifier designs:

$$SFOM = \frac{B_W C_L}{P_{diss}} \tag{14a}$$

$$SFOM_N = \frac{B_W C_L}{P_{diss} \cdot Area} \tag{14b}$$

$$LFOM_{\pm} = \frac{SR \pm C_L}{P_{diss}} \tag{14c}$$

$$LFOM_{\mathrm{N}\pm} = \frac{SR \pm C_L}{P_{diss} \cdot Area} \tag{14d}$$

where B_W is the closed-loop unity-gain bandwidth, C_L the load capacitance, $SR_{\pm}$ are the positive and negative slew-rate, and P_{diss} (I_{tot}) is the total power (current) consumption. L and S in (14) stand for large-signal and small-signal, while the $S(L)FOM_N$ are normalized with respect to the layout area of the OTA. We consider both positive and negative slew-rate large-signal FOMs, to take into account OTAs with asymmetric slew-rate behavior, while our design, being complementary, is almost symmetrical.

4.1. Results of Typical Simulations

The open-loop frequency response of the proposed OTA from 1 Hz to 10 MHz is shown in Figure 5. The response has a dominant pole at a very low frequency and all higher-frequency poles are beyond the unity-gain frequency, so that the phase margin is high (80°). There are at least three poles at frequencies beyond 1 MHz.

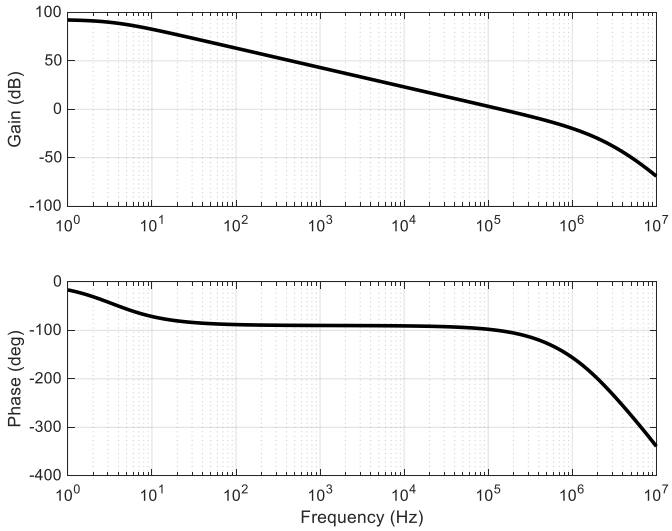

Figure 5. Open-loop frequency response of the proposed amplifier.

Figure 6 shows the closed-loop frequency response in unity-gain configuration. The high phase margin causes the frequency response to be monotonic, and the high DC gain results in a low-frequency closed-loop gain very close to 0 dB.

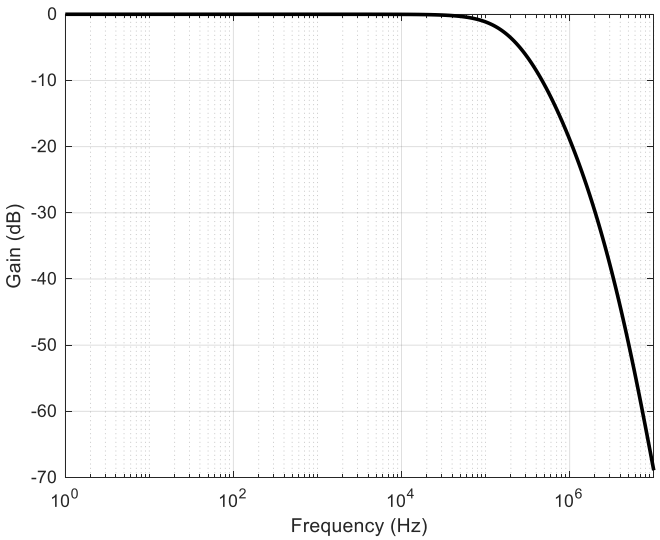

Figure 6. Closed-loop frequency response.

The DC transfer characteristic and the DC gain versus the amplitude of the input signal for values ranging from the negative supply voltage V_{SS} to the positive supply voltage V_{DD} are shown in Figure 7. The non-inverting buffer is critical for large-signal performance because the input common-mode signal varies together with the input signal, so that rail-to-rail behavior proves that both the output and the input common-mode are rail-to-rail. This is mostly due to the complementary input; at least one differential pair is active at each input signal level. Furthermore, linearity is significantly improved by the large DC gain, so that even at −0.45 V and 0.45 V, just 50 mV from the supplies, gain is still 0.95, i.e., −0.45 dB. The folded cascode OTA reported in Figure 4, even if it adopts complementary input differential pairs, exhibits lower linearity (not shown), owing to the much lower DC open-loop gain.

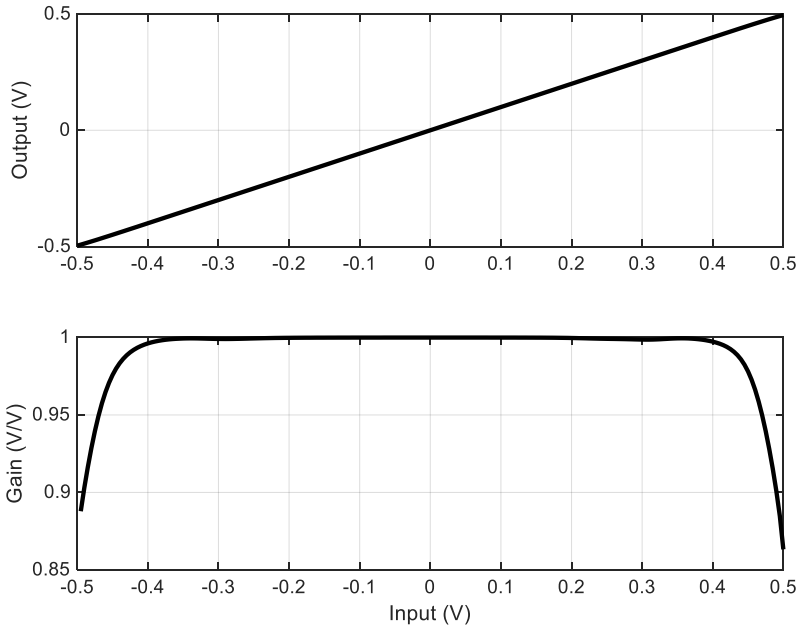

Figure 7. Closed-loop large-signal input/output characteristic and gain.

The DC transfer characteristic and the DC gain versus the amplitude of the input signal for values ranging from the negative supply voltage V_{SS} to the positive supply voltage V_{DD} are shown in Figure 7. The non-inverting buffer is critical for large-signal performance, because the input common-mode signal varies together with the input signal, so that rail-to-rail behavior proves that both the output and the input common-mode are rail-to-rail. This is mostly due to the complementary input; at least one differential pair is active at each input signal level. Furthermore, linearity is significantly improved by the large DC gain, so that even at −0.45 V and 0.45 V, just 50 mV from the supplies, gain is still 0.95, i.e., −0.45 dB. The folded cascode OTA reported in Figure 4, even if it adopts complementary input differential pairs, exhibits lower linearity (not shown), owing to the much lower DC open-loop gain.

Figure 8 shows the response to a sinusoidal input in time and frequency. The output is 500 mVpp, i.e., 50% of the supply rail, and the frequency is 10 kHz. For this input and a capacitive load of 200 pF, the peak output current is 3.1 µA, which is 8.6 times larger than the biasing current of the output stage (360 nA), highlighting the class-AB behavior of the circuit. This also explains why the folded cascode, in class-A, cannot produce a decent output for this signal swing and frequency.

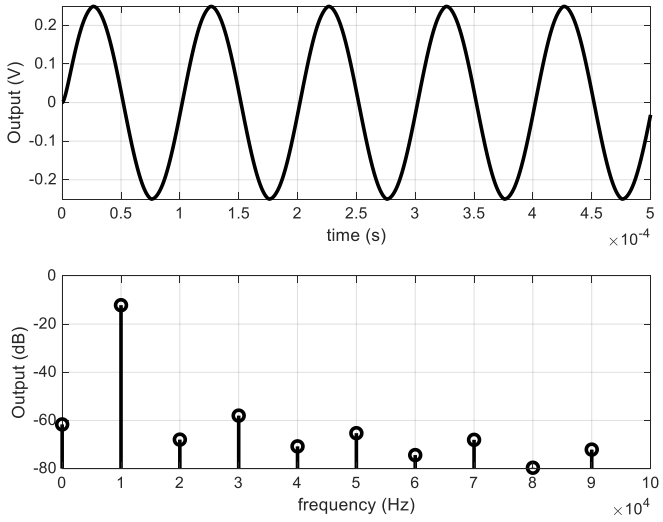

Figure 8. Sinusoidal response in time (**top**) and frequency (**bottom**).

Simulations at 1 kHz from 300 mVpp to 900 mVpp input signal swing show rail-to-rail behavior with high linearity (54 dB at 900 mVpp).

The step response is shown in Figure 9. The transient is monotonic, owing to the large phase margin, and the peak current is significantly larger than output biasing current. In fact, the slew-rate is 30 V/ms on both rising and falling edges, which corresponds to 6 µA over a 200 pF load, 17 times larger than the quiescent current.

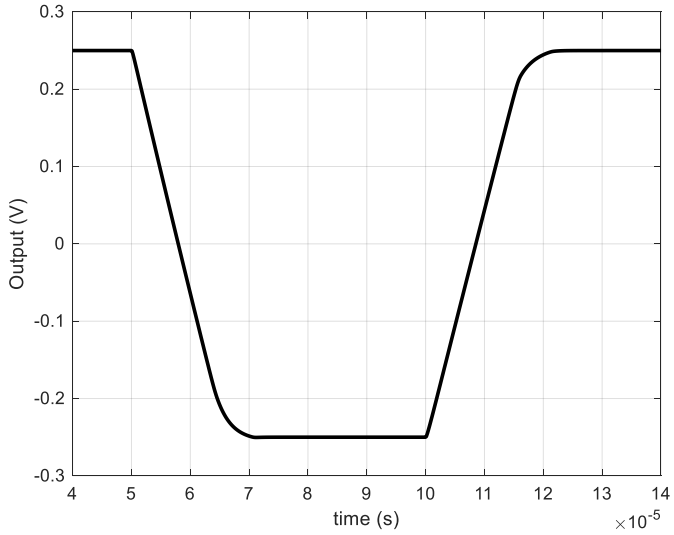

Figure 9. Pulse response of the amplifier.

The output noise spectral density is shown in Figure 10. The noise density for white noise is slightly higher than in the reference cascode amplifier (not shown), because the input stage is smaller in the proposed OTA: $K = 3$, $S = 6$. However, the average spectral noise density (total output noise power divided by the closed-loop bandwidth) is better in the proposed amplifier, due to its much larger bandwidth. In fact, in the conventional folded cascode amplifier, the contribution of flicker noise is dominant, since the noise corner frequency is at several kHz and therefore very close to the amplifier bandwidth.

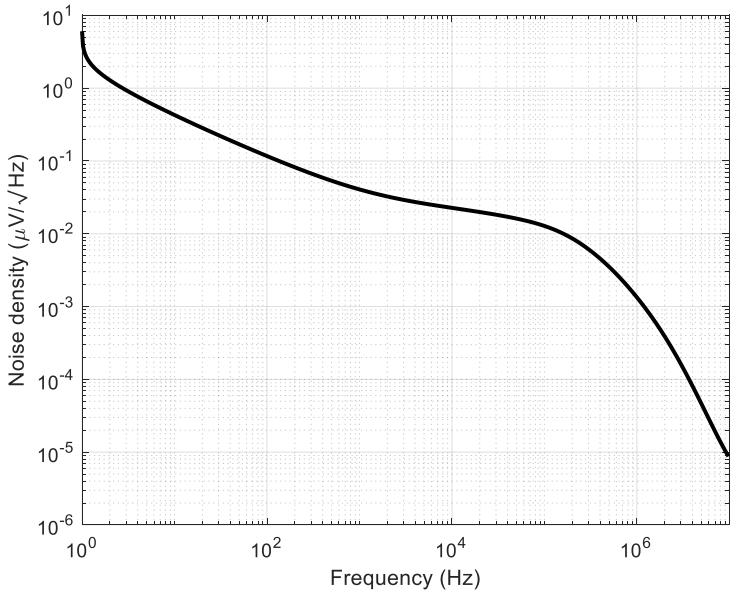

Figure 10. Output noise spectral density from 1 Hz to 10 MHz.

Finally, PSRR and CMRR performance are reported in Figure 11. The CMRR and PSRR are very good, thanks to the small common-mode and supply gains, and the large differential gain. Positive and negative PSRR are almost symmetrical, owing to the complementary push–pull architecture.

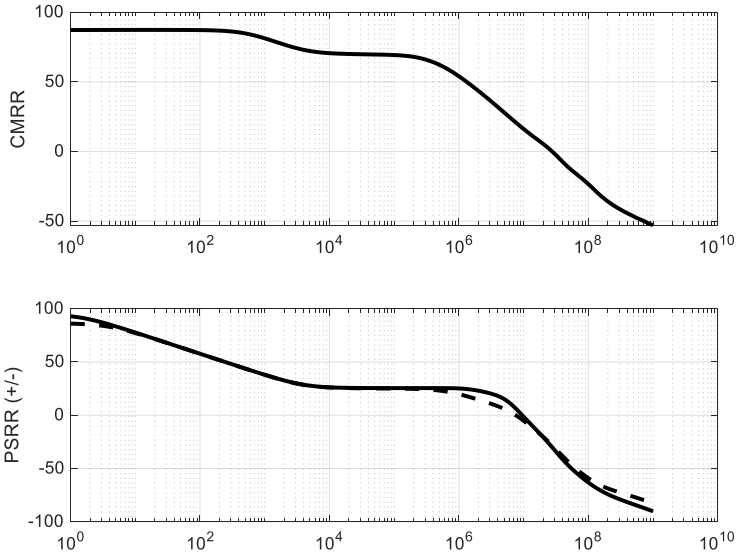

Figure 11. CMRR (**top**) and PSRR (**bottom**) frequency responses. The solid line is the positive PSRR, the dashed line the negative.

The results of the simulations in typical conditions are summarized in Table 2, where A_0, f_u, m_φ, I_{TOT}, V_{os}, V_{oPP}, V_{on}, HDx, SNR, $SNDR$ denote the DC gain, unity-gain frequency, phase margin, total bias current, offset voltage, peak-to-peak output voltage amplitude, output noise integrated between 1 Hz and 10 MHz, x-th order harmonic distortions, signal-to-noise ratio and signal-to-noise-and-distortions ratio, respectively.

Table 2. Typical 27 °C simulation results.

-	Proposed OTA	Conventional Folded Cascode	-
A_0	92	67	dB
f_u	141	7.8	kHz
m_φ	79	90	deg
$PSRR+$	86	52	dB
$PSRR-$	86	53	dB
$CMRR$	87	80	dB
I_{TOT}	990	1100	nA
V_{os}	−14	88	µV
V_{oPP}	500	-	mV
V_{on}	71.3	18	µV
$HD2$	56	-	dB
$HD3$	46	-	dB
$HD5$	53	-	dB
SNR	68	-	dB
$SNDR$	45	-	dB
$SR+$	29.8	0.94	V/ms
$SR-$	31.0	0.96	V/ms
$Area$	1.46k	1.03k	µm^2

The reference folded cascode amplifier has $S = 6$ in order to have roughly the same power consumption, but bandwidth and slew-rate performance are insufficient for processing the 10 kHz 500 mVpp input sinusoid and the 500 mVpp 10 kHz input square wave, so transient data are not reported in Table 2. Gain is also significantly lower, whereas the stability margins are better, owing to the lower number of high-frequency poles, and the much lower unity-gain frequency.

The results in Table 2 show that the proposed OTA exhibits 25 dB higher gain, 18 times larger bandwidth, and 30 times larger peak slew-rate with respect to the reference folded cascode OTA, even with a slightly lower power consumption and the same capacitive load. CMRR and PSRR (positive and negative) data are also very good, owing to the low common-mode and supply voltage gains toward the output. Closed-loop offset (V_{os}) is lower in our design, owing to the higher DC gain. The PSRR of the proposed amplifier is significantly better than that of the reference folded cascode, because amplification is obtained by current mirroring, and current mirrors are insensitive to supply voltage variations. Moreover, the area-normalized FOMs prove the effectiveness of the approach also when area consumption is a concern; the slight penalty in area is more than compensated by the large improvement in bandwidth and slew-rate.

4.2. Temperature and Supply Voltage Simulations

Parametric simulations in temperature were performed at −30, 0, 30, 60, 90, 120 °C, and the best and worst results of the main performance indicators of the OTA in this temperature range are reported in Table 3, confirming the robustness of the OTA with respect to temperature variations, despite the adopted sub-threshold operation of MOS devices. The bandwidth variation is compatible with subthreshold operation, given the inverse relation between the temperature and the transconductance in subthreshold MOS devices.

Table 3. Temperature variations in the −30 °C to 120 °C range.

T	−30	120	°C
A_0	91	92	dB
f_u	160	110	kHz
B_W^{CL}	200	130	kHz
m_φ	79	80	Deg
I_{TOT}	990	1030	nA
V_{os}	20	−40	µV
V_{oPP}	500	500	mV
V_{on}	62	87	µV
$HD2$	49	55	dB
$HD3$	50	43	dB
$HD5$	47	53	dB
SNR	69	66	dB
$SNDR$	47	42	dB
$SR+$	31	30	V/ms
$SR-$	29	30	V/ms

Parametric simulations were also performed for supply voltages equal to 0.9, 1.0 and 1.1 V, i.e., over a 10% variation of the nominal supply voltage. Results for 0.9 V and 1.1 V are reported in Table 4, showing that the amplifier is fundamentally insensitive to supply voltage variations, except for a slight dependence of slew-rate behavior on supply voltage, owing to the larger V_{GS} voltages allowing larger currents in the devices.

Table 4. Supply voltage variations in the 0.9 V to 1.1 V range.

V_{DD}	0.9	1.1	V
A_0	92	93	dB
f_u	140	145	kHz
B_W^{CL}	174	178	kHz
m_φ	79	79	deg
m_G	25	25	dB
I_{TOT}	985	993	nA
V_{os}	−12	−15	µV
V_{oPP}	500	500	mV
V_{on}	71	71	µV
$HD2$	47	56	dB
$HD3$	44	49	dB
$HD5$	46	53	dB
SNR	68	68	dB
$SNDR$	43	45	dB
$SR+$	28	30	V/ms
$SR-$	30	32	V/ms

4.3. Process and Mismatch Monte Carlo Simulations

Monte Carlo simulations were carried out using accurate statistical models of MOS transistors provided by the IC manufacturer, to assess the robustness of the proposed OTA to process and mismatch variations. Tables 5 and 6 show the results of Monte Carlo simulations referring to process and mismatch variations, respectively. Table 5 also reports process corner simulations with fast (F) and slow (S) CMOS devices. The amplifier is fundamentally insensitive to process variations, as the load capacitor is ideal (200 pF) and the transconductance depends on transistor ratios (K, H) and on the biasing current (owing to subthreshold biasing). Sensitivity to mismatches is higher, mostly due to mismatches in the current mirrors, causing variations in the total biasing current (and an offset voltage of 2.6 mVrms). Still, the amplifier is also robust and reliable under mismatch variations, thanks to the large size of the MOS devices.

Table 5. Monte Carlo simulation results (process only) and corner simulations.

-	Mean	Std	FF	FS	SS	SF	Unit
A_0	92.4	0.1	91.2	92.1	92.4	92.2	dB
f_u	141	1	144	141	138	141	kHz
B_W^{CL}	178	1	182	178	174	178	kHz
m_φ	79.1	0.2	78.8	78.9	79.3	79.2	Deg
m_G	25.4	0.2	25.4	25.2	25.6	25.4	dB
I_{TOT}	990	1	993	991	985	987	nA
V_{os}	−14	1	−16	−18	−12	−11	µV
V_{oPP}	499	0	499	499	499	499	mV
V_{on}	71	1	69	71	73	72	µV
$HD2$	55.6	1.0	53.5	51.1	57.7	53.5	dB
$HD3$	46.0	0.7	44.7	49.0	48.7	45.2	dB
$HD5$	53.1	0.3	52.4	53.5	52.4	52.5	dB
SNR	67.9	0.1	68.1	68.0	67.7	67.8	dB
$SNDR$	44.8	0.6	43.5	46.0	46.7	44.0	dB
$SR+$	31.0	100	29.9	29.4	29.5	29.9	V/ms
$SR-$	29.7	100	31.4	31.4	30.5	30.6	V/ms

Table 6. Monte Carlo simulation results (mismatch only).

-	Mean Value	Standard Deviation	-
A_0	91.7	4.9	dB
f_u	138	16	kHz
B_W^{CL}	180	18	kHz
m_φ	77	6	Deg
m_G	25.3	1.7	dB
I_{TOT}	1000	200	nA
V_{os}	0	2.6k	µV
V_{oPP}	499	1	mV
V_{on}	72	2	µV
$HD2$	52.5	7.8	dB
$HD3$	46.0	3.2	dB
$HD5$	53.8	1.5	dB
SNR	67.8	0.3	dB
$SNDR$	43.4	2.4	dB
$SR+$	30.5	1.4	V/ms
$SR-$	29.6	0.5	V/ms

5. Conclusions and Comparisons with the Literature

This paper proposes a novel architecture and design approach to boost gain, bandwidth and slew-rate performance of operational transconductance amplifiers. It shows remarkable improvements with respect to a conventional folded cascode with the same load capacitor and power consumption. Adding intermediate stages employing current mirrors with gain allows a polynomial (in the current mirrors' gain and number of additional stages) increase in gain, bandwidth, and peak slew-rate performance to be obtained for the same power consumption and load. Hence, the use of current-mode gain stages allows the design of OTAs with extremely high FOMs. The resulting amplifier is shown to be robust to PVT variations and mismatches, to have good CMRR and PSRR performance, good noise performance, and very high gain (25 dB higher than a comparable folded cascode), bandwidth (20 times higher) and slew-rate (30 times higher), with a slight improvement also with respect to average noise power density. Table 7 shows a comparison with state-of-the-art OTAs taken from the literature. The proposed amplifier has the highest reported FOMs (both small- and large-signal) in the literature, large gain, and small area footprint.

Table 7. Comparison with the literature (best values shown in bold).

	Unit	This Work	[28]	[34]	[31]	[42]	[30]	[29]	[46]	[27]	[25]	[17]	[32]	[39]	[47]
Year	–	*2021*	*2021*	*2021*	*2020*	*2020*	*2020*	*2020*	*2018*	*2018*	*2017*	*2016*	*2015*	*2015*	*2007*
Process	nm	*130*	*130*	*130*	180	180	180	180	65	180	*350*	*180*	*65*	*350*	*350*
Measured	-	N	N	N	Y	Y	Y	N	N	Y	Y	Y	Y	Y	Y
V_{DD}	V	*1*	*0.3*	*0.3*	0.3	0.3	0.3	0.5	*0.3*	*0.3*	*0.9*	*0.7*	*0.5*	*1*	*0.6*
DC_{gain}	dB	*92*	*40.8*	*64.6*	*64.7*	30	*98.1*	69.5	*60*	65.8	*65*	*57*	*46*	**120**	*70*
C_L	pF	*200*	*40*	*50*	*30*	150	30	15	5	20	*10*	*20*	*3*	*200*	*15*
GBW	kHz	141	*18.65*	3.58	2.96	*0.25*	3.1	*36*	70	*2.78*	1k	*3k*	*38k*	20	11.35
m_φ	deg	*79*	*51.39*	*53.76*	52	**90**	54	*65*	*53*	*61*	*60*	*60*	*57*	*54*	*65*
SR+	V/ms	*30*	*10.83*	*1.7*	1.9	0.068	*14*	*9.7*	*25*	*6.44*	*250*	*2.8k*	*43k*	*7.4*	*14.6*
SR−	V/ms	*30*	*32.37*	*0.15*	*6.4*	*0.101*	*4.2*	*9.7*	*25*	*7.8*	*250*	*2.8k*	*43k*	*2.9*	*14.6*
SR_{avg}	V/ms	*30*	*21.60*	*0.93*	*4.15*	*0.085*	*9.1*	*9.7*	*25*	*7.12*	*250*	*2.8k*	*43k*	*5*	*14.6*
THD	%	*0.20*	*1.4*	0.84	*1*	*2*	*0.49*	*0.27*	–	*1*	*?*	0.99	0.4	–	**0.13**
$@V_{iPP}$	% of V_{DD}	*90*	*80*	100	*85*	*90*	*83.33*	*80*	–	*93.33*	*?*	57.14	–	–	86.67
CMRR	dB	*87*	*67.94*	*61*	*110*	*41*	*60*	*90*	**126**	*72*	*80*	*19*	*35*	*70*	74.5
PSRR	dB	86	*45*	*26*	*56*	*30*	*61*	*81/90*	*90/91*	*62*	50	52.1/66.4	37	**184/198**	53.7
Spot noise	$\mu V/\sqrt{}Hz$	*0.22*	*2.12*	*2.61*	*1.6*	–	*1.8*	*0.91*	*2.82*	*1.85*	*0.065*	*0.1*	*0.94*	*4.85*	0.29
@f	Hz	*10k*	*1k*	*100*	–	–	–	*1k*	*1k*	*36*	–	*1M*	–	*1k*	1k
P_{diss}	nW	*990*	*73*	*11.4*	*12.6*	*2.4*	*13*	*60*	*51*	*15.4*	*24.3k*	*25k*	*182k*	*195*	*550*
MODE	–	*GD*	*BD*	*BD*	*BD*	*DIGITAL*	*BD*	*BD*	*BD*	*BD*	*GD*	*BD*	*BD*	*GD*	*BD*
SFOM	kHz·pF/µW	**35.1*k***	*10.2k*	*15.7k*	*7.05k*	*15.6k*	*7.15k*	*9k*	*2.45k*	*3.61k*	*411*	*2.4k*	*630*	*20.5k*	*310*
$SFOM_N$	$kHz \cdot pF/mW \cdot \mu m^2$	**24.04**	*2.83*	*2.44*	*0.83*	*15.92*	*0.73*	*2.65*	*0.82*	*0.44*	0.029	0.12	0.126	4.66	0.005
$LFOM_{WC}$	V·pF/ms·µW	*6.06k*	*5.93k*	*0.66k*	*4.52k*	*4.25k*	*6.3k*	*2.43k*	*2.45k*	**8.36*k***	*100*	*2.24k*	*710*	*5.0k*	398
$LFOM_{WC_N}$	$V \cdot pF/mW \cdot ms \cdot \mu m^2$	*4.15*	*1.65*	*0.1*	*0.53*	**4.34**	*0.64*	*0.71*	*0.82*	*1.02*	0.007	0.11	0.142	0.68	0.006
Area	μm^2	**1.46*k***	*3.6k*	*6.4k*	*8.5k*	*0.98k*	*9.8k*	*3.4k*	*3k*	*8.2k*	*14.0k*	*19.8k*	*5.0k*	*4.4k*	60*k*

It is evident that the FOMs of the proposed amplifiers are much larger than any comparable amplifier. The best in the literature so far, [6], has about one half of the small-signal FOM, and 17% lower large-signal FOM. Simulations show that the theoretical idea behind the proposed architecture allows achieving record-breaking bandwidth and slew-rate performance, besides large gain increases, for low-power amplifiers. Moreover, the proposed architecture shows remarkable improvement in terms of area-normalized FOMs. Indeed, the gate-driven approach allows the minimization of the layout area, given that, unlike body-driven amplifiers, it does not require separate wells for the devices. As a result, the proposed architecture shows the highest $S(L)FOM_N$, therefore proving to be an excellent choice when both bandwidth and slew-rate and area consumption are important requirements.

Author Contributions: Conceptualization, P.M.; Methodology, P.M., F.C., G.S.; Software, P.M., R.D.S.; Validation, P.M., F.C., G.S., R.D.S., A.T.; Formal Analysis, P.M.; Investigation, P.M., R.D.S.; Data Curation, P.M., R.D.S.; Writing—Original Draft Preparation, P.M., R.D.S.; Writing—Review & Editing, P.M., F.C., G.S., R.D.S., A.T.; Visualization, P.M.; Supervision, P.M., F.C., G.S., A.T.; Project Administration, P.M., F.C., G.S., A.T. All authors have read and agreed to the published version of the manuscript.

Funding: This research received no external funding.

Conflicts of Interest: The authors declare no conflict of interest.

References

1. Alioto, M. *Enabling the Internet of Things—From Integrated Circuits to Integrated Systems*; Springer: New York, NY, USA, 2017.
2. Balas, V.E.; Solanki, V.K.; Kumar, R.; Ahar, M.A.R. *A Handbook of Internet of Things in Biomedical and Cyber Physical System*; Springer: New York, NY, USA, 2020.
3. Wang, J.; Lim, M.K.; Wang, C.; Tseng, M.L. The evolution of the Internet of Things (IoT) over the past 20 years. *Comput. Ind. Eng.* **2021**, *55*, 107174. [CrossRef]
4. Sala, R.D.; Monsurrò, P.; Scotti, G.; Trifiletti, A. Area-Efficient Low-Power Bandpass Gm-C Filter for Epileptic Seizure Detection in 130nm CMOS. In Proceedings of the ICECS 2019 IEEE International Conference Electronics, Circuits and Systems, Genoa, Italy, 27–29 November 2019; pp. 298–301.
5. Lebedev, M.A.; Nicolelis, M.A.L. Brain-machine interfaces: Past, present and future. *Trends Neurosci.* **2006**, *29*, 536–546. [CrossRef]
6. Lin, Q.; Song, S.; Castro, I.D.; Jiang, H.; Konijnenburg, M.; van Wegberg, R.; Biswas, D.; Stanzione, S.; Sijbers, W.; Van Hoof, C.; et al. Wearable multiple modality bio-signal recording and processing on chip: A review. *IEEE Sens. J.* **2021**, *21*, 1108–1123. [CrossRef]
7. Avoli, M.; Centurelli, F.; Monsurrò, P.; Scotti, G.; Trifiletti, A. Low power DDA-based instrumentation amplifier for neural recording applications in 65 nm CMOS. *AEU Int. J. Electron. Commun.* **2018**, *92*, 30–35. [CrossRef]
8. Jeong, S.; Kim, D.H.; Song, J.; Kim, H.; Lee, S.; Song, C.; Lee, J.; Song, J.; Kim, J. Smartwatch strap wireless power transfer system with flexible PCB coil and shielding material. *IEEE Trans. Ind. Electron.* **2019**, *55*, 4054–4064. [CrossRef]
9. Far, A. Enhanced gain, low voltage, rail-to-rail buffer amplifier suitable for energy harvesting. In Proceedings of the ROPEC 2017 IEEE International Autumn Meeting on Power, Electronics and Computing, Ixtapa, Mexico, 8–10 November 2017.

10. Far, A. Amplifier for energy harvesting: Low voltage, ultra low current, rail-to-rail input-output, high speed. In Proceedings of the ROPEC 2016 IEEE International Autumn Meeting on Power, Electronics and Computing, Ixtapa, Mexico, 9–11 November 2016.
11. Magno, M.; Wang, X.; Eggimann, M.; Cavigelli, L.; Benini, L. InfiniWolf: Energy efficient smart bracelet for edge computing with dual source energy harvesting. In Proceedings of the DATE 2020 Design, Automation & Test in Europe Conference, Grenoble, France, 9–13 March 2020; pp. 342–345.
12. Grasso, A.D.; Pennisi, S. Ultra-low power amplifiers for IoT nodes. In Proceedings of the ICECS 2018 IEEE International Conference Electronics Circuits and Systems, Bordeaux, France, 9–12 December 2018; pp. 497–500.
13. Far, A. Low noise rail-to-rail amplifier runs fast at ultra low currents and targets energy harvesting. In Proceedings of the ROPEC 2017 IEEE International Autumn Meeting on Power, Electronics and Computing, Ixtapa, Mexico, 8–10 November 2017.
14. Richelli, A.; Colalongo, L.; Kovacs-Vajna, Z.; Calvetti, G.; Ferrari, D.; Finanzini, M.; Pinetti, S.; Prevosti, E.; Savoldelli, J.; Scarlassara, S. A survey of low voltage and low power amplifier topologies. *J. Low Power Electron. Appl.* **2018**, *8*, 22. [CrossRef]
15. Cellucci, D.; Centurelli, F.; Di Stefano, V.; Monsurrò, P.; Pennisi, S.; Scotti, G.; Trifiletti, A. 0.6V CMOS cascode OTA with complementary gate-driven gain boosting and forward body bias. *Int. J. Circuit Theory Appl.* **2020**, *48*, 15–27. [CrossRef]
16. Akbari, M.; Hashemipour, O. A 0.6-V, 0.4-µW bulk-driven operational amplifier with rail-to-rail input/output swing. *Analog Integr. Circuits Signal Process.* **2016**, *86*, 341–351. [CrossRef]
17. Cabrera-Bernal, E.; Pennisi, S.; Grasso, A.D.; Torralba, A.; Carvajal, R.G. 0.7-V three-stage class-AB CMOS operational transconductance amplifier. *IEEE Trans. Circuits Syst. Part I* **2016**, *63*, 1807–1815. [CrossRef]
18. Miguel, J.M.A.; Lopez-Martin, A.J.; Acosta, L.; Ramirez-Angulo, J.; Carvajal, R.G. Using floating gate and quasifloating-gate techniques for rail-to-rail tunable CMOS transconductor design. *IEEE Trans. Circuits Syst. Part I* **2011**, *58*, 1604–1614. [CrossRef]
19. Centurelli, F.; Monsurrò, P.; Parisi, G.; Tommasino, P.; Trifiletti, A. A topology of fully differential class-AB symmetrical OTA with improved CMRR. *IEEE Trans. Circuits Syst. Part II* **2018**, *65*, 1504–1508. [CrossRef]
20. Garde, M.P.; Lopez-Martin, A.; Algueta, J.M.; Carvajal, R.G.; Ramirez-Angulo, J. Class AB amplifier with enhanced slew rate and GBW. *Int. J. Circuit Theory Appl.* **2019**, *47*, 1199–1210. [CrossRef]
21. Ng, K.A.; Xu, Y.P. A low-power, high CMRR neural amplifier system employing CMOS inverter-based OTAs with CMFB through supply rails. *IEEE J. Solid State Circuit* **2016**, *51*, 724–737.
22. Castaño, F.; Torelli, G.; Pérez-Aloe, R.; Carrillo, J.M. Low-voltage rail-to-rail bulk-driven CMFB network with improved gain and bandwidth. In Proceedings of the ICECS 2010 IEEE Int. Conf. Electronics Circuits and Systems, Athens, Greece, 12–15 December 2010; pp. 207–210.
23. Centurelli, F.; Monsurrò, P.; Trifiletti, A. High-gain, high-CMRR class-AB operational transconductance amplifier based on the flipped voltage follower. *Int. J. Circuit Theory Appl.* **2019**, *47*, 499–512. [CrossRef]
24. Wang, Y.; Zhang, Q.; Zhao, X.; Dong, L. An enhanced bulk-driven OTA with high transconductance against CMOS scaling. *AEU Int. J. Electron. Commun.* **2021**, *130*, 153581. [CrossRef]
25. Grasso, A.D.; Pennisi, S.; Scotti, G.; Trifiletti, A. 0.9-V class-AB Miller OTA in 0.35-µm CMOS with threshold-lowered non-tailed differential pair. *IEEE Trans. Circuits Syst. Part I* **2017**, *64*, 1740–1747. [CrossRef]
26. Centurelli, F.; Monsurrò, P.; Parisi, G.; Tommasino, P.; Trifiletti, A. A 0.6V class-AB rail-to-rail CMOS OTA exploiting threshold lowering. *IET Electron. Lett.* **2018**, *54*, 930–932. [CrossRef]
27. Kulej, T.; Khateb, F. Design and implementation of sub 0.5-V OTAs in 0.18-µm CMOS. *Int. J. Circuit Theory Appl.* **2018**, *46*, 1129–1143. [CrossRef]
28. Centurelli, F.; Della Sala, R.; Monsurrò, P.; Scotti, G.; Trifiletti, A. A 0.3 V rail-to-rail ultra-low-power OTA with improved bandwidth and slew rate. *J. Low Power Electron. Appl.* **2021**, *11*, 19. [CrossRef]
29. Deo, N.; Sharan, T.; Dubey, T. Subthreshold biased enhanced bulk-driven double recycling current mirror OTA. *Analog Integr. Circuits Signal Process.* **2020**, *105*, 229–242. [CrossRef]
30. Kulej, T.; Khateb, F. A 0.3-V 98-dB rail-to-rail OTA in 0.18 µm CMOS. *IEEE Access* **2020**, *8*, 27459–27567. [CrossRef]
31. Kulej, T.; Khateb, F. A compact 0.3-V class AB bulk-driven OTA. *IEEE Trans. VLSI Syst.* **2019**, *28*, 224–232. [CrossRef]
32. Abdelfattah, O.; Roberts, G.W.; Shih, I.; Shih, Y. An ultra-low-voltage CMOS process-insensitive self-biased OTA with rail-to-rail input range. *IEEE Trans. Circuits Syst. Part I* **2015**, *62*, 2380–2390. [CrossRef]
33. Baghtash, H.F. A 0.4V, body-driven, fully differential, tail-less OTA based on current push-pull. *Microelectron. J.* **2020**, *99*, 104768. [CrossRef]
34. Centurelli, F.; Della Sala, R.; Scotti, G.; Trifiletti, A. A 0.3 V, rail-to-rail, ultralow-power, non-tailed, body-driven, sub-threshold amplifier. *Appl. Sci.* **2021**, *11*, 2528. [CrossRef]
35. Rodovalho, L.H.; Aiello, O.; Rodrigues, C.R. Ultra-low-voltage inverter-based operational transconductance amplifiers with voltage gain enhancement by improved composite transistors. *Electronics* **2020**, *9*, 1410. [CrossRef]
36. De Aguirre, P.C.C.; Bonizzoni, E.; Maloberti, F.; Susin, A.A. A 170.7-dB FoM-DR 0.45/0.6-V inverter-based continuous-time sigma–delta modulator. *IEEE Trans. Circuits Syst. Part II* **2020**, *67*, 1384–1388. [CrossRef]
37. Jung, Y.H.; Hong, S.K.; Kwon, O.K. A low load- and cross-regulation SIDO converter using an adaptive current sensor and LDO regulator with a selectable charge pump for mobile devices. *Analog Integr. Circuits Signal Process.* **2017**, *92*, 293–301. [CrossRef]

38. Nguyen, B.; Tang, N.; Hong, W.; Zhou, Z.; Heo, D. High-efficiency fully integrated switched-capacitor voltage regulator for battery-connected applications in low-breakdown process technologies. *IEEE Trans. Power Electron.* **2018**, *33*, 6858–6868. [CrossRef]
39. Grasso, D.; Marano, D.; Palumbo, G.; Pennisi, S. Design methodology of subthreshold three-stage CMOS OTAs suitable for ultra-low-power low-area and high driving capability. *IEEE Trans. Circuits Syst. Part I* **2015**, *62*, 1453–1462. [CrossRef]
40. Giustolisi, G.; Palumbo, G. Design of three-stage OTA based on settling-time requirements including large and small signal behavior. *IEEE Trans. Circuits Syst. Part I* **2021**, *68*, 998–1011. [CrossRef]
41. Giustolisi, G.; Palumbo, G. A gm/id-based design strategy for IoT and ultra-low-power OTAs with fast-settling and large capacitive loads. *J. Low Power Electron. Appl.* **2021**, *11*, 21. [CrossRef]
42. Toledo, P.; Crovetti, P.; Aiello, O.; Alioto, M. Fully digital rail-to-rail OTA with sub-1000-μm^2 area, 250-mV minimum supply, and nW power at 150-pF load in 180 nm. *IEEE Solid State Circuits Lett.* **2020**, *3*, 474–477. [CrossRef]
43. Toledo, P.; Crovetti, P.; Aiello, O.; Alioto, M. Design of digital OTAs with operation down to 0.3 V and nW power for direct harvesting. *IEEE Trans. Circuits Syst. Part I* **2021**, in press. [CrossRef]
44. Rodovalho, L.H.; Rodrigues, C.R.; Aiello, O. Self-biased and supply-voltage scalable inverter-based operational transconductance amplifier with improved composite transistors. *Electronics* **2021**, *10*, 935. [CrossRef]
45. Toledo, P.; Crovetti, P.; Klimach, H.; Bampi, S.; Aiello, O.; Alioto, M. 300mV-supply, sub-nW-power digital-based operational transconductance amplifier. *IEEE Trans. Circuits Syst. Part II* **2021**, in press. [CrossRef]
46. Veldandi, H.; Shaik, R.A. A 0.3-V pseudo-differential bulk-input OTA for low-frequency applications. *Circuits Syst. Signal Process.* **2020**, *37*, 5199–5221. [CrossRef]
47. Ferreira, L.H.C.; Pimenta, T.C.; Moreno, L.R. An ultra-low-voltage ultra-low-power CMOS Miller OTA with rail-to-rail input/output swing. *IEEE Trans. Circuits Syst. Part II* **2007**, *54*, 843–847. [CrossRef]