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Floating Filler (FF) in an Indium Gallium Zinc Oxide (IGZO) Channel Improves the Erase Performance of Vertical Channel NAND Flash with a Cell-on-Peri (COP) Structure

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Abstract: In this study, we developed a V-NAND with an improved IGZO-P type (IP) floating filler (FF) structure based on an IGZO channel verified in previous studies and demonstrated that it has a very fast erase speed through device simulation. The proposed FF structure can supply holes generated through the Gate-Induced Drain Leakage (GIDL) phenomenon in the upper polysilicon string select line (SSL) channel to the IGZO channel through a P-type filler, and the structure proposed by this operation shows a very fast erase speed of 4 µs. A fast erase speed was achieved because the filler adjacent to the IGZO channel, like IP structures in previous studies, functioned as a path through which electrons emitted from the charge storage layer moved easily, rather than simply supplying holes. This assumption was confirmed by assessing the change in electron density of the channel during the erase operation. Next, we investigated the optimum conditions for leakage current reduction through various condition changes of the lower ground select line (GSL) gate in the proposed structure. We confirmed that the leakage current of the proposed structure can be minimized by changing the number of lower GSL gates, changing the length of the GSL channel, and/or changing the work function of the GSL gate material. We obtained a leakage current of 10^{-17} A when the GSL channel was 480 nm long with six GSL gates, each with a length of 40 nm. The work function of the gates was 4.96 eV.

Keywords: IGZO; vertical channel NAND flash; polysilicon; GIDL

1. Introduction

NAND flash technology for high-density storage has been utilized extensively in industry. After the first vertical channel NAND flash technology was announced by Toshiba in 2007 [1], Samsung developed the Terabit Cell Array Transistor (TCAT) [2] and SK Hynix developed the Stacked Memory Array Transistor (SMArT) [3] in 2009 based on this technology. Much progress has been made since then, particularly the development of vertical channel structures, and the layering of vertical channels to form a 100-layer stacked structure was achieved in 2019 [4].

Although the usefulness of a vertical channel NAND (V-NAND) structure is clear, continuous improvement of device performance has been difficult because of several disadvantages of the polysilicon used as a channel material in realistic operating environments. The principal problems are an increase in the leakage current due to grain boundaries of the polysilicon, scattering of the threshold voltage, and a change in operating current with temperature [5–8]. Since these problems are fatal in V-NAND operation, research aimed at solving these problems is ongoing. One proposed solution is to change the channel material to one resistant to the leakage current and temperature change; IGZO is one candidate for such material.



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Copyright: © 2021 by the authors. Licensee MDPI, Basel, Switzerland. This article is an open access article distributed under the terms and conditions of the Creative Commons Attribution (CC BY) license (https:// creativecommons.org/licenses/by/ 4.0/). IGZO is a material described by the Sharp and Hosono groups in 2004 [9–11] that has since been studied extensively as a TFT channel material for displays because of its relatively wide bandgap (~3.1 eV) and moderately high carrier mobility (10–65 cm²/V·s). Recently, it has been shown that the crystal structure can be easily formed in a chosen direction in the form of C-AXIS aligned crystal (CAAC)-IGZO [12–14]. The use of this type of IGZO as a channel material should be able to overcome the problems of leakage current interruption and temperature-dependent operating current.

Using IGZO as a channel material in a V-NAND structure can potentially improve the leakage current and ameliorate changes in current due to operating temperature. However, because of the very poor hole carrier properties of IGZO, the hole erase method cannot be used for V-NAND structures with IGZO channels. This problem could potentially be a fatal weakness for the use of IGZOs considering that other erase operations are practically impossible in V-NAND structures.

To solve this problem, we studied an IGZO-nitride-P type filler (INP) structure and an IGZO-P type filler (IP) structure in previous studies and verified these structures through device simulations. The proposed INP and IP structures have an added P-type filler (P-filler) in the center of the holes in the V-NAND structure [15]. This filler is connected to the P-sub region at the bottom of the structure to facilitate the rapid transport of hole carriers, thereby assisting in maintaining high voltage across the entire channel during the erase operation. When a high voltage is supplied to the channel by the filler, the field erase operation and electron-hole recombination by the supplied holes are possible by the potential difference between the high voltage of the IGZO channel and the ground voltage of each WL. Because of these phenomena, when the IP structure proposed in the previous study was applied to the V-NAND structure, the deletion operation speed was 2.5 μ s. This is a very fast erase rate compared with the ~10 ms erase rate of the conventional V-NAND architecture.

However, peri-under-cell (PUC) or cell-on-peri (COP) structures have been introduced in recent V-NAND structures to improve the degree of integration. By placing the peri circuit area for cell array control in the V-NAND structure below the existing cell array, the entire chip area can be drastically reduced. However, to obtain such a structure, a polysilicon material used only for general deposition needs to be used because the crystallization of crystalline silicon material is impossible. Polysilicon sub-layers formed in this way cannot freely move holes because of the many traps present, so hole carriers required for bulk erase are not available.

To address this issue, a GIDL erase method [1], which does not require a sub-layer, should be used for a V-NAND structure with an attached PUC structure. Therefore, it is necessary to optimize the IP structure proposed previously for application in the PUC structure. In this paper, we developed a floating filler (FF) structure and verified the GIDL erase performance of this structure by device simulation.

2. Details of the Proposed Structure and Operation

The structure proposed in this paper is illustrated in Figure 1a. As shown in Figure 1b, in the SSL region at the top, there is a high concentration of N-type doped polysilicon to generate holes by the GIDL phenomenon and a low-concentration P-type polysilicon layer to transfer these holes to the IGZO channel. This P-type polysilicon layer should have a low concentration of P-type doped states to facilitate hole transfer. Next, in the WL region of Figure 1c, hole carriers transferred from the top and charged in the filler are transferred to the IGZO channel by the high voltage of BL. The same effect can be expected for this structure, as it has been proven by prior research that an IGZO channel with a thickness of about 20 nm can sufficiently transmit holes if there are enough hole carriers in the filler. The GSL area shown in Figure 1d should have a certain minimum height to block the leakage current. IGZO channels have a very low leakage current, but the threshold voltage of the IGZO channel, which is a weak N-type state, can be negative. Therefore, even when the gate voltage is in the GND state, some current can pass. Therefore, to reliably suppress

the leakage current without changing the material properties of the IGZO channel, it is important to determine the optimum channel length.



Figure 1. Description of a floating filler (FF) structure for ferroelectric memory based on the gateinduced drain leakage (GIDL) phenomenon. (**a**) Overall structure, (**b**) string select line (SSL) transistor structure with an over-doped region to generate the GIDL phenomenon, (**c**) word line (WL) region, and (**d**) ground select line (GSL) region without an over-doped region.

A more detailed explanation of the erase operation is provided in Figure 2. First, the operating voltage shown in Figure 2a is almost the same as that of a general V-NAND, but in the case of the lower GSL region, it is not necessary to generate the GIDL phenomenon, so instead of applying 20 V, it can be kept in a floating state. As shown in Figure 2b, it is possible to transfer holes formed by the GIDL phenomenon in SSL to the charge trap layer through the IGZO channel during the erase operation. The transferred holes neutralize electrons by generating e–h recombination with the stored electrons. This phenomenon is also an important mechanism in the erase operation of charge trap flash (CTF) memory. If one tries to erase according to the GIDL phenomenon with only the IGZO channel, the hole concentration of IGZO is low, so the hole is not transmitted to the channel and the erase operation itself does not proceed. Since these problems have already been demonstrated in our previous work, it can be said that the proposed FF structure is essential to enable the erase operation in V-NAND structures based on CTF memories and IGZO channels.



Figure 2. (a) Voltage applied during the erase operation in the floating filler structure and (b) the mechanism of the erase operation.

3. Simulation Results and Discussion

In this study, we used the Sentaurus simulation tool of Synopsys [16] to form half of the vertical channel NAND structure section. In addition, this structure was employed as the virtual gate-all-around (GAA) structure during device simulation through the cylindrical command (360 degree rotation) of the Sentaurus tool. Through this process, a complete vertical channel 3D NAND string was simulated.

First, as shown in Figure 3a, the structure used had 10 word lines (WL), a string select line (SSL) at the top, and a ground select line (GSL) at the bottom. In addition, a bit line (BL) served as a drain at the top of the highest level, and a common source line (CSL) served as a source at the lowest level. Detailed information, such as descriptions and the thickness and height of the various materials, are displayed in the enlarged structure located to the right of the entire structure. Since the displayed structure shows half the entire string, the actual string diameter is 100 nm, and accordingly, the diameter of the polysilicon filler is 20 nm. Figure 3b shows the doping states of the simulated structure. As described above, the polysilicon channel for the GIDL generation and an excessively doped region exist only in the SSL region, not the GSL region. If the same structure exists in the GSL region, holes generated by the GIDL phenomenon cannot be transferred to the IGZO channel because there is no filler, resulting in a meaningless operation. Therefore, the structure for the GIDL phenomenon should be present only in the upper SSL area connected to the filler.



Figure 3. Details of the simulated device and a description of the state of doping. (**a**) Overall structure and enlarged view of the simulation structure used. (**b**) Description of the doping state.

Note that doping concentration dependence, high field saturation, and trap scattering mobility models were used in the device simulations. In addition, Shockley–Read–Hall, Auger, and Hurkx band-to-band recombination models were used to simulate the operation of the IGZO transistor and the V-NAND structure. The filler region in the proposed structure had a trap concentration of 5×10^{17} cm⁻³. In addition, for each material trap, the parameters listed in Table 1 for polysilicon, IGZO, and silicon nitride were applied. Table 2 shows the applied voltages for each operation.

Figure 4 shows the memory operation simulation results using the V-NAND structure of a general polysilicon channel and the FF structure of the proposed IGZO channel. The proposed FF structure showed a very fast erase speed, as we expected. Specifically, the erase rate of the known erase operation of the conventional V-NAND structure was 10 ms, whereas the erase rate of the proposed FF structure was 4 μ s.

D (Value				
Parameters	Polysilicon [16]	IGZO [17,18]	Si ₃ N ₄ [19]		
Trap concentration (cm ⁻³) (electrons, hole trap)	1×10^{21}	$1 imes 10^{20}$	$1 imes 10^{20}$ (electrons) $1 imes 10^{19}$ (holes)		
Energy level (eV)	0.1 (electrons) -0.1 (holes)	0.55 (electrons) -0.175 (holes)	2.5 (electrons) —1.0 (holes)		

Table 1. Trap parameters of each material.

Table 2. Applied voltages for each operation.

Operation -	Value					
	Target (WL5)	Non-Target (Other WLS)	GSL	SSL	BL	CSL
Program	20 V	5 V	0 V	5 V	0V	0 V
Erase	0 V	0 V	10 V	10 V	20 V	20 V
Read	-5 to 7 V	5 V	5 V	5 V	1 V	0 V



Figure 4. Memory simulation results for the general V-NAND structure and the proposed FF structure: (**a**) program operation and (**b**) erase operation.

These results suggest that the proposed FF structure requires very little time, so it is expected that the erase operation will consume very little power. Of course, in order to accurately calculate the power consumption in the erase operation, the high voltage circuit required to generate a high erase voltage must be considered, but the voltage used for the erase operation of the proposed structure is the same as the voltage used in the conventional V-NAND structure. Therefore, the only difference in the calculation of energy consumption is the operating time. Based on this, we expect that the proposed FF structure will consume approximately 1000 times less energy during the erase operation than the existing V-NAND structure.

The cause of the outstanding erasing performance of the proposed FF structure is explained in Figure 5. First, considering the change in the electron density of each channel during the erasing operation shown in Figure 5a, in the case of the existing V-NAND structure, similar to the change in the threshold voltage, after 10 μ s, electron density was almost constant at 10⁵ cm⁻³. On the contrary, in the case of the proposed FF structure, it can be seen that, similar to the change in the threshold voltage, electron density rapidly decreased after 1 μ s and approached zero. On the contrary, it can be seen that the electron density of the FF structure adjacent to the IGZO channel maintained a relatively high value of 10⁵ to 100 cm⁻³ during the erasing operation. As a result of this, it can be considered that the electrons emitted from the silicon nitride layer during the erasing operation in the FF structure do not accumulate in the channel but are emitted directly to the bit line contact through the filler.



Figure 5. Description of the movement of electrons through the structure in the erase operation. (**a**) Electron density in the channel during the erase operation and (**b**) movement of electrons in each structure.

Figure 5b shows the movement of electrons during the erase operation. As mentioned above, in the existing V-NAND structure, electrons emitted from the silicon nitride layer during the erase operation enter the channel and then move in the direction of each contact because of the high voltage of the bit line (BL) or common source line (CSL). However, this movement means that many electrons emitted from silicon nitride through very thin channels have to be moved a long distance by the high voltage of distant contacts. Therefore, the electron density of the channel is always kept high during the erase operation, and electrons remain in place. By contrast, in the FF structure, the emitted electrons are immediately attracted by the high voltage of the filler and move to the filler. For this reason, the electron density of the channel can always be kept low, and the movement of electrons is very fast. Because of these advantages, the proposed FF structure does not cause congestion of electron movement and has a very fast erase speed.

Overall, we confirmed that the proposed FF structure uses the GIDL erase method but has an extremely fast erase speed similar to that of the INP and IP structures proposed in previous studies because of the presence of filler inside the channel. This indicates that the proposed structure can use the operation of existing V-NANDs while maintaining the unique characteristics of the IGZO channel, including a low leakage current and stable temperature change performance.

Next, the most important gate in the proposed structure is the GSL, which controls the current in the CSL direction during V-NAND operation to suppress the leakage current in the standby state and plays an important role in program suppression mode during multi-string operation. In particular, in the case of the SSL, which is required for stronger and more accurate operation for the same reasons, a polysilicon channel must be used to generate the GIDL phenomenon. Therefore, the structure and operating characteristics of the novel V-NAND proposed here, such as the leakage current, will be similar to those of existing V-NAND structures. However, if a polysilicon channel is used up to the GSL, it will not be possible to obtain the low leakage current characteristic of an IGZO channel because both gates are polysilicon channels. One of the two gates must contain an IGZO channel, and considering the COP structure, the IGZO channel should be used as the lower GSL gate. However, to use the IGZO channel in the GSL gate, the low threshold voltage of the IGZO channel FET needs to be overcome.

Figure 6 and Table 3 show the results of verifying the operation characteristics of the GSL mentioned in the previous article in the proposed FF structure. this result shows a fairly high leakage current of about 10^{-13} A. In addition, even if the GSL was kept in the off state, the leakage current did not decrease at all, and the high current of 10^{-8} A was maintained. This result is very different from the very low leakage current (10^{-15} A) of the IP structure that we previously published [15]. Contrary to expectations, the proposed FF structure did not seem to show the low leakage current characteristic of the IGZO channel. Of course, during the normal operation (GSL on) state of WL5, the P-type filler

was connected to the BL contact to which a read voltage of 1 V was applied, not the CSL contact in the GND state as in the IP structure. Therefore, the leakage current generated at this time likely flows through the polysilicon filler. We made this assumption because a leakage current of about 10^{-13} A was observed in the figure, and the value of this leakage current is a typical polysilicon channel leakage current level.



Figure 6. I–V operation results according to gate position.

Operation	Value					
	WL5	Other WLs	GSL	SSL	BL	CSL
WL5	-5 to 5 V	5 V	5 V	5 V	1V	0 V
WL5 (GSL off)	-5 to 5 V	5 V	0 V	5 V	1 V	0 V
GSL	5 V	5 V	-5 to 5 V	5 V	1 V	0 V

Table 3. Applied voltage for the I–V operation shown in Figure 6.

However, the real problem is that the same leakage current was present even when the GSL was is in GND state and was approximately 10^{-8} A when the voltage of WL5 was positive. This suggests that the GSL was not controlling the current of the entire channel. Therefore, we next examined the operation characteristics of the GSL itself, and the results are shown in blue in Figure 6. The operating leakage current of the GSL gate with only an IGZO channel was approximately 10^{-16} A. However, the threshold voltage was located in the negative region (-0.83 V). For this reason, even when the GSL gate was in the GND state, the current flowing through the IGZO channel of the GSL gate had a relatively high value of 10^{-8} A. These results indicate that the high leakage current exhibited during the operation of the WL5 gate was due to the low threshold voltage of the GSL gate.

To solve this problem, a method to move the threshold voltage of the GSL gate to a positive region is required. However, changing the gate material, changing the composition of the material, or changing the material of the gate insulator to achieve this shift could increase process costs. Naturally, as the work function increases, the threshold voltage will move in the positive direction, but with a proportional increase in process cost.

Therefore, we investigated the effects of increasing the number of GSL and SSL gates or increasing the length of the gate itself to reduce the leakage current and increase gate controllability. A low threshold voltage for an IGZO channel is unavoidable because of the material properties of IGZO, which has weak N-type characteristics. Therefore, the change in the work function according to a change in the gate material or insulator material mentioned must be performed in parallel.

Figure 7 shows the changes in operation characteristics according to changes in the work function of GSL in the proposed structure. First, in the proposed structure, a TiN gate with a thickness of 10 nm was used as the GSL gate. The results shown in Figure 7

are for a 100-nm-long GSL gate. A structure with a long gate can be obtained by epitaxial growth of crystal silicon, which was performed for GSL channels when using the bulk erase method prior to COP. Therefore, the above structure cannot be used in the polysilicon channel in the current COP structure, but it is possible to use this structure for an IGZO channel because of the low leakage current characteristics of IGZO channels.



Figure 7. Changes in operating characteristics according to changes in the work function of GSL: (a) results when GSL was on, and (b) results when GSL was off. (c) The graph shown here summarizes leakage current according to the difference in the work function of GSL as shown in (b). (d) Change in the threshold voltage according to the change in the work function of the GSL.

Next, for the range setting of the work function change of the TiN gate, we assumed the work function would change if complex structures with various combinations of TiN or MoN were used. However, changes in the materials and structure can increase the process cost, so in this study, 5.0 eV was set as the limit [20].

Based on the results shown in Figure 7a, the increase in the work function of the GSL gate did not significantly affect the operating characteristics of the V-NAND, especially the on current. This led us to predict that an increase in the work function of the GSL gate would not significantly affect the operation speed of the entire string. Next, as shown in Figure 7b, in which the GSL gate was in the off state, the leakage current rapidly decreased as the work function increased, as expected. Particularly noteworthy is that when the GSL gate work function was increased to 4.96 eV by assuming the gate material combination in the referenced paper or by other processes, the leakage current was only approximately 10^{-15} A. This reflects the unique leakage current characteristics of the IGZO channel. Figure 7c provides a summary of the change in the leakage current according to the change in the work function in Figure 7b. It is clear from this figure that the change in the leakage current corresponding to the change in the work function was almost linear. Therefore, if the work function can be further increased by improving the gate material, the leakage current can likely be further reduced. Finally, the results shown in Figure 7d show the I–V results of the GSL gate itself. As expected, as the work function increased, the threshold

voltage moved in a positive direction by approximately 0.5 V. As a result, the amount of current flowing when the GSL gate voltage was 0 V decreased rapidly and reached 10^{-15} A.

Figure 8 shows the I–V characteristics when multiple GSL gates were used. First, as shown in Figure 8a, using a long GSL gate with a length of 100 nm and using three GSL gates with lengths of 40 nm improved the controllability of the channel. Although the length of the GSL channel doubled, the ratio of the length occupied by the entire string did not increase drastically. In fact, as shown in Figure 8b, the current was similar to that obtained when a single GSL gate with a length of 100 nm was used. There was also no significant difference in the leakage current corresponding to the use of a single long GSL gate or multiple GSL gates. This can be attributed to the large leakage current component generated by the filler adjacent to the IGZO channel when the GSL was on. However, when the GSL gate was in the off state (Figure 8c), the device with multiple gates showed a lower leakage current than the device with a 100-nm-long single GSL gate (Figure 8d). In particular, when a tungsten gate (4.5 eV) was used, the leakage current decreased by 90%, but when a TiN gate (4.66–4.96 eV) was used, there was a relatively uniform reduction in the leakage current of between 65% and 68%.



Figure 8. I–V operation results when multiple GSL gates were used. (**a**) Change in the structure of the GSL gate, and (**b**) I–V operation when this GSL gate was on. (**c**) I–V operation when the GSL was off, and (**d**) changes in leakage current when the GSL was off compared with the previous 100-nm-long GSL gate.

Finally, Figure 9 shows the result of using six GSL gates for the previous leakage current change result. Notably, when the work function of the GSL gate was 4.96 eV, the leakage current could reach the theoretical expected value of 10^{-17} A for IGZO materials. From these results, the proposed FF structure has the theoretical leakage current of the IGZO material because of the composition of the gate material or the combination of the constituent materials along with the change of the structure of the GSL gate, and at the same time, it shows an erasing speed that is more than 1000 times faster than the existing V-NAND structure. Of course, such a leakage current can be achieved through a change in the material composition of the IGZO channel, but in this case, there is a problem of discarding the secured mobility. Therefore, it will be important to optimize the

GSL gate and particularly to establish the optimal number of GSL gates and the channel length in order to secure the maximum mobility and improve the overall operation speed, considering the high mobility and fast erase speed. When this optimization is achieved, the IGZO channel-based FF structure may be an optimal structure that shows a fast erasing speed with a reduction in power consumption due to a low leakage current.



Figure 9. Comparison of the leakage current when the GSL was turned off according to the number of GSL gates, channel length, and the work function of the GSL gate.

4. Conclusions

In this study, we proposed an FF structure with an improved IP structure that has a very fast erase speed in V-NAND based on an IGZO channel demonstrated in previous studies, and we verified the proposed structure through device simulation. The proposed FF structure can supply holes generated through the GIDL phenomenon in the upper polysilicon SSL channel to the IGZO channel through a P-type filler, resulting in a very fast erase speed of 4 μ s. We confirmed that this structure can reduce the leakage current of the entire channel to 10^{-17} A, the theoretical limit value of IGZO material, through various optimization processes (the number of gates, GSL channel length, and work function changes in response to alterations in the gate material) of the lower GSL gate. Our results demonstrate that with the proposed FF structure, a very fast erase speed and low leakage current characteristics can be achieved even in a COP structure.

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