Article

Temperature Dependent Analytical Model for the Threshold Voltage of the SiC VJFET with a Lateral Asymmetric Channel

Sami Ghedira ^{1,*} , Abdelaali Fargi ¹ and Kamel Besbes ^{1,2}

¹ Microelectronics and Instrumentation Laboratory, University of Monastir, Avenue Taher Hadded B.P 56, Monastir 5000, Tunisia; fargi.abdelaali@gmail.com (A.F.); beskamel@gmail.com (K.B.)

² Centre for Research on Microelectronics & Nanotechnology, Sousse Technology Park, BP 334 Sahloul, Sousse 4050, Tunisia

* Correspondence: ghedirasam@yahoo.fr

Abstract: The wide-bandgap (WBG) semiconductor devices for modern power electronics require intensive efforts for the analysis of the critical aspects of their operation. In recent years, silicon carbide (SiC) based field effect transistor have been extensively investigated. Motivated by the significant employment of the SiC Vertical Junction Field Effect transistors with lateral channel (LC-VJFET) in the development of high-voltage and high temperature applications, the properties of the LC-VJFET device are investigated in this work. The most important normally-ON LC-VJFET parameter is their threshold voltage (V_{Th}), which is defined as the gate-to-source voltage necessary to block the device. The higher complexity of the blocking operation of the normally-ON device makes the accurate knowledge of the V_{Th} as a fundamental issue. In this paper, a temperature dependent analytical model for the threshold voltage of the normally-ON LC-VJFET is developed. This analytical model is derived based on a numerical analysis of the electrical potential distribution along the asymmetrical lateral channel in the blocking operation. To validate our model, the analytical results are compared to 2D numerical simulations and experimental results for a wide temperature range.

Keywords: wide bandgap semiconductors; SiC VJFET; threshold voltage; numerical simulations; temperature model

Citation: Ghedira, S.; Fargi, A.; Besbes, K. Temperature Dependent Analytical Model for the Threshold Voltage of the SiC VJFET with a Lateral Asymmetric Channel. *Electronics* **2021**, *10*, 1494. <https://doi.org/10.3390/electronics10121494>

Academic Editor: Fortunato Pezzimenti

Received: 24 May 2021
Accepted: 17 June 2021
Published: 21 June 2021

Publisher's Note: MDPI stays neutral with regard to jurisdictional claims in published maps and institutional affiliations.

Copyright: © 2021 by the authors. Licensee MDPI, Basel, Switzerland. This article is an open access article distributed under the terms and conditions of the Creative Commons Attribution (CC BY) license (<https://creativecommons.org/licenses/by/4.0/>).

1. Introduction

The threshold voltage (V_{Th}) and its dependence on temperature is an important parameter of any FET structure for device evaluation and circuit design. Several works took place in the literature on its modeling for MOSFETs [1–6]. However, there is a lack of similar work for power JFETs structure. During the last decade, wide bandgap devices such as those made of silicon carbide (SiC), have emerged as promising power switching devices for a wide field of advanced electronic applications, especially at high temperature and high voltage. Some of them have been fabricated and tested in various research laboratories, and others are on the market [7–15]. Compared with the SiC MOSFET, SiC VJFET received a lot of attention because of its threshold voltage (V_{th}) stability for different temperature values, since no reliability issues appear with gate oxide on contrary to SiC MOSFETs [5–7]. Different structures of the SiC VJFET device have been developed and studied [16–25]. Among of them, in this paper, the SiC LC-VJFET of Figure 1 [16,20] is investigated under a physical model of the threshold voltage. The SiC LC-VJFET has a normally-on behavior. In other words, it conducts current even if no gate-source voltage is applied. To turn this JFET off, a negative gate-to-source voltage bias should be applied. The main parameter that controls the blockage of the device is the gate-to-source threshold voltage. The blocking condition of the device corresponds to a pinch-off operation where the saturation current reaches zero. Although this condition is very important for the analysis and the modeling of the device, few studies in this context have been published, generally leading to a complex or non-analytical expression of the threshold voltage [26,27].

Figure 1. Structure of the SiC LC-VJFET investigated device.

In a previous work [26], the modeling of the asymmetrical double gate channel of the SiC LC-VJFET structure was investigated. A numerical method has been used to define the blocking conditions of the JFET device. These conditions have been presented by complex functions that are not easy to implement in software to simulate the physical model of the JFET. Therefore, for such complicated SiC LC-VJFET structure, it is a great interest to elaborate an analytical expression of the threshold voltage and its dependence with the temperature. Figure 1 represents the schematic of the investigated device LC-VJFET.

In the present study, an analytical model of threshold voltage for the SiC LC-VJFET is derived. We demonstrate that this model is far from being a classic threshold voltage expression [28]. We will show that the analytical expression of the threshold voltage is simple and easy to use. The proposed model can be used as an efficient tool for design, fabrication and modeling for the SiC VJFET device. The validity of the developed analytical model is investigated by comparing the model results with the experimental and the numerical simulation results within a wide temperature range.

2. Analysis and Modeling of the Asymmetric Lateral Channel of the VJFET

This section concerns the analysis and the modeling of the behavior of the SiC LC-VJFET at blocking operation, which is controlled by the P^+NP^+ lateral channel. Figure 2 shows the lateral channel structure of Figure 1. This lateral channel controls asymmetrically the current in the device that is maintained by the difference in potentials between the two P^+ layers, which are connected to the gate and source terminals, respectively. The asymmetry of the lateral channel does not concern the geometry, which is symmetric, but concerns the control of the channel. So, a model of the current distribution in the asymmetric lateral channel is needed.

Figure 2. Channel structure of the SiC LC-VJFET investigated device.

In [26] the gradual channel approximation is used to derive the current flow in the asymmetrical lateral channel of the JFET. This approximation yields reasonably good results if the channel has a small width and large length and if the carrier mobility can be assumed to be constant and independent of the electric field [28].

Under this approximation, the channel current of the LC-VJFET can be derived analytically and may be expressed as:

$$I_{CH} = q\mu_n N_D Z (2a - W_1(x) - W_2(x)) \frac{dV}{dx} \quad (1)$$

where a is the half of the channel width, Z is the equivalent width of the channel in the perpendicular direction, N_D is the doping density of channel, W_1 and W_2 are the depletion layer widths under Gate 1 and Gate 2, respectively as clearly shown in Figure 2.

The drain current in the linear region is obtained by the integration of Equation (1) along the channel:

$$I_{CH} = \frac{V_P}{3R_{CH}} \times \left\{ \frac{3V_{CH}}{V_P} - V_P^{-3/2} \times \left[(V_{bi} + V_{CH} - V_{G1S})^{3/2} - (V_{bi} - V_{G1S})^{3/2} + (V_{bi} + V_{CH} - V_{G2S})^{3/2} - (V_{bi} - V_{G2S})^{3/2} \right] \right\} \quad (2)$$

where V_{bi} is the built-in voltage and is given by [29]:

$$V_{bi} = \frac{kT}{q} \ln \left(\frac{N_A N_D}{n_i^2(T)} \right) \quad (3)$$

The intrinsic carrier concentration n_i is expressed according to:

$$n_i^2(T) = N_v N_c e^{\frac{E_G(T)}{kT}} \quad (4)$$

where N_v and N_c are the density of states in the valence and conduction bands, respectively, T the absolute temperature, k the constant of Boltzmann and $E_G(T)$ is the energy gap.

The pinch-off voltage V_P and channel resistance R_{CH} are defined as:

$$V_P = \frac{qN_D a^2}{2\epsilon_{SiC}} \quad (5)$$

$$R_{CH} = \frac{L}{2q\mu_n N_D a Z} \quad (6)$$

They have the same expression than in the symmetric channel model. So, for:

$$V_{G1S} = V_{G2S} = V_{GS} \quad (7)$$

We can find the channel current in the symmetric case which is given by [28]:

$$I_{CH}^{sy} = \frac{V_P}{3R_{CH}} \times \left\{ \frac{3V_{CH}}{V_P} - 2V_P^{-3/2} \times \left[(V_{bi} + V_{CH} - V_{GS})^{3/2} - (V_{bi} - V_{GS})^{3/2} \right] \right\} \quad (8)$$

Since the channel voltage V_{CH} is less than the saturation voltage V_{CHSAT} the SiC JFET works in linear region. Beyond this value of saturation, the channel current will be saturated and the SiC JFET works in the saturation region. So, the saturation value is an important parameter, which represents the boundary between linear and saturation regions. This saturation region corresponds to the pinch-off operation which is reached when Equation (9) is valid:

$$W_1(x) + W_2(x) = 2a \quad (9)$$

From Equation (9) the saturation voltage can be determined by taking into account the expressions of depletion layer widths W_1 and W_2 in the case of a uniformly doped channel with doping level N_D :

$$\frac{W_1(x)}{a} = \sqrt{\frac{1}{V_P}(V_{bi} + V_{CH} - V_{G1S})} \quad (10)$$

$$\frac{W_2(x)}{a} = \sqrt{\frac{1}{V_P}(V_{bi} + V_{CH} - V_{G2S})} \quad (11)$$

Assuming that the pinch-off condition is reached for $x = L$. Using (10) and (11), Equation (9) allows to define the saturation voltage:

$$V_{CHSAT} = V_P - V_{bi} + \frac{V_{G1S} + V_{G2S}}{2} + \frac{(V_{G1S} - V_{G2S})^2}{16 V_P}. \quad (12)$$

At this point the saturated drain current I_{CHSAT} can be obtained from Equation (2) by using the standardized voltage values of the saturation voltage, the “Gate 1” to source voltage and the “Gate 2” to source voltage:

$$u_{CHSAT} = \frac{V_{CHSAT}}{V_P} \quad (13)$$

$$\delta_1 = \frac{V_{bi} - V_{G1S}}{V_P} \quad (14)$$

$$\delta_2 = \frac{V_{bi} - V_{G2S}}{V_P} \quad (15)$$

$$I_{CHSAT} = \frac{V_P}{3R_{CH}} \times \left\{ 3u_{CHSAT} - (u_{CHSAT} + \delta_1)^{3/2} - (u_{CHSAT} + \delta_2)^{3/2} + \delta_1^{3/2} + \delta_2^{3/2} \right\} \quad (16)$$

The saturated drain current can be calculated from this equation by substituting the drain voltage at pinch-off with Equation (12):

$$I_{CHSAT} = \frac{V_P}{3R_{CH}} \Gamma(\delta_1, \delta_2) \quad (17)$$

with:

$$\Gamma(\delta_1, \delta_2) = 3u_{CHSAT} - \left(1 + \frac{(\delta_2 - \delta_1)^2}{16} - \frac{\delta_2 - \delta_1}{2} \right)^{3/2} - \left(1 + \frac{(\delta_2 - \delta_1)^2}{16} + \frac{\delta_2 - \delta_1}{2} \right)^{3/2} + \delta_1^{3/2} + \delta_2^{3/2} \quad (18)$$

In the symmetric case, $\delta_1 = \delta_2 = \delta$ and Equation (17) becomes:

$$I_{CHSAT}^{Sy}(\delta) = \frac{V_P}{3R_{CH}} \times \left\{ 1 - 3\delta + 2\delta^{3/2} \right\} \quad (19)$$

which is the classical saturation current for the symmetric JFET channel. In the blocking region:

$$V_{CHSAT}^{sy} = V_P - V_{bi} + V_{GS} \leq 0 \quad (20)$$

the channel current is zero, in particular for $\delta = 1$. Therefore, in the symmetric case, the classical condition of the blocking operation is expressed in the form of:

$$V_{GS} \leq V_{Th} = V_{bi} - V_P \quad (21)$$

where V_{Th} is the classical threshold voltage. It is defined as the gate-to-source voltage value at which the saturation current becomes zero, ($I_{CHSAT}^{Sy}(V_{Th}) = 0$).

However, it is much more complicated to find a simple threshold voltage model for asymmetric JFET channel. So, a numerical method can be adopted for solving the Equation (17). Figure 3 shows the plot of the $\Gamma(\delta_1, \delta_2)$ function.

Figure 3. Function that presents regular and positive function.

Figure 4, which is extracted from Figure 3 shows the curve Γ_0 which correspond to the pinch-off operation where the saturation current becomes null and satisfies this condition: $\Gamma(\delta_1, \delta_2)$ reaches to:

$$\Gamma(\delta_1^0, \delta_2^0) = 0 \quad (22)$$

where:

$$\delta_1^0 = \frac{V_{bi} - V_{GS}}{V_P} \quad (23)$$

Figure 4. Numerical Solution of Γ_0 function extracted from Figure 3.

In addition:

$$\delta_2^0 = \delta = \frac{V_{bi}}{V_P} \quad (24)$$

Therefore, from the graphical representation of Figure 5 a relation between δ_1^0 and δ_2^0 can be implicitly given by:

$$\delta_1^0 = \Gamma_0(\delta) \quad (25)$$

which correspond to a blocking operation where the gate-to-source voltage reaches the threshold voltage value. At the blocking threshold $V_{GS} = V_{Th}$ and Equation (23) may be rewritten as:

$$\delta_1^0 = \frac{V_{bi} - V_{Th}}{V_P} \quad (26)$$

which gives an implicitly expression of the threshold voltage:

$$V_{Th} = V_{bi} - V_P \Gamma_0 \left(\frac{V_{bi}}{V_P} \right) \quad (27)$$

Figure 5. 2D numerical simulation of the device showing the overlap of the space charge regions 1 and 2.

This expression is based on a graphical representation which making it difficult to introduce in the circuit simulator, so an analytical threshold voltage model is needed.

3. Threshold Voltage Model and Validation

In this section we proceed to develop the threshold voltage model based on the analysis of the potential distribution, ϕ , inside the lateral channel. To simplify the analysis, the gradual channel approximation is used to obtain a simple electric potential expression by solving the 1-D Poisson's equation along the y-direction from the top gate "Gate 1" to the bottom gate "Gate 1".

The 1-D Poisson equation can be written as [30]:

$$\frac{\partial^2 \phi}{\partial y^2} = -\frac{qN_D}{\epsilon_{SiC}} \quad (28)$$

using the following boundary conditions:

$$\phi(0) = V_{G1S} \quad (29)$$

$$\phi(2a) = 0 \quad (30)$$

and assuming that at $y = y_m$ which is the maximum value of y when:

$$-\frac{\partial \phi}{\partial y} = E = 0 \quad (31)$$

In addition:

$$\phi = \phi_m \quad (32)$$

in the case of a uniformly doped channel with doping level N_D , an expression for the electrical potential is obtained:

$$\phi(y) = \phi_m - v_P \left(\frac{y - y_m}{a} \right)^2 \quad (33)$$

using (29) and (30) conditions we would acquire:

$$V_{G1S} = V_{GS} = \phi_m - v_P \left(\frac{y_m}{a} \right)^2 \quad (34)$$

In addition:

$$\phi_m = V_P \left(2 - \frac{y_m}{a} \right)^2 \quad (35)$$

substituting ϕ_m in (34) we obtain the expression for the depletion width value as function of the applied voltage V_{GS} :

$$y_m = a \times \left(1 - \frac{V_{GS}}{4V_P} \right) \quad (36)$$

using (36), Equation (35) can be rewritten in the form of:

$$\phi_m = \phi(y_m) = V_P \times \left(1 + \frac{V_{GS}}{4V_P} \right)^2 \quad (37)$$

By substituting Equations (36) and (37) in Equation (33), the expression for the electric potential is obtained as follows:

$$\phi(y) = V_{GS} - V_P \times \left(\frac{y^2}{a^2} + \frac{2y}{a} \left(\frac{V_{GS}}{4V_P} - 1 \right) \right) \quad (38)$$

which represents the variation of the electric potential as function of the applied voltage V_{GS} .

The electrical potential evolution in the lateral channel under the blocking condition is analyzed by using a 2D TCAD physical simulator [31]. This analysis is based on many simulations by changing the parameters of the lateral channel (half width of the lateral channel “a” and the doping level “ N_D ”). By considering the gradual channel approximation, the length L of the lateral channel was taken bigger than its width. The other typical parameters were taken from [25]. Referring to Figure 1, Table 1 summarizes the values of the doping concentrations and geometrical parameters used in this numerical simulation.

Table 1. Geometrical and Doping parameters values used in the simulations.

Symbol	Definition	Value
a	Half width of the lateral channel	0.72 μm
L	Length of the lateral channel	6 μm
N_D	Doping level in the lateral channel	$2.4 \times 10^{16} \text{ cm}^{-3}$
N_A	Dopping in the gate	$1 \times 10^{18} \text{ cm}^{-3}$
W	Thickness of the epilayer	15 μm
N_{DD}	Doping level in the epilayer	$5 \times 10^{15} \text{ cm}^{-3}$
h	Width of the vertical channel	0.7 μm
b	Length of the vertical channel	2.6 μm

The numerical simulation results are presented in Figures 5 and 6, which show that the electrical potential reaches its maximum ϕ_m at the point y_m where the two space charge regions coincide. The first space charge region (SCR1) corresponds to the spreading of

depletion layer under the top gate to achieve the width y_m when the applied gate-source voltage becomes equal to the threshold gate voltage, which is given by:

$$y_m = 2a - \omega_0 \quad (39)$$

where ω_0 is the depletion-layer width of the second space charge region (SCR2) caused by the built-in potential (V_{bi}) when no voltage is applied to the bottom gate abrupt junction. Therefore, substituting (39) in (35), we obtain:

$$\phi_m = V_P \left(2 - \frac{2a - \omega_0}{a} \right)^2 = V_P \left(\frac{\omega_0}{a} \right)^2 = \frac{qN_D}{2\epsilon_{SiC}} \omega_0^2 \quad (40)$$

which corresponds well to the built-in potential (V_{bi}) producing the depletion layer given by [30]:

$$\omega_0 = \sqrt{\frac{2\epsilon_{SiC}}{qN_D} V_{bi}} \quad (41)$$

Figure 6. Numerical simulation of the electric Potential distribution along the lateral channel of the SiC LC-VJFET structure.

A vertical cut from “Gate 1” to “Gate 2” has been accomplished on Figure 5 and from this cut we obtained the electric potential distribution along the channel of the SiC LC-VJFET structure and is illustrated in Figure 6.

Furthermore, as illustrated in Figure 6 when V_{GS} reaches V_{Th} , the electrical potential ϕ_m reaches V_{bi} and Equation (37) can be rewritten in the form of:

$$V_{bi} = V_P \times \left(1 + \frac{V_{Th}}{4V_P} \right)^2 \quad (42)$$

which yields to the following expression:

$$V_{Th} = V_{bi} - V_P \left(2 - \sqrt{\frac{V_{bi}}{V_P}} \right)^2 \quad (43)$$

Equation (43) represents the new model of threshold voltage which corresponds to the same expression (27) cited above when:

$$\Gamma_0(\delta) = (2 - \sqrt{\delta})^2 \quad (44)$$

This result is validated and shown in Figure 7. We obtained a good agreement between analytical expression given in Equation (44) and the numerical solution of Γ_0 function given in Figure 4.

Figure 7. Comparison of Analytical and Numerical solutions of $\Gamma_0(\delta)$ function.

So, we have developed a novel approach of the asymmetrical threshold voltage channel different from the standard JFET model given by the classical expression:

$$V_{Th} = V_{bi} - V_P \quad (45)$$

Figure 8 demonstrates the calculated values of the threshold voltage model compared with the experimental results for a wide temperature range. The experimental data as well as the pinch-off voltage and the lateral channel doping concentration used in the calculation of the threshold voltage model are reported in [27] and are given by:

$$V_P = 7.29 \text{ V and } N_D = 1.64 \times 10^{16} \text{ cm}^{-3} \quad (46)$$

Figure 8. Comparison of the threshold voltage model with Experimental values over a wide range of Temperature.

It is seen from the figure an excellent agreement between the model and experimental results is observed. This confirms the validity of the suggested threshold voltage model. It is also clear that there is a big difference between the standard model of threshold voltage (given by Equation (45)) and the analytical model results, thus cannot describe well enough the behavior of threshold voltage of the studied device.

Figure 9 depicts the dependence of threshold voltage versus the Pinch-off voltage using the proposed model for two different built-in voltages.

Figure 9. Graphical representation of threshold voltage model versus the Pinch-off voltage for two different values of V_{bi} .

Since it is too difficult to determine the V_p value directly from the analytical model which is presented as an implicit expression, Figure 9 serves as a chart tool for parameter extraction. Knowing its threshold voltage experimentally, one can easily extract the pinch-off voltage value and then estimate geometric and doping parameters of the device.

4. Conclusions

This paper focuses essentially on the physical analysis of the behavior of the SiC LC-VJFET with lateral channel in the blocking mode. The difficulty posed by this device is that the blockage is controlled asymmetrically by the lateral channel. The asymmetry concerns the difference of the applied gate voltages between the two P^+ layers and not the geometry of the channel structure which is symmetric. The blocking condition of the power device has not been previously solved correctly. To address this problem, this work was investigated to accurately propose an analytical model of the gate to source threshold voltage which is a main parameter that controls the blockage of the device.

So, a temperature dependent analytical model for the threshold voltage of the power device SiC LC-VJFET has been derived under two steps: Firstly, numerical method has been adopted to solve the saturation current which allows to a graphical solution of the blocking condition. Secondly, a physical analysis of the electric potential distribution in the asymmetric side-channel blocking condition leads to an analytical solution which was validated regarding the graphical solution and numerical simulation. The model is compared with experimental data for a wide temperature range. Good agreement has been observed demonstrating the accuracy of the proposed model.

Author Contributions: Modelling and simulation, S.G. and A.F.; writing—original draft preparation, S.G.; writing—review and analysis, S.G. and A.F.; review and editing, S.G. and K.B. All authors have read and agreed to the published version of the manuscript.

Funding: This research received no external funding.

Conflicts of Interest: The authors declare no conflict of interest.

References

- Ortiz-Conde, A.; García Sánchez, F.J.; Liou, J.J.; Cerdeira, A.; Estrada, M.; Yue, Y. A review of recent MOSFET threshold voltage extraction methods. *Microelectron. Reliab.* **2002**, *42*, 583–596. [\[CrossRef\]](#)
- Tsormpatzoglou, A.; Tassis, D.H.; Dimitriadis, C.A.; Ghibaudo, G.; Collaert, N.; Pananakakis, G. Analytical threshold voltage model for lightly doped short-channel tri-gate MOSFETs. *Solid-State Electron.* **2011**, *57*, 31–34. [\[CrossRef\]](#)
- Tsormpatzoglou, A.; Pappas, I.; Tassis, D.H.; Dimitriadis, C.A.; Ghibaudo, G. Analytical threshold voltage model for short-channel asymmetrical dual-gate material double-gate MOSFETs. *Microelectron. Eng.* **2012**, *90*, 9–11. [\[CrossRef\]](#)
- Ortiz-Conde, A.; García-Sánchez, F.J.; Muci, J.; Terán Barrios, A.; Liou, J.J.; Ho, C.-S. Revisiting MOSFET threshold voltage extraction methods. *Microelectron. Reliab.* **2013**, *53*, 90–104. [\[CrossRef\]](#)
- Aichinger, T.; Rescher, G.; Pobegen, G. Threshold voltage peculiarities and bias temperature instabilities of SiC MOSFETs. *Microelectron. Reliab.* **2018**, *80*, 68–78. [\[CrossRef\]](#)
- Guevara, E.; Herrera-Pérez, V.; Rocha, C.; Guerrero, K. Threshold Voltage Degradation for n-Channel 4H-SiC Power MOSFETs. *J. Low Power Electron. Appl.* **2020**, *10*, 3. [\[CrossRef\]](#)
- Friedrichs, P.; Stephani, D. Unipolar SiC power devices and elevated temperature. *Microelectron. Eng.* **2006**, *83*, 181–184. [\[CrossRef\]](#)
- Gachovska, T.K.; Hudgins, J.L. 5-SiC and GaN Power Semiconductor Devices. In *Power Electronics Handbook*, 4th ed.; Rashid, M.H., Ed.; Butterworth-Heinemann: Oxford, UK, 2018; pp. 95–155.
- Ji, D.; Chowdhury, S. Design of 1.2 kV Power Switches with Low R_{ON} Using GaN-Based Vertical JFET. *IEEE Trans. Electron. Devices* **2015**, *62*, 2571–2578. [\[CrossRef\]](#)
- Kaneko, M.; Kimoto, T. High-Temperature Operation of n- and p-Channel JFETs Fabricated by Ion Implantation into a High-Purity Semi-Insulating SiC Substrate. *IEEE Electron. Device Lett.* **2018**, *39*, 723–726. [\[CrossRef\]](#)
- Huang, H.; Li, F.; Sun, Z.; Sun, N.; Zhang, F.; Cao, Y.; Zhang, H.; Tao, P. Gallium Nitride Normally-Off Vertical Field-Effect Transistor Featuring an Additional Back Current Blocking Layer Structure. *Electronics* **2019**, *8*, 241. [\[CrossRef\]](#)
- Barbagallo, C.; Rizzo, S.A.; Scelba, G.; Scarcella, G.; Cacciato, M. On the Lifetime Estimation of SiC Power MOSFETs for Motor Drive Applications. *Electronics* **2021**, *10*, 324. [\[CrossRef\]](#)
- Kizilyalli, I.C.; Aktas, O. Characterization of vertical GaN p-n diodes and junction field-effect transistors on bulk GaN down to cryogenic temperatures. *Semicond. Sci. Technol.* **2015**, *30*, 124001. [\[CrossRef\]](#)
- Li, H.; Liao, X.; Hu, Y.; Huang, Z.; Wang, K. Analysis of Voltage Variation in Silicon Carbide MOSFETs during Turn-On and Turn-Off. *Energies* **2017**, *10*, 1456. [\[CrossRef\]](#)
- Alonso, A.R.; Díaz, M.F.; Lamar, D.G.; Azpeitia, M.A.P.d.; Hernando, M.M.; Sebastián, J. Switching Performance Comparison of the SiC JFET and SiC JFET/Si MOSFET Cascode Configuration. *IEEE Trans. Power Electron.* **2014**, *29*, 2428–2440. [\[CrossRef\]](#)
- Elpelt, R.; Friedrichs, P.; Biela, J. Fast Switching with SiC VJFETs-Influence of the Device Topology. *Mater. Sci. Forum* **2010**, *645–648*, 933–936. [\[CrossRef\]](#)
- Veliadis, V. Silicon Carbide Junction Field-Effect Transistors (SiC JFETs). In *Wiley Encyclopedia of Electrical and Electronics Engineering*; John Wiley & Sons: Linthicum, MD, USA, 2014; pp. 1–37.
- Neudeck, P.G.; Spry, D.J.; Chen, L.Y. Experimental and Theoretical Study of 4H-SiC JFET Threshold Voltage Body Bias Effect from 25 °C to 500 °C. *Mater. Sci. Forum* **2016**, *858*, 903–907. [\[CrossRef\]](#)
- Kayambaki, M.; Makris, N.; Stavrinidis, A.; Konstantinidis, G.; Zekentes, K. On the Optimum Determination and Use of SiC VJFET Threshold Voltage. *Mater. Sci. Forum* **2018**, *924*, 657–660. [\[CrossRef\]](#)
- Asllani, B.; Bevilacqua, P.; Zaoui, A.; Grosset, G.; Planson, D.; Morel, H. High-Voltage SiC-JFET Fabrication and Full Characterization. *Mater. Sci. Forum* **2019**, *963*, 688–692. [\[CrossRef\]](#)
- Fernández-Martínez, P.; Flores, D.; Hidalgo, S.; Jordà, X.; Perpiñà, X.; Quirion, D.; Ré, L.; Ullán, M.; Vellvehí, M. A New Vertical JFET Power Device for Harsh Radiation Environments. *Energies* **2017**, *10*, 256. [\[CrossRef\]](#)
- Bargiel, K.; Bisewski, D.; Zarębski, J. Modelling of Dynamic Properties of Silicon Carbide Junction Field-Effect Transistors (JFETs). *Energies* **2020**, *13*, 187. [\[CrossRef\]](#)
- Zhang, Y.; Tang, M.; Song, Q.; Tang, X.; Lv, H.; Liu, S. High temperature characterization of normally-on 4H-SiC junction field-effect transistor. *Superlattices Microstruct.* **2016**, *99*, 113–117. [\[CrossRef\]](#)
- Grekov, A.E.; Chen, Z.; Fu, R.; Hudgins, J.L.; Mantooth, H.A.; Sheridan, D.C.; Casady, J.; Santi, E. Parameter Extraction Procedure for Vertical SiC Power JFET. *IEEE Trans. Ind. Appl.* **2011**, *47*, 1862–1871. [\[CrossRef\]](#)
- Ghedira, S.; Buttay, C.; Morel, H.; Besbes, K. Measurement and numerical analysis of C-V characteristics for normally-on SiCED-JFET. *Eur. Phys. J. Appl. Phys.* **2014**, *66*, 20103. [\[CrossRef\]](#)

-
26. Hervé, M.; Youness, H.; Dominique, T.; Rémi, R.; Fabien, D.; Damien, R.; Christian, M.; Dominique, B.; Cyril, B.; Régis, M. A multi-physics model of the VJFET with a lateral channel. In Proceedings of the 2011 14th European Conference on Power Electronics and Applications, Birmingham, UK, 30 August–1 September 2011; pp. 1–10.
 27. Dubois, F.; Bergogne, D.; Tournier, D.; Buttay, C.; Meuret, R.; Morel, H. Analysis of the SiC VJFET gate punch-through and its dependence with the temperature. In Proceedings of the 2013 15th European Conference on Power Electronics and Applications (EPE), Lille, France, 2–6 September 2013; pp. 1–10.
 28. Baliga, B.J. *Modern Power Devices*; Wiley: Hoboken, NJ, USA, 1987.
 29. Baliga, B.J. *Fundamentals of Power Semiconductor Devices*; Springer International Publishing: Berlin/Heidelberg, Germany, 2018.
 30. Sze, S.M.; Lee, M.K. *Semiconductor Devices: Physics and Technology*; John Wiley & Sons: New York, NY, USA, 2013.
 31. Synopsys. *Sentaurus Device User Guide*, Version F-2011.09 ed.; Synopsys: Mountain View, CA, USA, 2011.