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# Study on Multiple Input Asymmetric Boost Converters with Simultaneous and Sequential Triggering

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**Abstract:** Paralleled boost asymmetric configurations operating in discontinuous conduction mode (DCM) are suitable for integrating dissimilar green energy generating sources and control algorithms in versatile scenarios where voltage step-up, low cost, stable operation, low output ripple, uncomplicated design, and acceptable efficiency are needed. Unfortunately, research has mainly been conducted on the buck, sepic, switched-capacitor, among other asymmetric configurations operating in continuous conduction mode (CCM), to the authors' knowledge. For asymmetric boost type topologies, achieving simultaneous CCM is not a trivial task, and other problems such as circulating currents arise. Research for interleaved converters cannot be easily extended to asymmetric boost topologies due to the dissimilarity of control algorithms and types of sources and parallel stages. This paper analytically establishes properties of stability, output ripple, output voltage, and design for asymmetrical paralleled boost converters operating in DCM with simultaneous or phase delayed (sequential) triggering. A 300 W experimental design and the respective tests allow validation of such properties, resulting in an easy-to-implement configuration with acceptable efficiency.

**Keywords:** asymmetric converter; multiple-input converter; parallel boost; discontinuous conduction mode; simultaneous triggering; sequential triggering



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## 1. Introduction

Wind generators, photovoltaic modules (PVM), fuel cells (FC), storage systems (batteries), and many other energy sources should be integrated into green power distributed generation plants (hybrid sources) [1–4] and modern smart grids [5–8]. If any energy sources cannot provide energy, the rest could satisfy the customers' energy demand as a multiple uninterrupted power supply.

Smart grids require higher voltage levels (enough to convert to 120/220 VAC) than those provided by energy sources such as PVM or FC. For example, outstanding research was aimed to obtain very high gain and efficiency levels for a single source by combining switched-capacitor and sepic stages [9] or new interleaved boost configurations [10]. Several investigations on interleaved-type converters proposed models and control schemes based on phase-shifted triggering for multiple stages and a single source; these would allow for a power increase, decrease input and output distortions (ripple), and even mitigate nonlinear bifurcation phenomena [11–18].

However, the integration of several different energy sources by power electronic converters (PEC) is necessary but presents complications (recirculating currents, harmonics,

high ripple, degradation phenomena, among others) to match the grid impedance, mainly due to the dissimilarity in power capacities. Even the series interconnection of several power sources of the same type creates undesirable effects—for instance, the well-known potential-induced degradation of PVM due to their series interconnection [19].

Parallel multiple input PEC with boost stages operating in DCM are still promising configurations for a scenario of hybrid sources combining MPPT with other algorithms due to their simplicity, low cost, and acceptable efficiency for high voltage gains. CCM implies high-capacity, costly, and voluminous inductors and cannot be ensured for all power-demand regimes [20]. In discontinuous conduction mode (DCM), the converter efficiency is always higher than in CCM [21,22]. Unfortunately, most research on asymmetric paralleled topologies has been devoted to more complicated configurations, which have a higher cost or a low gain, such as sepic, buck-boost, and their variants and combinations operating in CCM, or consider few inputs, among other disadvantages [23].

In [24], the authors analyzed two buck, boost, and buck-boost paralleled, and asymmetrical stages operating in CCM; ripple and output voltage estimations were presented, and a small-signal model was developed to design an output voltage controller by an average current-mode approach. Unfortunately, for green energy sources, Maximum Power Point Tracking (MPPT) controllers are regularly used for more than two stages. The authors in [25,26] proposed single-inductor converters with $n$ inputs and $m$ outputs, and a complete analysis of ripple and output voltages; however, since the inputs must be order-connected by their voltage level, this converter is not suitable for hybrid sources requiring MPPT and other algorithms. In [27–31], the authors presented a voltage accumulator with $n$ inputs and a switched diode-capacitor voltage accumulator on conventional boost converters and included steady-state analyzes; however, many capacitors/components decrease reliability, and MPPT is not achieved. The authors in [32] proposed a single-inductor, asymmetric, boost type, two-input converter to operate multiple MPPT via a sequential triggering; although they presented a circuit design methodology, stability was not ensured for combining other control algorithms or power source types. Furthermore, the single inductor must be of considerable capacity, cost, and dimensions, in addition to withstanding high stress in CCM. A paralleled boost asymmetric configuration combined with a buck topology was presented in [33]; although the configuration can be easily extended to $n$ boost stages, the authors do not guarantee the simultaneous and independent operation of the hybrid sources and presented only basic analyzes for CCM.

The authors in [34] presented a parallel multiple-input PEC with boost stages operating in CCM to feed an h-bridge inverter configuration and included a design analysis; although the controllers were independent for all of the PVM, the authors solved the boost-stages equalization problem by integrating two additional MOSFETS per stage to achieve the decoupling, increasing monetary and computational costs and decreasing efficiency. In [35], the authors analyzed the symmetric configuration of boost interleaved and paralleled stages in CCM to combine FC and PVM. Unfortunately, the authors considered equal stages and similar input voltage levels, simplifying the formulations considerably. Neither did they consider combining different algorithms and MPPT, nor was a stability analysis performed; hence, this work cannot be extended to asymmetric configurations. The authors in [36], presented an asymmetric configuration of $n$ boost paralleled stages operating in CCM with simultaneous triggering and equal duty-cycle; the authors only presented a basic formulation for the output voltage. In [37], the authors presented an analysis of two interleaved converters of two stages connected in parallel and with a 180-degree phase-shift for the stages (sequential triggering). Steady-state analysis was provided for operation in CCM. Unfortunately, the study was limited to two power supplies with two inductors and two switches per source; furthermore, the CCM has the same disadvantages as the previous proposals.

Other modified/new architectures for two (hybrid) sources can be consulted in [38–44], to mention only a few.

Some interesting adverse effects of uncontrolled and arbitrary phase-delay triggering in paralleled stages with a final diode (as the case of boost topologies), were numerically shown in [45]; however, the benefit of a sequential triggering over the input/output current ripple reduction is well known [46,47]. Regardless of the above, no analytical research has been conducted on the benefits of a sequential triggering (with phase delay instead simultaneous) for paralleled boost converters operating in DCM for $n$ stages and controllers, to the authors' knowledge. Neither was any study found on the combination of MPPT algorithms for some sources, with other control strategies for different sources, for boost paralleled converters.

Hence, from the review above, the found research cannot be easily extended or modified to the design of multiple-input converters, with $n$ asymmetric boost stages, operating in DCM and sequential or simultaneous triggering. This paper presents the following contributions:

- An output voltage stability analysis for an $n$ paralleled boost stages converter operation with MPPT control combined with other controllers.
- Formulations for the steady-state voltage gain and the output voltage ripple.
- An approach to design an easy-to-implement, versatile, and stable boost-type paralleled MIC with $n$ unequal stages and sources and independent controllers (MPPT/other). This strategy allows different energy sources to feed a resistive load and decouple the paralleled boost stages without extra components, avoiding circulating currents with a low-cost implementation. The output voltage and current ripples are diminished in comparison with simultaneous triggering schemes; an experimental exemplification of the MIC design is provided.

With these objectives in mind, this document is organized as follows. Section 2 presents the MIC setup and dynamic modeling from a switched-systems perspective. The analysis ensures stability regardless of whether multiple MPPT controllers are combined with other strategies. In Section 3, the steady-state analysis to determine the averaged and ripple output voltage levels for sequential triggering are presented, and the ripple concerning simultaneous triggering is compared. Section 4 is aimed at the design of the MIC and the experimental platform. Sections 5 and 6 present numerical and experimental validations of the models and, finally, Section 7 is dedicated to providing some discussion, conclusions, and future work.

## 2. Paralleled-Boost-Converter, Dynamic Modeling, and Stability

Let us begin by recalling the boost converter large-signal analysis, which is regularly used in the literature [20,48,49]. This analysis can be extended to $n$ asymmetric boost stages connected in parallel to study the MIC configuration shown in Figure 1a. For sequential or phase-delayed triggering, the activations of MOSFETs/switches are ordered and evenly distributed within every operation period $T_s$, of a pulse width modulator (PWM). To be precise, sequential triggering means that the $Q_i$-th MOSFET is deactivated (off-state) $T_s/n$ seconds after the $Q_{i-1}$ switch was deactivated, and the first MOSFET is deactivated $T_s/n$ seconds after the $n$-th MOSFET ($n$ is the number of stages); activation-timing must be calculated on this time base (see Figure 1b) with $u_{i,1} \leq 1/n$ where $u_{i,1}$ is the duty-cycle of the $i$-th stage. Only a single switch is activated at a time, and the next switch is activated when the previous has been deactivated; this allows simultaneous energy charge of inductors to be avoided. On the other hand, while the first switch is deactivated, the stored energy flows towards the load until it is discharged. Within this period, two scenarios are possible: another single switch can be activated to charge the next inductor, or all switches remain deactivated until another switch should be activated. In other words, for the sequential triggering proposed in this paper, the simultaneous charge of two or more inductors is not allowed, nor is the simultaneous discharge of two or more inductors allowed; this is because additional harmonics are introduced (currents through the diodes are summed within $T_S/n$, and the ripple stops having a triangular shape).

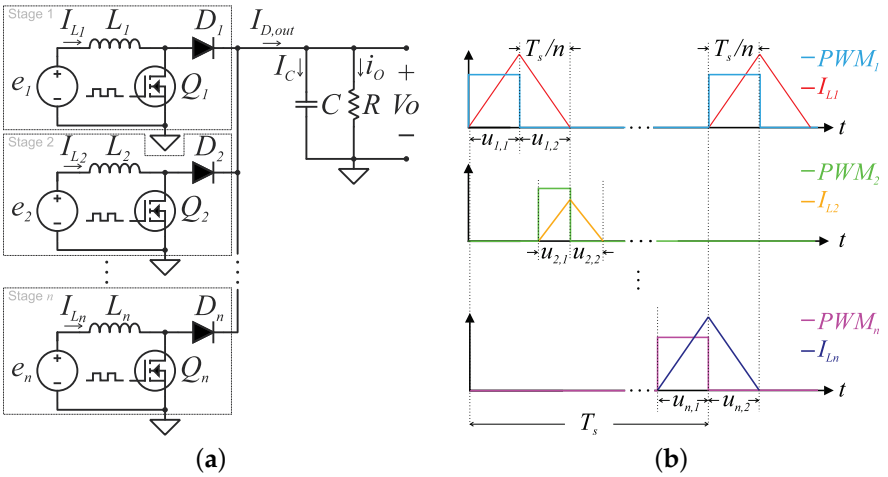



**Figure 1.** Schematic and triggering of the boost type, multiple-input converter proposed in this paper. (**a**) Schematic of the MIC; the converter can include $n$ boost stages. (**b**) Timeline for illustration of the sequential triggering. Squared signals represent PWM triggering; triangle waves represent the currents going through the inductors. $PWM_1$ and $PWM_n$ are illustrated with maximum duty-cycles $(1/n)$ while for $PWM_2$ is lesser; hence, every PWM can operate independently. Only a single inductor discharge is allowed at a time; simultaneously, at most, a single inductor is allowed to charge.

Table 1 illustrates the allowed operation modes of the MIC with two stages, including their corresponding dynamic equations; note that the quantity of modes depends on the number of stages, but only subindexes in equations change and can be easily extended to $n > 2$. The gray lines in the schematics indicate no current flow, while black lines mean a current flow. Figure 2 shows an exemplification of the sequential triggering for the two stages MIC and the obtained mode sequence. Note that such a sequence depends on the duty cycles, but simultaneous charge and discharge of inductors are avoided.

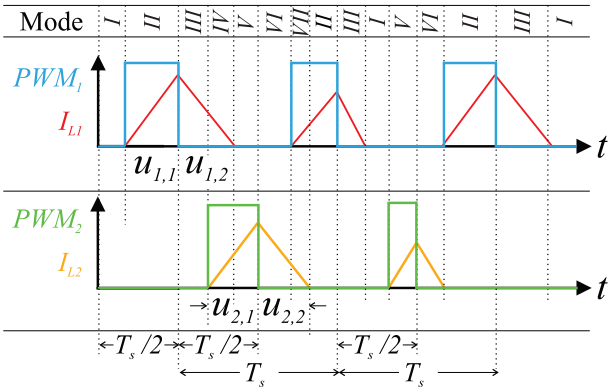
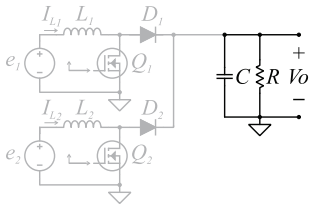
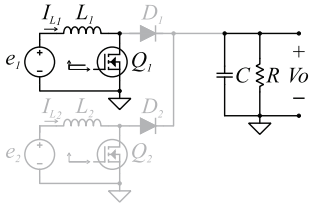
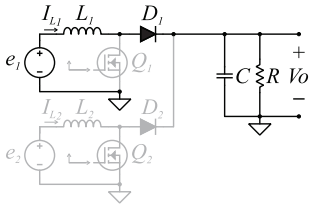
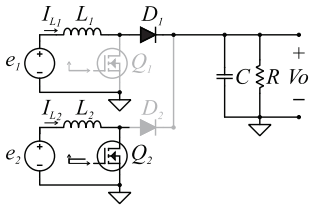
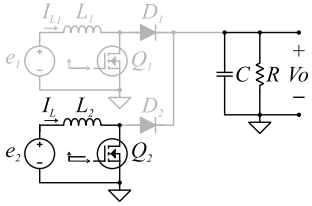
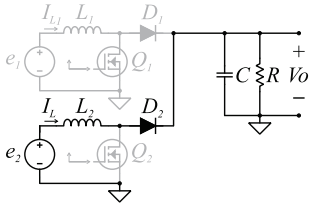
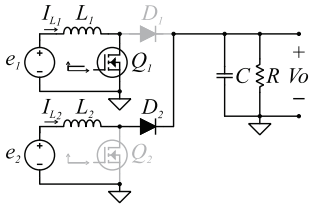



**Figure 2.** Exemplification of two stages MIC sequential triggering-timeline and operating modes. Charging periods are alternated. A charge and discharge of inductors can occur simultaneously, depending on the duty cycles; hence, one of the seven dynamic operating modes shown in Table 1 is possible with two stages. The sequential triggering and proper component selection (see Section 4) exclude other modes for dual charge/discharge.

**Table 1.** Exemplification of the Allowed Operating Modes for Sequential Triggering in a Two Stages MIC.

| Mode | Current Flow Schematic | Inductors Currents | Output Voltage |
|---|---|---|---|
| *I* |  | $\frac{dI_{L_1}}{dt} = 0$<br>$\frac{dI_{L_2}}{dt} = 0$ | $\frac{dV_o}{dt} = -\frac{V_o}{RC}$ |
| *II* |  | $\frac{dI_{L_1}}{dt} = \frac{e_1}{L_1}$<br>$\frac{dI_{L_2}}{dt} = 0$ | $\frac{dV_o}{dt} = -\frac{V_o}{RC}$ |
| *III* |  | $\frac{dI_{L_1}}{dt} = \frac{e_1 - V_o}{L_1}$<br>$\frac{dI_{L_2}}{dt} = 0$ | $\frac{dV_o}{dt} = \frac{I_{L_1}}{C} - \frac{V_o}{RC}$ |
| *IV* |  | $\frac{dI_{L_1}}{dt} = \frac{e_1 - V_o}{L_1}$<br>$\frac{dI_{L_2}}{dt} = \frac{e_2}{L_2}$ | $\frac{dV_o}{dt} = \frac{I_{L_1}}{C} - \frac{V_o}{RC}$ |
| *V* |  | $\frac{dI_{L_1}}{dt} = 0$<br>$\frac{dI_{L_2}}{dt} = \frac{e_2}{L_2}$ | $\frac{dV_o}{dt} = -\frac{V_o}{RC}$ |
| *VI* |  | $\frac{dI_{L_1}}{dt} = 0$<br>$\frac{dI_{L_2}}{dt} = \frac{e_2 - V_o}{L_2}$ | $\frac{dV_o}{dt} = \frac{I_{L_2}}{C} - \frac{V_o}{RC}$ |
| *VII* |  | $\frac{dI_{L_1}}{dt} = \frac{e_1}{L_1}$<br>$\frac{dI_{L_2}}{dt} = \frac{e_2 - V_o}{L_2}$ | $\frac{dV_o}{dt} = \frac{I_{L_2}}{C} - \frac{V_o}{RC}$ |

From a switched-systems perspective, considering that the duty cycle for any stage is $0 \leq D_i < 1/n$ where $i = 1, 2, ..., n$ and differentiating the voltage equations in each mode (one looks only for the output voltage dynamic behavior), one can get the following switched system (arbitrary switching) from Table 1 equations:

$$\dot{x} = A_i x + B_i \tag{1}$$

where $x = [x_1, x_2]^T = \left[V_o, \dot{V}_o\right]$, $i = 1, 2, ..., n+1$, and

$$A_1 = \begin{bmatrix} 0 & 1 \\ -\frac{1}{L_1 C} & -\frac{1}{RC} \end{bmatrix}, A_2 = \begin{bmatrix} 0 & 1 \\ -\frac{1}{L_2 C} & -\frac{1}{RC} \end{bmatrix}, ...,$$
$$A_n = \begin{bmatrix} 0 & 1 \\ -\frac{1}{L_n C} & -\frac{1}{RC} \end{bmatrix}, A_{n+1} = \begin{bmatrix} 0 & 1 \\ 0 & -\frac{1}{RC} \end{bmatrix},$$
$$B_1 = \begin{bmatrix} 0 \\ \frac{e_1}{L_1 C} \end{bmatrix}, B_2 = \begin{bmatrix} 0 \\ \frac{e_2}{L_2 C} \end{bmatrix}, ..., B_n = \begin{bmatrix} 0 \\ \frac{e_n}{L_n C} \end{bmatrix}, B_{n+1} = \begin{bmatrix} 0 \\ 0 \end{bmatrix}.$$

Since the dynamic (qualitative) behavior of each autonomous subsystem is invariant to shifts in the equilibrium point [50], one can propose $n$ coordinate changes $y = x - x_e$ where $x_e$ is the respective equilibrium point (abusing notation):

$$\dot{y} = \mathcal{A}_i y \tag{2}$$

where

$$\mathcal{A}_1 = \begin{bmatrix} 0 & 1 \\ -\frac{\rho}{L_1 C} & -\frac{1}{RC} \end{bmatrix}, \mathcal{A}_2 = \begin{bmatrix} 0 & 1 \\ -\frac{\rho}{L_2 C} & -\frac{1}{RC} \end{bmatrix}, ..., \mathcal{A}_n = \begin{bmatrix} 0 & 1 \\ -\frac{\rho}{L_n C} & -\frac{1}{RC} \end{bmatrix},$$

and $\rho \in \{0, 1\}$ is introduced to consider the last $(A_{n+1})$ subsystem (for simplicity in the next algebra).

In the following, a stability test is developed under a common Lyapunov function (CLF) design approach. Hence, stability is ensured despite arbitrary switching [51] regardless of the control actions of $n$ MPPT control systems or of the combination of MPPT control for some stages, and other controllers for the rest.

Consider the common Lyapunov candidate function:

$$V(y) = y^T P y, \quad P = \begin{bmatrix} 1 & p_2 \\ p_2 & p_3 \end{bmatrix} \tag{3}$$

where $p_2, p_3 \in \mathbb{R}$ must be constants such that $P \succ 0$ (positive definite); note that $V(y) = 0$ in $y = [0, 0]^T$. Since one looks for $P \succ 0$, the leading minors of $P$ must be positive, hence $det(P) > 0$ (Sylvester's criterion) such that $p_3 > p_2^2$ is the first condition to meet.

The time derivative of $V(y)$ along the system trajectories is:

$$\dot{V} = y^T (P\mathcal{A}_i + \mathcal{A}_i^T P) y \tag{4}$$

In order to ensure stability despite the arbitrary switching, $Q_i = P\mathcal{A}_i + \mathcal{A}_i^T P \prec 0$ (negative definite) for all $i$, and for all $\rho \in \{0, 1\}$. Consider the case $\rho = 1$, the principal minors of $Q_i$ are as follows:

$$M_1 = -\frac{2p_2}{L_i C} \tag{5}$$
$$M_2 = -\frac{L_i^2 C^2 R^2 - 2L_i^2 RCp_2 + 4L_i CR^2 p_2^2 - 2L_i CR^2 p_3^2 + L_i^2 p_2^2 - 2L_i Rp_2 p_3}{L_i^2 C^2 R^2} - \frac{R^2 p_3^2}{L_i^2 C^2 R^2} \tag{6}$$

$Q_i \prec 0$ if $M_1 < 0$ hence, $p_2 > 0$ is a second condition to meet (odd leading minors must be less than zero). Besides, it must also be fulfilled that $M_2 > 0$:

$$-L_i^2 C^2 R^2 + 2L_i^2 RCp_2 - (4L_i CR^2 + L_i^2) p_2^2 + 2L_i Rp_2 p_3 + 2L_i CR^2 p_3 - R^2 p_3^2 > 0 \tag{7}$$

This is to say, the even minor must be greater than zero. Selecting the worst-case values (for the previous inequality) of $L_m \leq L_i \leq L_M$, where $L_m$ is the lowest $L_i$ value and $L_M$ is the highest $L_i$ value, $p_2$ and $p_3$ values should be selected such that

$$\begin{aligned} -L_m^2C^2R^2 + 2L_M^2RCp_2 - (4L_mCR^2 + L_m^2)p_2^2 + 2L_MRp_2p_3 & \\ +2L_mMCR^2p_3 - R^2p_3^2 & > \\ -L_i^2C^2R^2 + 2L_i^2RCp_2 - (4L_iCR^2 + L_i^2)p_2^2 + 2L_iRp_2p_3 & \\ +2L_iCR^2p_3 - R^2p_3^2 & > 0 \end{aligned} \tag{8}$$

Selecting

$$p_2 = \frac{2L_M^2RC}{4L_mR^2C + L_m^2} > 0 \tag{9}$$

the second condition is met, and the inequality (8) reduces to

$$-L_m^2C^2R^2 + 2L_MRp_2p_3 + 2L_mMCR^2p_3 - R^2p_3^2 > 0 \tag{10}$$

Setting

$$p_3 = \frac{2L_Mp_2 + 2L_MCR}{2R} > 0 \tag{11}$$

Inequality (10) reduces to

$$p_2 > 0 > RC\frac{L_m - L_M}{L_M} \tag{12}$$

such that the second condition is congruent. Now, it must be proved that $p_3 > p_2^2$, which is the first previously stated condition; substituting $p_3$ from (11) in such inequality one has:

$$L_Mp_2 + L_MCR > 2p_2^2 \tag{13}$$

and it is enough to demonstrate that the sole first term is greater than the right side of the previous inequality when $p_2$ from (9) is used:

$$L_Mp_2 > 2p_2^2 \tag{14}$$

$$4L_MR^2C + L_M^2 > 4L_mR^2C + L_m^2 > 4L_MR^2C \tag{15}$$

$$L_M^2 > 0 \tag{16}$$

Consider now the case $\rho = 0$ and note that $\rho \to 0$ when $L_i \to \infty \; \forall i$, such that the previous analysis for $M_2$ holds. On the other hand, it is easy to demonstrate that $M_1 \to 0$ when $L_i \to \infty$, hence $Q_i$ is negative semi-definite. In other words, the bounding of the solutions or practical stability (or simply 'stability') can be ensured; in fact, since there will always be a ripple in the output voltage due to switching between modes, asymptotic stability cannot be expected, but rather the confinement of the system solutions to a small region of the state space. Such regions, in this case, correspond to the level of the ripple of the output voltage that will be estimated in the next section.

## 3. Steady-State Analysis

In the previous section, a dynamic analysis of the MIC was done regardless of the triggering. Next, the output voltage level and the voltage ripple will be obtained by steady-state analysis for the multiple-input, sequential triggering converter (MISeC), and, for completeness purposes, also with simultaneous triggering (MISiC) for comparison purposes.

### *3.1. Averaged Output Voltage for the MISeC*

Considering the MISeC with $n$ parallel boost stages and ideal components, each inductor current will increase linearly when the corresponding MOSFET is activated (on-state), as illustrated in Figure 1b. If the MOSFET is turned off, the corresponding inductor current decreases linearly to zero. Note that the corresponding diode prevents a reverse current through such an inductor; hence the current remains zero (DCM) until the next period ($T_s$) is started, as illustrated in Figure 3a. The sequential triggering can grant an energy flow toward the load with independent control for each stage, ensuring that the average current $< i_{D,out} >$ can be calculated as follows:

$$< i_{D,out} >= \frac{1}{T_s}\int_0^{T_s}\left(i_{D_1} + i_{D_2} + ... + i_{D_n}\right)dt \tag{17}$$

where $i_{D_i}$ is the corresponding current through the diode for each stage.

To calculate $i_{D_i}$, the graphic depicted in Figure 3b shows the behavior of the current through the diode within a $T_s$ period, and whose value can be calculated using the triangle area formulation:

$$i_{D_i} = \frac{T_s}{2}(I_{pk_i}u_{i,2}). \tag{18}$$

Substituting (18) in (17) one has:

$$\int_0^{T_s} i_{D,out} = \frac{T_s}{2}\left(I_{pk_1}u_{1,2} + I_{pk_2}u_{2,2} + ... + I_{pk_n}u_{n,2}\right) \tag{19}$$

where $u_{i,2}$ is the $i$-th inductor discharge period, and $I_{pk_i}$ represents the respective inductor peak current (see Figure 3). $I_{pk_i}$ can be calculated as [52]:

$$I_{pk_i} = \frac{e_i}{L_i}u_{i,1}T_s. \tag{20}$$

Substituting (20) in (19), the average current of all of the diodes can be approximated by:

$$< i_{D,out} >= \frac{T_s}{2}\sum_{i=1}^{n-1}\frac{e_i u_{i,1}u_{i,2}}{L_i}. \tag{21}$$

The discharge period $u_{i,2}$ can be calculated by the relationship between the legs and the hypotenuse derived from the current's triangular shape through the diode, as shown in Figure 3b. This means that the tangent angle is a function of $u_{i,2}$, and $I_{pk_i}$, and its value can be expressed as follows:

$$\frac{-(e_i - V_o)}{L_i} = \frac{I_{pk_i}}{u_{i,2}T_s}. \tag{22}$$

Solving for $u_{i,2}$ one has:

$$u_{i,2} = \frac{e_i u_{i,1}}{V_o - e_i}. \tag{23}$$

Note that in the previous equations, the notation for $V_o$ is being abused because it was also used in the switched model, and it should not cause confusion since it now represents the same voltage but is seen in an averaged way.

Substituting $u_{i,2}$ from the preceding expression into Equation (21) and considering that the maximum current through the diodes is $i_{D,out,max} = \frac{V_o}{R}$, the average output voltage can be expressed as follows:

$$K_0\left[V_o^{n+1}-(e_1+,...,+e_n)V_o^n+,...,+\left(\prod_{m=1}^{n}e_m\right)V_o\right]+,...,$$
$$+\frac{\prod_{m=1}^{n}e_mL_m}{e_1e_2L_1L_2}(K_1e_2L_2+K_2e_1L_1)+,...,$$
$$+K_n\prod_{m=1}^{n-1}e_mL_m=0, \quad (24)$$

where

$$K_0=\frac{2\prod_{m=1}^{n}L_m}{RT_s}, K_1=e_1^2u_{1,1}^2, K_2=e_2^2u_{2,1}^2,...,K_n=e_n^2u_{n,1}^2$$

Equation (24) is a polynomial function where the roots are $V_o$ values. One can infer that the real $V_o$ value must be the maximum, real and positive one. In later sections, this assumption is validated.

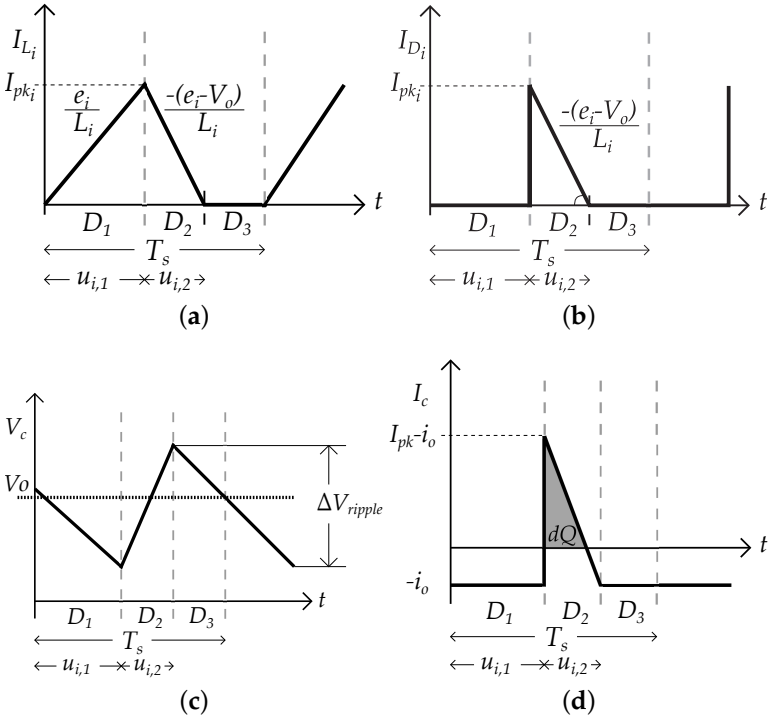



**Figure 3.** Waveforms for the *i*-th stage of the MISeC operating in DCM: (**a**) Inductor current. (**b**) Current through the diode. (**c**) Capacitor output-voltage. (**d**) Capacitor current.

### *3.2. Output Voltage Ripple for the MISeC*

The voltage ripple ($\Delta_{V_{ripple}}$) is defined as the difference between the maximum and minimum of the steady-state output voltage, as illustrated in Figure 3c; in this paper, this difference is expressed as a function of the capacitor current as depicted in Figure 3d:

$$I_c=C\frac{dV_{ripple}}{dt}=\left|\frac{dQ}{dt}\right| \quad (25)$$

where $Q$ is the capacitor charge. The differential of charge for each stage ($dQ_i$) can be approximated using the capacitor charge period $u_{i,2}$, and the triangle area formulation (see Figure 3d):

$$dQ_i=\frac{b_ih_i}{2} \quad (26)$$

where $h_i = I_{pk_i} - i_o$ is the triangle height, $i_o$ the output current, and $b_i$ the base width. Using similarity theorems, one has:

$$b_i = \frac{(I_{pk_i} - i_o)u_{i,2}T_s}{I_{pk_i}}. \tag{27}$$

To determine the value of $b_i$ as a $u_{i,1}$ function, one can substitute (23) in (27), thus:

$$b_i = \frac{(I_{pk_i} - i_o)u_{i,1}e_iT_s}{I_{pk_i}(V_o - e_i)}. \tag{28}$$

Substituting the value of $u_{i,2}$ in Equation (23), and substituting Equation (27) in (26):

$$dQ_i = \left| \frac{1}{2} \frac{(I_{pk_i} - i_o)^2 u_{i,1}e_iT_s}{I_{pk_i}(V_o - e_i)} \right|. \tag{29}$$

Replacing (29) in (25) and solving for the $i$-th $dV_{ripple}$:

$$\Delta V_{ripple,i} = \left| \frac{(e_iu_{i,1}T_s)}{2CI_{pk_i}} \frac{(I_{pk_i} - i_o)^2}{V_o - e_i} \right|. \tag{30}$$

Using $L_i$ from Equation (20), Equation (30) can be expressed as:

$$\Delta V_{ripple,i} = \left| \frac{L_i}{2C} \frac{(I_{pk_i} - i_o)^2}{V_o - e_i} \right|. \tag{31}$$

Since one looks only for the maximum ripple:

$$\Delta V_{ripple} = \max_i \left( \left| \frac{L_i}{2C} \frac{(I_{pk_i} - i_o)^2}{V_o - e_i} \right| \right). \tag{32}$$

Usually, keeping a lower percentage of voltage ripple is desirable in converter applications. If the output voltage ripple is greater than that supported by the load, it could be damaged. In the following, the output ripple for the MISiC is calculated; an analytic comparative is performed to show the sequential benefits concerning simultaneous triggering.

### *3.3. Average Output Voltage for the MISiC*

In this scenario, the average current through all of the diodes can be approximated as in Equation (21). Since $< I_{D_{out}} > = V_o/R$, the average output voltage can be estimated as:

$$V_o \approx \frac{RT_s}{2} \sum_{i=1}^{n-1} \frac{e_iu_{i,1}u_{i,2}}{L_i}. \tag{33}$$

It is important to recall that in this scenario, all of the switches are activated within the same period; this formulation is not precise for the MISeC.

### *3.4. Output Voltage Ripple for the MISiC*

In this scenario, the total peak current $I_{pk}$ due to simultaneous triggering can be calculated as:

$$I_{pk} = I_{pk1} + I_{pk2} + I_{pk3} + ... + I_{pkn}. \tag{34}$$

Considering that the charge interval $ui, 1$ ends within the same period, the capacitor current can be calculated as in Equation (25). Two scenarios to calculate the area for $dQ_i$ are possible. All input/source voltages are the same in the former, and in the latter, all

input voltages are different. For the former, substituting Equation (34) in (25) and solving for $\Delta V_{ripple,i}$, one has:

$$\Delta V_{ripple,i} = \max_i \left( \left| \frac{(e_i u_{i,1} T_s)}{V_o - e_i} \frac{(I_{pk} - i_o)^2}{2C I_{pk}} \right| \right). \tag{35}$$

Note that again, one looks only for the maximum ripple.

For the latter case (different input voltages), and using Figure 4, $dQ$ can be approximated as:

$$dQ \approx \left( \left| \frac{I_{pk} - i_o}{2} \bar{\iota u_2} T_s \right| \right), \tag{36}$$

where $\bar{\iota u_2}$ is the average of the discharge periods. Substituting Equation (36) in (25):

$$\Delta V_{ripple} \approx \left( \left| \frac{I_{pk} - i_o}{2C} \bar{\iota u_2} T_s \right| \right). \tag{37}$$

Since $\bar{\iota u_2}$ can be expressed in terms of $u_{i,1}$, (37) can be rewritten as:

$$\Delta V_{ripple} \approx \left( \left| \frac{I_{pk} - i_o}{2C} \frac{1}{n} \sum_{i=1}^{n} \frac{e_{i,1} u_{i,1}}{V_o - e_{i,1}} T_s \right| \right). \tag{38}$$

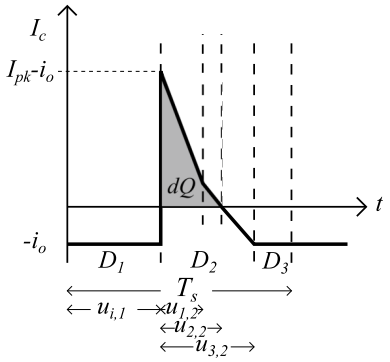



**Figure 4.** Capacitor current exemplification for the MISiC in DCM.

### *3.5. Analytic Ripple Comparison for Sequential and Simultaneous Triggering*

From Equations (20), (32), and (35), it is easy to see that the ripple for the simultaneous triggering with the same voltage inputs is greater than the sequential case because

$$I_{pk} = I_{pk1} + I_{pk2} + I_{pk3} + ... + I_{pkn} > I_{pki} \tag{39}$$

for the same duty cycles, except for the trivial case in which all peak currents are zero.

To show that the ripple with simultaneous triggering and unequal voltage inputs is greater than that with sequential triggering, it is enough to compare Equations (20), (32) and (38):

$$\max_i \left| \frac{e_i u_{i,1} T_s}{2C(V_o - e_i)} \frac{(I_{pk_i} - i_o)^2}{I_{pk_i}} \right| < \left| \left( \frac{I_{pk1} + I_{pk2} + ... + I_{pkn} - i_o}{2C} \right) T_s \frac{1}{n} \sum_{i=1}^{n} \frac{e_{i,1} u_{i,1}}{V_o - e_{i,1}} \right|, \tag{40}$$

$$\max_i \left| \frac{e_i u_{i,1}}{(V_o - e_i)} \frac{(I_{pk_i} - i_o)^2}{I_{pk_i}} \right| < \left| \left( I_{pk1} + I_{pk2} + ... + I_{pkn} - i_o \right) \frac{1}{n} \sum_{i=1}^{n} \frac{e_{i,1} u_{i,1}}{V_o - e_{i,1}} \right|. \tag{41}$$

Since the input voltages $e_i$ are different:

$$\sigma = \frac{\frac{1}{n}\sum_{i=1}^{n}\frac{e_{i,1}u_{i,1}}{V_o - e_{i,1}}}{\max_i\left(\frac{e_i u_{i,1}}{V_o - e_i}\right)} < 1. \tag{42}$$

Using $\gamma = (I_{pk_i} - i_o)/I_{pk_i} < 1$:

$$\gamma|I_{pk_i} - i_o| < |I_{pk_i} - i_o| < \sigma|I_{pk1} + I_{pk2} + ... + I_{pkn} - i_o| \leq |I_{pk1} + I_{pk2} + ... + I_{pkn} - i_o|. \tag{43}$$

Hence,

$$|I_{pk_i}| < |I_{pk1} + I_{pk2} + ... + I_{pkn}| \tag{44}$$

and all of the (rest of the) triangle inequality theorem conditions are met, except, again, for trivial cases in which all or almost all, peak currents are zero.

Section 5 illustrates numerically and graphically how the ripple is considerably less using sequential triggering.

## 4. Component Selection

The configuration of $n$ parallel stages of the proposed MISeC allows individual component sizing, with the only condition of maintaining the DCM. Considering that the MISeC enables the use of different types of DC sources, a scenario is illustrated and experimented with three 100 W maximum power sources without loss of generality. These sources are two 100 W maximum-power PVM (at 1000 W/m$^2$ irradiation) and a battery with the capacity to give a constant 100 Wh rate (emulated by a power supply).

For such design, the maximum duty cycle for each stage $u_{max}$, to avoid the superposition of each stage ripple and get a clean (regular) output-voltage signal, is $0 \leq u < 1/3$. Here, the PWM operating frequency $f_s$ is established as 10 kHz without loss of generality; this frequency is selected here because it is easy to achieve with cheap components such as micro-controllers. Hence, for DCM, the critical inductance is defined as [53,54]:

$$L_c \leq \max_i\left(\frac{Ru_i(1-u_i)^2}{2f_s}\right) \tag{45}$$

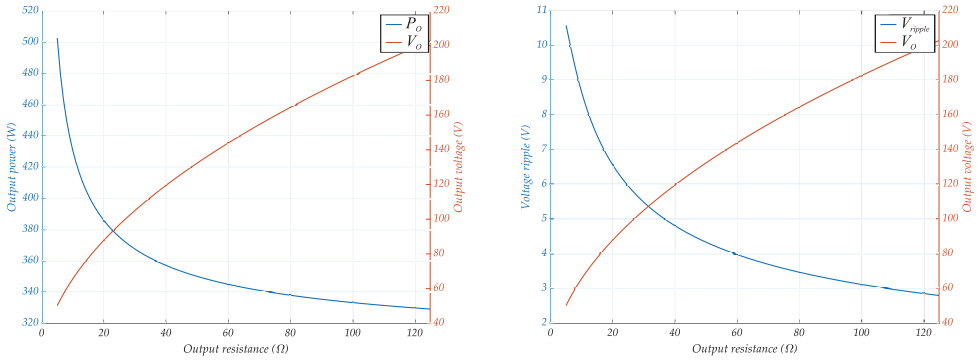
Using an $R \geq 10\ \Omega$ load, $L_i < 74\ \mu$H, and from Equation (20), a maximum-voltage vs. current trade-off is advertised. Looking for commercial values, Coilcraft inductors of 22 µH and a 35.4 A maximum current are selected because of their availability and low cost. Hence, the peak voltage supported is 23.364 V per stage.

From Figure 5a, the power output and output voltage can be estimated since they depend on the load resistance as stated in the previous sections. The range of power for this design is approximately $[300, 600]$, W and the range of average output voltage is $[35, 670]$ V. Here, the load is selected as $R = 75\ \Omega$, according to this design. Figure 5b illustrates the output voltage and the voltage ripple as a function of the load resistance for a 25 µF capacitor; hence, this capacitance is selected for the design (this value must be chosen based on the real-application desired ripple level).

Table 2 shows the relevant and real (experimentally measured) parameters obtained from commercial parts. Note that relevant parameters for inductors were individually validated to gain precision on the next validations.

**Table 2.** Relevant Parameters.

| | |
|---|---|
| **Photovoltaic Panel SE-156*104-100P-72** | |
| Power (nominal-real) | 100–70 W |
| Maximum open circuit voltage | 21.61 V |
| Short circuit current @ 1000 W/m$^2$ | 5.74 A |
| Voltage at maximum power (nominal-real) | 17.70–17.50 V |
| Current at maximum power (nominal-real) | 5.65–4.00 A |
| **Inductor AGP4233-223** | |
| Peak current (nominal) | 35.4 A |
| $L_1$ (real @ 10 kHz)<br>$L_2$ (real @ 10 kHz)<br>$L_3$ (real @ 10 kHz) | 23.6381 µH<br>24.7115 µH<br>23.6081 µH |
| $L_1$ resistance (real @ 10 kHz)<br>$L_2$ resistance (real @ 10 kHz)<br>$L_3$ resistance (real @ 10 kHz) | 0.644 Ω<br>0.656 Ω<br>0.650 Ω |
| **MOSFET FDP** | |
| $R_{DS_{on}}$ | 94 mΩ |
| **Diode MUR1520** | |
| $V_D$ | 0.85 V |
| **Capacitor** | |
| Value | 25 µF |
| Series resistance | 8.6 mΩ |
| **Output load** | |
| Value | 75 Ω |
| **Power supply BKPrecision 9132B** | |




(**a**) (**b**)

**Figure 5.** Illustration of the estimated ranges for the power output and output voltage as functions of the load resistance: (**a**) Power & voltage vs. resistance. (**b**) Ripple & voltage vs. resistance. The range of power for this design is [300, 600] W, and the range of average output voltage is [35, 670] V. Here, the load is selected as R = 75 Ω as an exemplar.

## 5. Numerical Validation of the Models

To validate the formulations provided, in this section, the results of numerical comparison against PSIM are presented. The previously stated design includes three boost

stages, and 22 operation modes are possible. This switched model is integrated into Matlab Simulink, and in both models, the components are considered ideal.

The first validation consists of comparing the output voltage obtained with the proposed model against that provided by PSIM. For this test, $e_1 = 17.7$ V, $e_2 = 17.7$ V, and $e_3 = 23$ (design parameters for maximum irradiation), with 33.3% duty cycles. In Figure 6, the average and ripple outputs are compared. The PSIM model response is plotted in purple for the averaged output voltage and yellow for the ripple. The model response is plotted in red and blue for the averaged output voltage and ripple, respectively. It can be seen that the average voltage is 157.80 V and 155.92 V, with PSIM and the proposed models, respectively; the voltage ripple is 3.4717 V for the PSIM simulation and 3.3977 V for the proposed model. This is a $-0.33\%$ numerical precision error in average that can be neglected.

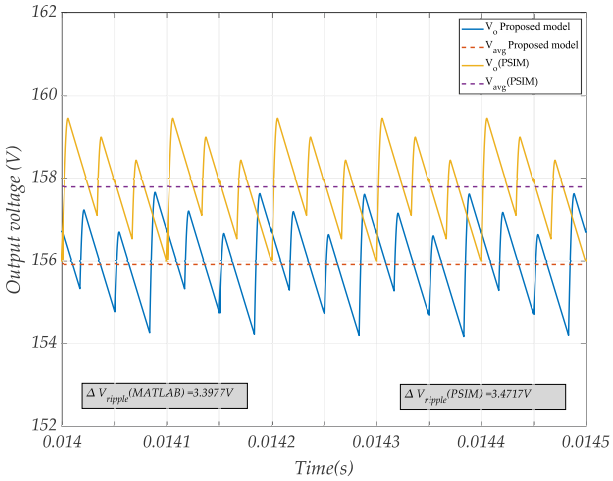



**Figure 6.** Comparison of the averaged output voltage and ripple of the MISeC, obtained with the circuit simulated in PSIM (purple, yellow respectively) and the integration of Equation (1) in Simulink. For this test, $e_1 = 17.7$ V, $e_2 = 17.7$ V, and $e_3 = 23$ (design parameters for maximum irradiation), with 33.3% duty cycles.

Two scenarios for validation for the steady-state formulations are presented. In the former, equal 17.7 V input voltage sources were used, and in the latter $e_1 = 12$ V, $e_2 = 17.3$ V, and $e_3 = 22$ V. In both scenarios, a 33% duty cycle for all stages is used. Other tests with different combinations of input voltage levels and duty cycles were performed, corroborating the model's validity; however, only representative results are presented.

Figure 7 shows a simulation interval for the first scenario. The upper plot shows the average and ripple output voltages for the MISiC, and the lower for the MISeC, both simulated in Matlab (proposed model) and PSIM. The errors concerning the average voltage for the MISiC formulations are $-2.18$ and $-0.34\%$ for the proposed model and the PSIM model, respectively; $-1.72$ and $-0.40\%$ output voltage ripple errors are estimated for the proposed and PSIM models, respectively. For the MISeC formulations, the average voltage errors are $-1.53$ and $-0.35\%$ for the proposed and PSIM models, respectively; $-0.72$ and $-0.46\%$ output voltage ripple errors are estimated for the proposed model and the PSIM model, respectively.

The second scenario (different input sources) in Figure 8 shows the average and ripple output voltages for the MISiC in the upper plot, and in the lower plot for the MISeC, both simulated in Matlab (proposed model) and PSIM. The errors concerning the average voltage for the MISiC formulations are $-2.10$ and $-0.39\%$ for the proposed and PSIM models, respectively; 1.01 and 2.20% output voltage ripple errors are estimated for the proposed and PSIM models, respectively. For the MISeC formulations, the average voltage errors are $-1.57$ and $-0.35\%$ for the proposed and PSIM models, respectively; $-1.88$ and $-0.52\%$ output voltage ripple errors are estimated for the proposed and PSIM models, respectively.

Other tests with different combinations of voltage levels and duty cycles were performed, corroborating the validity of the formulations; however, only representative results are presented here. Note that both the provided model and the formulations for the steady-state output voltage provide reasonable approximations.

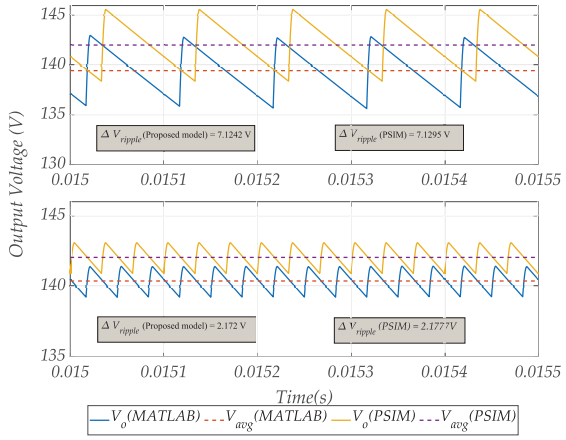



**Figure 7.** Average and ripple output voltages for the MISeC and the MISiC (upper and lower plots, respectively). The diminution of the ripple with the MISeC is notable. This plot allows the proposed model and formulations in a scenario of equal 17.7 V input source voltage levels and 33% duty cycles to be validated.

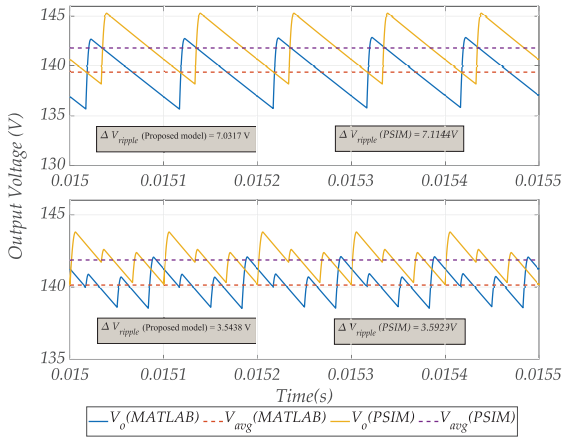



**Figure 8.** Average and ripple output voltages for the MISeC and the MISiC (upper and lower plots, respectively). The diminution of the ripple with the MISeC is notable. This plot allows the proposed model and formulations in a scenario with $e_1 = 12$ V, $e_2 = 17.3$ V, and $e_3 = 22$ V, and 33% duty cycles to be validated.

For completeness purposes, a comparison of the output voltage ripple (for both MISeC and MISiC) as a function of $R$ is presented. This is, the load resistance varies within a $[1, 100]$ $\Omega$ range. Such comparison is plotted in Figure 9. The diminution of the ripple with the MISeC is notable for a wide range of loads, as expected from Section 3.5.

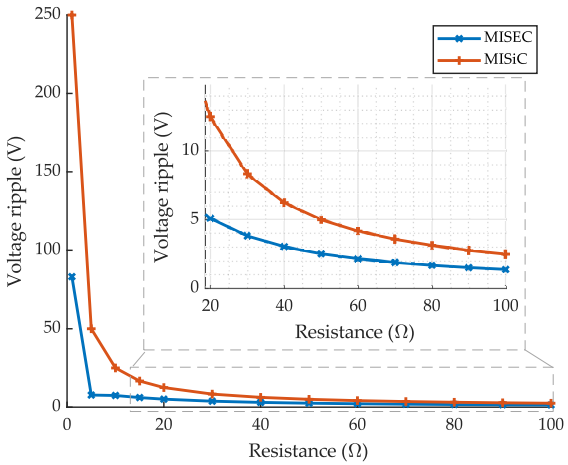



**Figure 9.** Voltage ripple comparison for the proposed MISeC and the MISiC, as a function of the load. The diminution of the ripple with the MISeC is notable for a wide range of loads.

## 6. Experimental Validation

### *6.1. Experimental Setup*

Figure 10 shows the complete system for the experimental tests, where each photovoltaic module is connected to each of the inputs and the power supply, emulating a battery. The MISeC uses a Microchip DSPIC33, three inline current sensors (at the bottom of the PCB), and other basic circuitry. The DSPIC performs analog to digital conversion, MPPT, and PWM functions. The PCB was built only for prototype test purposes; hence, some noise is expected. A final production PCB design is not the purpose of this paper and is left for future research.

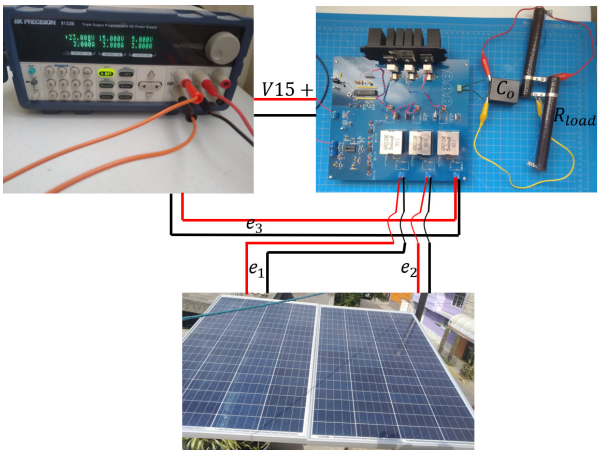



**Figure 10.** Proposed experimental platform to test the MISeC with three parallel boost stages.

### *6.2. Controller Design*

The following experimental tests are intended to demonstrate that the MISeC allows the independent operation of $n$ MPPT controllers, simultaneously with other power tracking techniques as a constant power rate one—to avoid degradation of fuel cells or batteries, for instance. There are various MPPT algorithms in the literature. Whether by direct methods [55–57], or indirect methods [55], it is essential to maintain the maximum power point available. Here, a simple and easy-to-implement technique is used, known as a perturb and observe (P&O) [58,59], illustrated in Figure 11 (for a single MPPT algorithm). This article is not aimed at developing a novel maximum power tracking method. It is important to recall that different MPPT algorithms are calculated individually in the MISeC. Particularly, two independent P&O MPPT algorithms are calculated by the DSPIC33, one for each photovoltaic module stage. The last stage is set to control its output power using a

PI controller; this is the case for some fuel cells or batteries in diverse scenarios and is quite different from an MPPT.

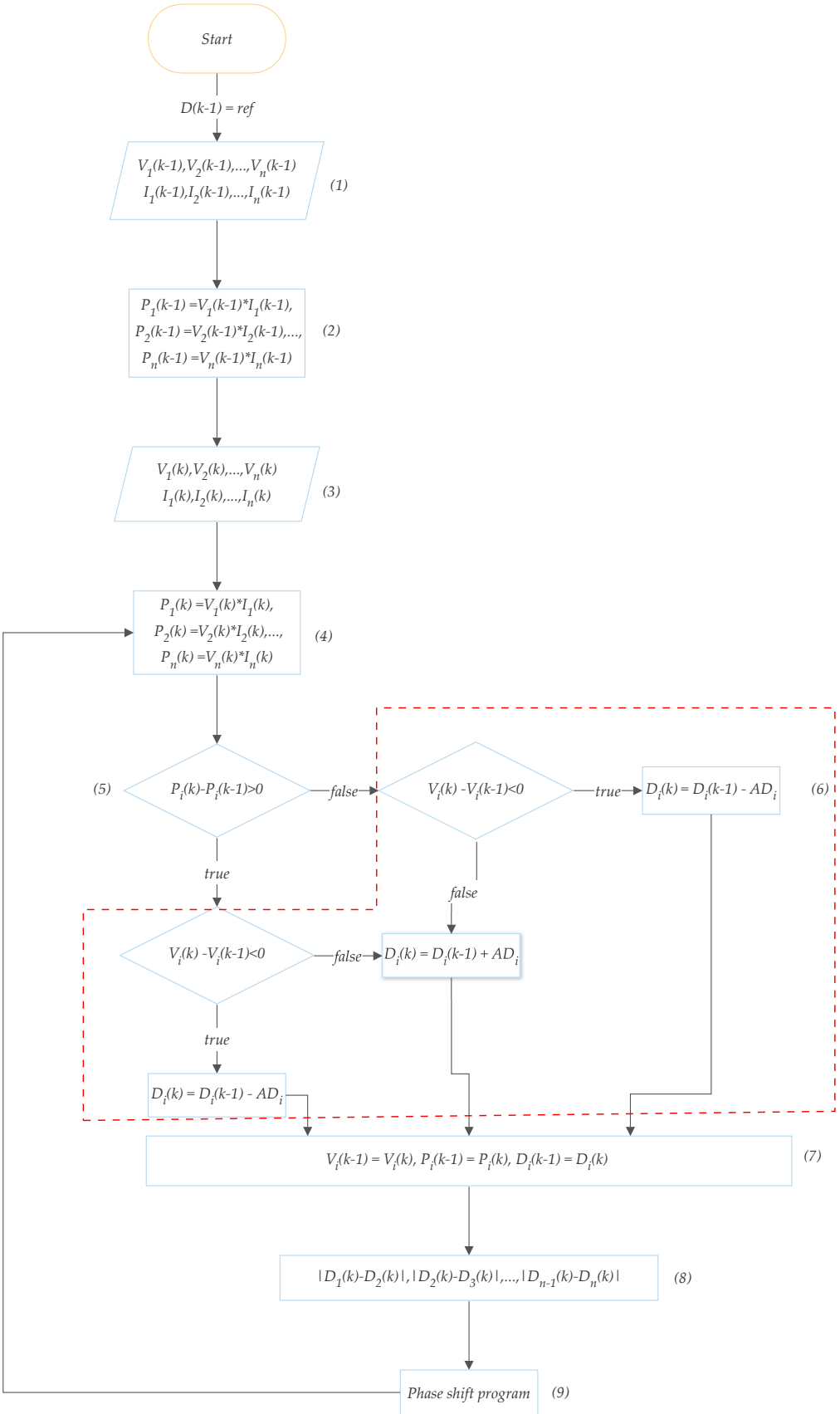
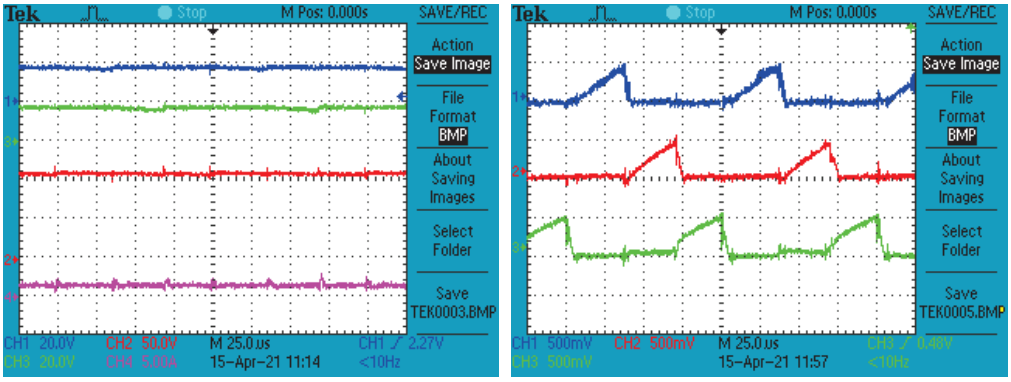



**Figure 11.** Description of a single MPPT algorithm operation.

### *6.3. Experimental Tests*

Figure 12a shows the PVM voltages, the output voltage, and the output current for high (full) irradiation conditions in both PVMs. Figure 12b shows the currents through the inductors. Note that the charging periods are not simultaneous, and the MPPT algorithms can operate independently from the third stage (constant power). Figure 13 shows the triggering signals and the output voltage for the MISeC. Please refer to Table 3 for efficiency, voltage, power, and current levels.




(**a**) (**b**)

**Figure 12.** Behavior of inputs, currents through the inductors, and output with double MPPT algorithm operation in the MISeC, full irradiation, and a constant power rate (power supply) in the third input. (**a**) The first photovoltaic panel voltage is shown in blue color. The second photovoltaic panel voltage is shown in green in channel 3 with the same scale. The output voltage is shown in red, with a scale of 50 V/div, on channel 2. The output current is shown with a scale of 5 A/div, on channel 4 and purple color. (**b**) Currents through the inductors for the MISeC at full irradiation. The upper signals (blue and red) are for the PVM stages with a 30% duty-cycle. The third signal (green) is for the battery at 33% duty-cycle. Please refer to Table 3 for efficiency, voltage, power and current levels.

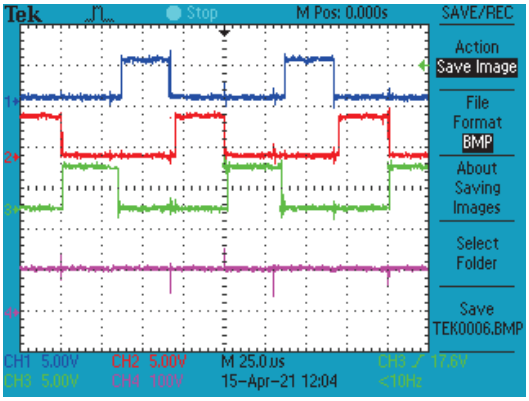
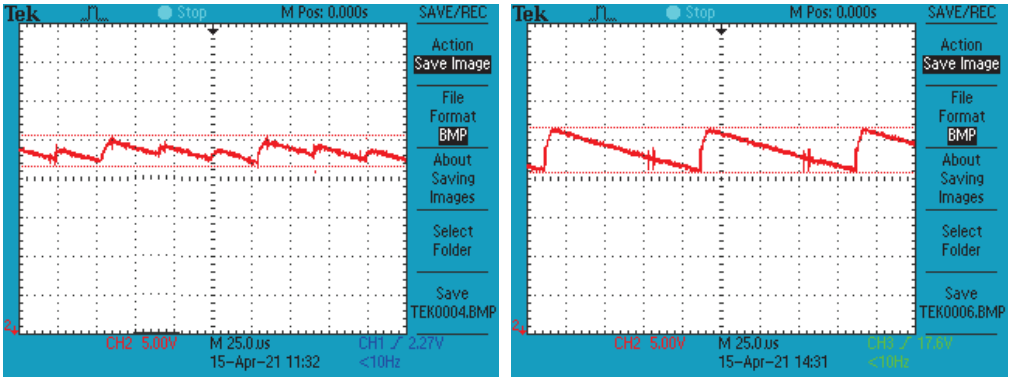



**Figure 13.** Triggering signals for the MISeC at full irradiation. The upper signals (blue, red) are for the photovoltaic panels with a 30% duty-cycle. The third signal (green) is for the battery at 33% duty-cycle, and the bottom signal (purple) is the output voltage (114 V).

Figure 14a shows the output voltage ripple with a 5 V/div scale for the MISeC. The average estimated value is 3.40 V, which represents a −2.39% error with respect to the 3.4834 V calculated with the previously stated formulations. Comparatively, Figure 14b shows the ripple for the MISiC under the same conditions; note that 6.2 V is considerably greater (82%) than for the MISeC. Figure 15 shows the simulations for this previous scenario (the proposed model and PSIM model). It should be mentioned that for this simulation, the values in Table 2 are used, including parasitic resistances. Comparatively, Figure 16 shows

the related voltages for the MISiC. Table 4 summarizes the accuracy of the proposed models for this test. The last two columns represent the PSIM model error, and the proposed model error, respectively, both regarding the experimental values. Note that the formulations provide acceptable values.

Finally, two additional experimental tests are presented. For the first one, irradiation is manually depleted on the first photovoltaic module (covered with a translucent film). For the second experiment, the two panels are covered. Figure 17a,b show the triggering pulses and output voltages for such scenarios, respectively. In Figures 18a and 19a, the PVM voltages, the output voltage, and the output current, respectively, are shown for each test. The duty cycle is 25% for a covered panel, while the other remains as in the full irradiation scenario. Figures 18b and 19b show the behavior of the currents through the inductors for each test. Please refer to Table 3 for efficiency, voltage, power, and current levels.




(**a**) (**b**)

**Figure 14.** Comparison of the voltage ripples obtained for full irradiation, for the MISeC and the MISiC, and a 5 V/div scale. (**a**) For the MISeC proposed in this paper, the ripple is approximately 3.40 V, while the error concerning the formulations is about −2.39%. (**b**) For the MISiC, the ripple is estimated as 6.2 V, and is considerably greater (82%) than for the MISeC under the same conditions.

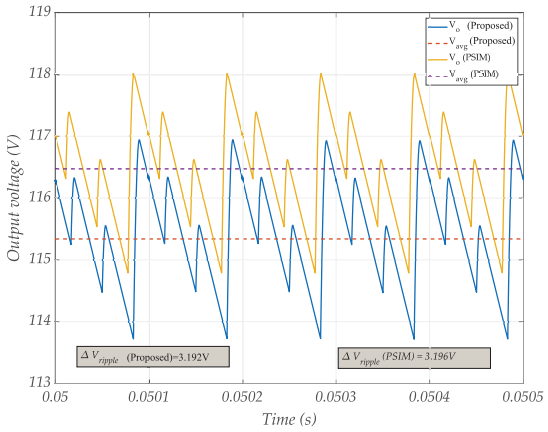



**Figure 15.** Voltage ripple obtained by simulations for comparison with the experimental results in Figure 14.

Note that the MISeC allows the independent operation of each MPPT while the ripple is small compared to other configurations and triggering strategies. For completeness purposes, Table 3 resumes power and efficiency values for all the experimental tests. Final production PCB and other considerations will provide better efficiency values; it is not the purpose of this paper to improve the efficiency, but, according to experiments, at least 88% can be obtained. Regardless of the above, the efficiency is much better for the MISeC, with less ripple, and $n$ independent MPPT controllers can be integrated.

From the previous tests, a stable operation of the MISeC can be concluded; multiple MPPT algorithms along with other controllers, such as the constant power one, can be used with acceptable efficiency and low ripple.

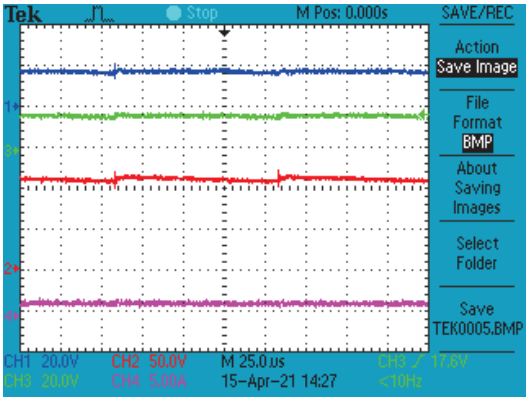
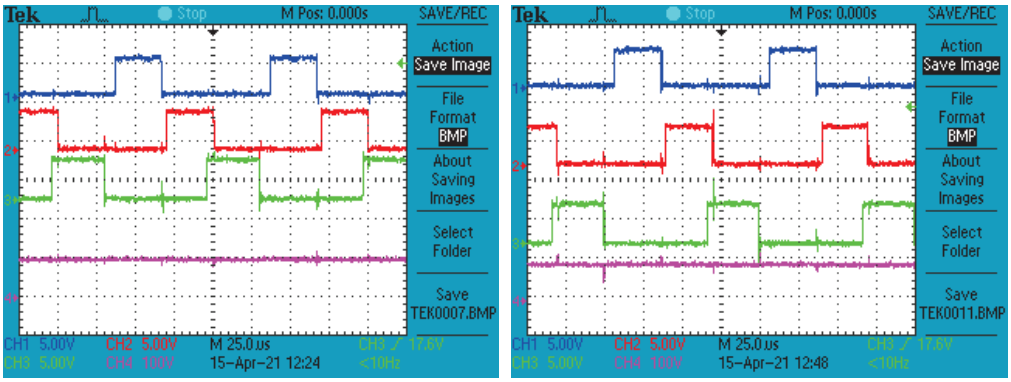



**Figure 16.** Voltage of PVM and the output voltage and current, with double MPPT algorithm operation in the MISiC, full irradiation, and a constant power rate (power supply) in the third input. The first photovoltaic panel voltage is shown in blue color with a value of 17.5 V on average (Channel 1, 20 V/div). The second photovoltaic panel voltage is shown in green in Channel 3 with the same scale and 17.4 V on average. The output voltage is shown in red, with a scale of 50 V/div, on channel 2, and an average voltage of 109 V. The output current is shown with a scale of 5 A/div, on channel 4 with a value of 1.53 A and purple color.

**Table 3.** Experimental Efficiency (Average).

| Stage | $I_{L_i}$ [A] | $e_i$ [V] | $P_i$ [W] | $V_o$ [V] | $i_o$ [A] | $P_o$ [W] | Efficiency |
|---|---|---|---|---|---|---|---|
| Maximum Irradiation (MISeC) | | | | | | | |
| 1 | 3.32 | 15.7 | 52.14 | | | | |
| 2 | 3.24 | 15.5 | 50.22 | 80.3 | 1.27 | 101.981 | 82.27 |
| 3 | 2.16 | 10 | 21.6 | | | | |
| Single PV Module Shaded (MISeC) | | | | | | | |
| 1 | 1.862 | 8 | 14.896 | | | | |
| 2 | 3.32 | 15.8 | 52.456 | 68.3 | 1.05 | 71.715 | 80.62 |
| 3 | 2.16 | 10 | 21.6 | | | | |
| Both Shaded PV Modules (MISeC) | | | | | | | |
| 1 | 2.1 | 10 | 21 | | | | |
| 2 | 1.92 | 8.5 | 16.32 | 57.3 | 0.82 | 46.986 | 79.74 |
| 3 | 2.16 | 10 | 21.6 | | | | |
| Maximum Irradiation (MISiC) | | | | | | | |
| 1 | 3.2 | 15.9 | 50.88 | | | | |
| 2 | 3.2 | 15.9 | 50.88 | 78.7 | 1.23 | 96.801 | 78.47 |
| 3 | 2.16 | 10 | 21.6 | | | | |

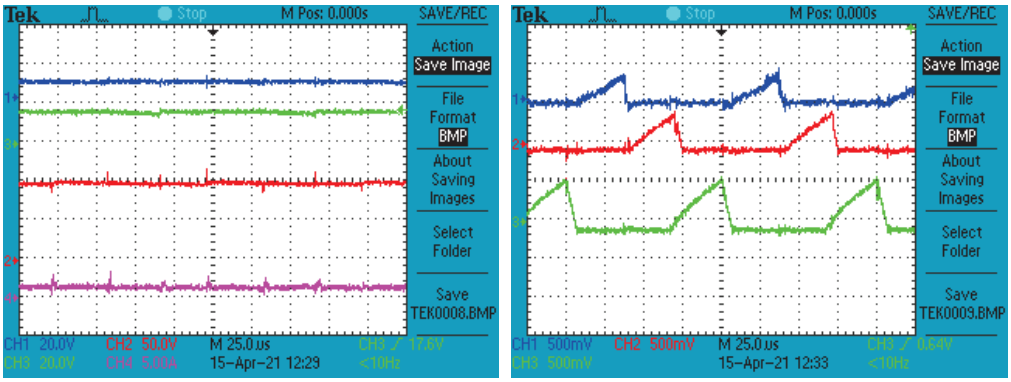



(**a**) (**b**)

**Figure 17.** Triggering and output voltage signals for the MISeC with partial shade. (**a**) A single module partially-shaded. (**b**) Both PVM partially-shaded.The two upper signals are the duty cycles for the modules (5 V/div), followed by those for the battery (5 V/div) and the output voltage (100 V/div). The MPPT algorithms can operate independently, even in the presence of the constant rate source. Please refer to Table 3 for efficiency, voltage, power and current levels.

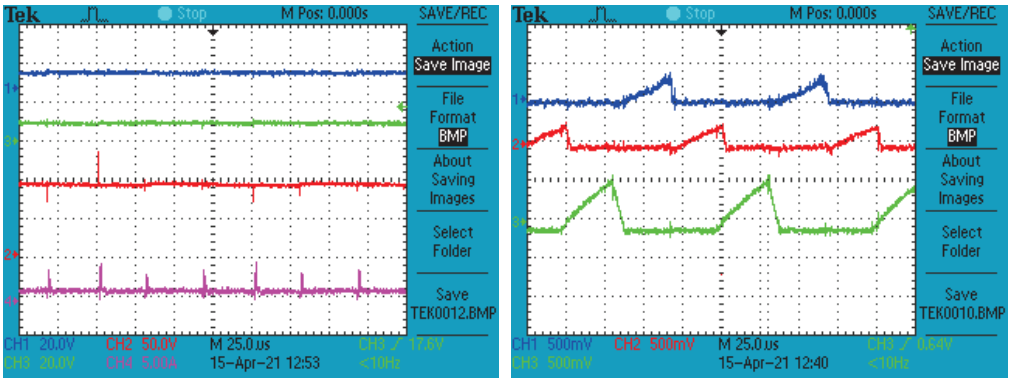
**Table 4.** Accuracy of the Models.

| | Values | | | Error | |
|---|---|---|---|---|---|
| | **PSIM** | **Model** | **Experimental** | **PSIM** | **Model** |
| $V_o$ | 116.47 V | 115.34 V | 114 V | −2.12 % | −1.16 % |
| $P_{out}$ | 184.97 W | 179.048 W | 193.8 W | 4.77 % | 8.21 % |
| $V_{ripple}$ | 3.196 V | 3.192 V | 3.40 V | 6.3 % | 6.51 % |




(**a**) (**b**)

**Figure 18.** PVM voltages, output voltage, output current, and currents through the inductors for a single photovoltaic module partially shaded of the MISeC. (**a**) The two upper signals are the modules voltages (20 V/div), followed by the output voltage (50 V/div), and the output current (5 A/div). The MPPT algorithms can operate independently, even in the presence of the constant rate supply. (**b**) The upper signals are for the photovoltaic panels with 25 and 30% duty cycles, respectively. The third signal is for the battery at 33% duty-cycle. Please refer to Table 3 for efficiency, voltage, power and current levels.




(**a**) (**b**)

**Figure 19.** PVM voltages, output voltage, output current, and currents through the inductors for both PVM partially shaded of the MISeC. (**a**) The two upper signals are the modules voltages (20 V/div), followed by the output voltage (50 V/div), and the output current (5 A/div). The MPPT algorithms can operate independently, even in the presence of the constant rate supply. (**b**) The upper signals are for the photovoltaic panels with 25% duty cycles. The third signal is for the battery at 33% duty-cycle. Please refer to Table 3 for efficiency, voltage, power and current levels.

## 7. Discussion, Conclusions, and Future Work

A dynamic model for the boost-type (paralleled) MIC with any finite number of stages/input sources is developed in this paper. Such a model can be used for different control objectives as voltage or current regulation. It is analytically demonstrated that the dynamic model is output-voltage stable for a resistive load regardless of the switching, and hence, of the conduction mode under regular (appropriate) parametrization. The stability in such a sense does not depend on the used controllers, and the controllers can operate independently as long as they follow compatible objectives.

Steady-state analyzes are performed to estimate the average output voltage and the output voltage ripple, including any finite number of stages/input sources. These analyzes can be extended to obtain the ripple of the currents through the inductors, output current ripple, and other variables of interest. Additional study analytically shows that the ripple is considerably reduced regarding a simultaneous triggering in the same electric configuration.

The presented dynamic model, the formulations obtained, the ripple reduction concerning a simultaneous triggering and, the stability under multiple control types (MPPT + constant rate) are validated numerically and experimentally.

The presented configuration allows any finite number of different DC voltage levels to be connected; hence, other energy collectors can be used. PVMs in different locations (irradiation conditions) can be integrated into a single DC bus, avoiding the potential induced degradation (because of their parallel interconnection instead of a series one). Even more, the implementation cost of the MISeC is relatively low.

Future work must consider AC input sources; although rectification could initially solve their integration in the MISeC, new phenomena can be generated, such as power quality issues and resonance effects.

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