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Open-Loop Class-BD Audio Amplifiers with Balanced Common-Mode Output

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Abstract: This paper presents new architectures and implementations of original open-loop Class-BD audio amplifiers with balanced Common-Mode output. The output stage of each proposed amplifier includes the typical H-bridge with four MOSFETs and four additional MOSFET switches that balance and keep the Common-Mode output constant. The presented amplifiers employ the extended NBDD PWM or PSC PWM modulation scheme. When the output stage is built only on NMOSFET transistors, gate drivers require a floating power supply, using a self-boost charge pump with capacitive isolation of the control signal. The use of complementary MOSFETs in the output stage greatly simplifies gate control systems. The proposed amplifiers were compared to the typical Class-BD configuration, using the optimal NBDD modulation with respect to audio performance of the Differential-Mode (DM) and Common-Mode (CM) outputs. Basic SPICE simulations and experimental studies have shown that the proposed Class-BD amplifiers have similar audio performance to the prototype with the optimal NBDD modulation scheme, while at the same time having a balanced constant voltage CM output, thus eliminating the main contributor to radiation emission. As a result, the filtering of the DM output signals can be greatly simplified, while the filtering of the CM output signals can be theoretically eliminated. Practically, due to the timing errors added by the gate drivers, spikes are generated at the CM output, which are very easy to filter out by the reduced LC output filter, even at very low L.

Keywords: Class-BD audio amplifier; Common-Mode (CM) and Differential-Mode (DM) output signals; Natural sampling Class-BD Double sided modulation (NBDD PWM); Phase Shifted Carrier PWM (PSC PWM)

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1. Introduction

Many works have been dedicated to different kinds of improved PWM methods and Class D power amplifier topologies in order to achieve two of the most important features: high fidelity and high efficiency.

Class-D amplifier architectures can generally be divided into two categories: open-loop Class-D amplifiers with natural pulse width modulation (NPWM), or its discrete-time version known as uniform PWM (UPWM); and closed-loop ones with Sigma-Delta modulation (SDM) and bang-bang control modulation.

Depending on the sampling method, PWM schemes are generally categorized in three of the most important classes: natural NPWM, uniform UPWM and linearized PWM (LPWM) [1,2].

In addition, each PWM sampling method also distinguishes one-edge or two-edge PWM, as well as two-level (Class-AD) or three-level (Class-BD) switching. Among four fundamental NPWM schemes, NBDD (Natural sampling Class-BD Double sided) modulation, which is equivalent to the level-three version of Phase Shifted Carrier Pulse Width Modulation (PSC PWM) [1,2], is the best in terms of the DM output and has by far the most

attractive spectral characteristic, which contains much less unwanted spectral components than all other PWM methods.

The H-bridge output stage of the Class-BD amplifier with the appropriate NBDD modulator and time domain waveforms of the control signals and output voltages are shown in Figure 1.

Figure 1. Class-BD amplifier, using NBDD PWM modulator: (a) Block diagram; (b) time domain waveforms of: NBDD output signals and voltages at DM and CM outputs.

The control signals contain dead time between the switch states where all switches are off to achieve zero voltage switching (ZVS) and to prevent shoot-through currents.

The DM and CM outputs of the NBDD modulation can be expressed after some conversion by the following Double Fourier Series (DFS) expressions [1–3]:

$$F_{NBDD}^{DM}(t) = M \cos(\omega_m t) - 4 \sum_{m=1}^{\infty} \sum_{n=\pm 1}^{\infty} \left\{ \frac{J_n\left(\frac{m\pi M}{2}\right)}{m\pi} \sin\left(\frac{(m+n)\pi}{2}\right) \sin\left(\frac{n\pi}{2}\right) \sin[m\Omega_c + n\omega_m)t - \frac{n\pi}{2}] \right\} = M \cos(\omega_m t) + 4 \sum_{m=1}^{\infty} \sum_{n=0}^{\pm \infty} \left\{ \frac{J_n\left(\frac{2m\pi M}{2}\right)}{2m\pi} \sin\left(\frac{[2m+(2n+1)]\pi}{2}\right) \sin\left[\{2m\Omega_c + (2n+1)\omega_m\}t + \frac{\pi}{2}\right] \right\} \quad (1)$$

$$F_{NBDD}^{CM}(t) = 2 \sum_{m=1}^{\infty} \frac{J_0\left(\frac{m\pi M}{2}\right)}{\frac{m\pi}{2}} \sin\left(\frac{m\pi}{2}\right) \cos(m\Omega_c t) + 2 \sum_{m=1}^{\infty} \sum_{n=\pm 1}^{\infty} \left\{ \frac{J_n\left(\frac{m\pi M}{2}\right)}{\frac{m\pi}{2}} \sin\left(\frac{(m+n)\pi}{2}\right) (1 + \cos n\pi) \cos[(m\Omega_c + n\omega_m)t] \right\} \quad (2)$$

where $\Omega_c = 2\pi f_c$ —switching angle frequency, $\omega_m = 2\pi f_m$ —audio angle frequency, M —modulation index, $M \in [0, 1]$, J_n —Bessel function of n -th order.

Equation (1) shows that effective sampling frequency of the DM output signal is doubled without increasing the transition frequency on the output, and all harmonics around odd multiples of the switching frequency are eliminated. However, the CM output (Equation (2)) reveals some drawback, as the frequency spectrum of the NBDD output contains the odd harmonics of the switching frequency and their even intermodulation (IM) components. The CM output components are present at full scale, even at a very low level of the modulating signal.

Fast switching of the output transistors, nearly rail-to-rail high swings, and wide frequency spectrum of PWM signals can lead to high-frequency RF emissions and interference from the output stage, printed circuit board traces, filter and speaker cables, which become inadvertent antennas [4–7].

A properly designed external LC filter, placed as close as possible to the switching output stage, suppresses the unwanted RF effects, limits the amount of the output ripple current, protects the speaker by attenuating the switching frequency, and also reduces EMI [8–10]. The LC filter for the Class-BD amplifier with NBDD modulation must be designed separately for DM and CM components. Filtration of unwanted components of the spectrum at the DM output is very easy because the NBDD frequency spectrum has no harmonics of the switching frequency, and no IM components around odd multiples of the switching frequency. In terms of DM output, NBDD is the best and has, by far, the most attractive spectral characteristics for all the other NPWM methods.

However, the frequency spectrum of the NBDD CM output contains the odd harmonics of the switching frequency, and their even IM components (2). The CM output components are present at full scale, even at a very low level of the modulating signal. The IM components around the first harmonic of the switching frequency are the most undesirable because they put strong demands on the CM output signals filtering. The output filter of the Class-BD amplifier uses, most often, a common mode choke coil instead of two normal inductors, which results in more effective CM output signal suppression because the CM choke coil exhibits much larger impedance for the CM output current than for the DM one [9,10].

In the last decade, filterless Class-D amplifiers have become very popular [10–12]. The output of the filterless Class-D amplifier is directly connected to a load (speaker), and the load itself provides filtering.

In many recent studies, the theory behind PWM and different modulation schemes, as well as new linearization methods, have been discussed; thus, high-fidelity improvements and EMI reduction of the filterless Class-D amplifiers have been proposed [6,7,12–16].

An original, Common-Mode Free BD (CMFBD) modulation that keeps the CM output constant is presented in [7]. The DM output of this amplifier has the same performance as that using the optimal NBDD modulation; however, the switching frequency of the power MOSFETs creating the new H-bridge output stage is doubled. A detailed analysis of the presented CMFBD modulation shows that it is equivalent to the Phase Shifted Carrier Pulse Width Modulation (PSC PWM) that is considered as a multi-level PWM method for Class-BD amplifiers [1,2].

Figure 2 shows the circuit diagram of the Class-BD output stage, using the PSCPMW modulation scheme and the block diagram of the PSC PWM modulator that generates all control S_1 – S_3 signals [2,7]. The H-bridge contains two additional series switches, M5 and M6, connected parallel with the load, which are used to shunt the bi-directional inductive load current when M1–M4 are off and to set both outputs at $V_{DD}/2$ with the help of shunt resistor R_b connected parallel with M1–M4 transistors. The DM and CM outputs of the PSC PWM modulation can be expressed after some conversion by the following DFS expressions [2,3]:

$$F_{FSC}^{DM}(t) = M \cos(\omega_m t) + 2 \sum_{m=1}^{\infty} \sum_{n=\pm 1}^{\pm \infty} \left\{ \frac{J_n\left(\frac{m\pi M}{2}\right)}{m\pi} \sin\left(\frac{(m+n)\pi}{2}\right) [1 - \cos(n\pi)] \sin[m\Omega_c + n\omega_m]t \right\} =$$

$$= M \cos(\omega_m t) + 4 \sum_{m=1}^{\infty} \sum_{n=0}^{\pm \infty} \left\{ \frac{J_n\left(\frac{2m\pi M}{2}\right)}{2m\pi} \sin\left(\frac{[2m+(2n+1)]\pi}{2}\right) \sin[\{2m\Omega_c + (2n+1)\omega_m\}t] \right\}$$

$$F_{FSC}^{CM}(t) = \frac{1}{2}$$

Figure 2. Class-BD amplifier based on PSC PWM modulation scheme: (a) Block diagram of PSC PWM modulator; (b) the output stage; (c) time domain waveforms at the outputs of the modulator and amplifier.

Comparing Equations (1) and (2) with the corresponding Equations (3) and (4), as well as Figure 1b with Figure 2c, we can see that the DM output of the Class-BD amplifier with the PSC PWM modulation is identical to that one for the optimal NBDD PWM; however, PSC PWM keeps the CM output constant.

The disadvantage of PSC PWM modulation is the need to use two additional series switches, M5 and M6, as well as switching power transistors with twice the frequency of NBDD modulation, which results in higher switching power losses. In addition, power losses occur in shunt resistors R_b connected in parallel with the M1–M4 to set both outputs at $V_{DD}/2$, which also increase the rise and fall times of the PWM output pulses, contributing to a further increase in switching power losses.

The organization of this paper is as follows. Section 2 presents original architectures and implementations of Class-BD audio amplifiers with the balanced CM output. The output stage of each proposed amplifier includes the typical H-bridge with four MOSFETs and four additional MOSFET switches that balance and keep the Common-Mode output constant. The presented amplifiers employ the extended NBDD PWM or PSC PWM modulation schemes. Section 3 presents basic SPICE simulations and experimental studies of the proposed Class-BD amplifiers implemented on the complementary MOSFET pairs. Conclusions are given in Section 4.

2. Class-BD Amplifiers with Balanced CM Output Employing the Extended NBDD PWM or PSC PWM Modulation Scheme

Figure 3a shows a slightly improved version of the Class-BD audio amplifier with a balanced CM output [3], using the extended NBDD PWM modulator (Figure 3c).

Figure 3. Class-BD audio amplifier with balanced CM output, using the extended NBDD PWM modulator: (a) Topology of the output stage, (b) time domain waveforms at the outputs of the modulator and amplifier. (c) Block diagram of the extended NBDD PWM modulator. (d) Floating gate driver with galvanic isolation of the control signal.

This amplifier consists of a typical H-bridge output stage with four MOSFETs, and four additional MOSFET switches (M5, M6 and M7, M8), separating the H-bridge from the power supply, and switching the bridge's power rails to the half-voltage $V_{DD}/2$, at the time intervals in which the MOSFETs of the high-side or the low-side of the H-bridge are closed simultaneously. At these states, when M1, M3 transistors of the high-side are on, M7 is off and M8 is on, whereas when M2, M4 transistors of the low-side are on, M5 is off and M6 is on. The switching frequency of all MOSFETs is the same as for NBDD modulation, i.e., twice as low as that for PSC PWM modulation as shown in Figure 2b.

When all gate drivers UCC27537 have the same turn-on and turn-off propagation delays (according to the datasheet, it is 17 ns), the modulated PWM waveform at the H-bridge output is undistorted and is only delayed in relation to the control signals. These delays do not have to be the same, as it is necessary to introduce an appropriate delay time on the rising edges of all control signals turning on the MOSFETs, with respect to the falling edges of all control signals turning off the MOSFETs. This allows a zero-switching

voltage to be achieved to prevent shoot-through currents during switching processes; however, dead time in particular has the most significant contribution of nonlinearity in the H-bridge output. The optimal turn-on delay time for MOSFETs is a compromise between low shoot-through currents and low switching power losses, and an acceptable THD level at the output of the class D amplifier.

To implement this delay, an input AND gate with two Schmitt Trigger inputs of the UCC27537 were used (Figure 3c). Time constant $R_d C_d$ of the circuit connected to one of the inputs of this gate determines the appropriate delay time on the rising edges of control signal turning on the MOSFET. The gate driver output is connected to the gate of the transistor via a resistor R_G and an anti-parallel Schottky diode, providing turn-off speed enhancement. The ground GND1 of the PWM controller is isolated from the floating ground GND of the driver, using the digital isolator ISO7420 with an insulating barrier made of silicon dioxide (SiO₂).

Figure 3c also shows a self-boost charge pump circuit [16], generating the floating power supply for the gate driver of the M2 transistor; the same solution applies to all other MOSFETs. Continuous switching of MCP1 ensures that the isolated and floating charge pump bias supply is available at all times to the corresponding driver, regardless of the modulation index M and without any interference with the desired phase-leg switching sequence.

Much simpler solutions for gate control systems can be used when the output stage of the amplifier is implemented on complementary MOSFET pairs.

As shown in Figure 4, the gate drivers of all MOSFETs share a common ground GND1 and are directly driven from the NBDD modulator outputs. The block diagram of the NBDD PWM modulator is also simpler (Figure 4d) because the output stage implemented on complementary MOSFET pairs does not need pairs of complementary control signals.

Taking into account that M6 and M8 transistors are supplied with a half voltage $V_{DD}/2$, the supply voltage V_{DD} of this system should be within a limited range, described by the following inequalities:

$$2|V_{GS\min}|_{\text{at } R_{DS(\text{on})\max}} > \frac{V_{DD}}{2} \quad ; \quad V_{DD} < |V_{GS\max}| \text{ and } V_{DD} < |V_{DS\max}| \quad (5)$$

At the higher gate voltage $|V_{GS\min}|$, the drain to source resistance $R_{DS(\text{on})\max}$ in the on state is less than a certain value at which the conduction power losses are still acceptable. $|V_{DS\max}|$ and $|V_{GS\max}|$ are the maximum values for complementary MOSFETs, the most common $|V_{GS\max}| < |V_{DS\max}|$, which result in the following condition: $V_{DD} < |V_{GS\max}|$. Therefore, it is not possible to use the supply voltage higher than $V_{DS\max}$: $V_{DD} < |V_{DS\max}|$.

Figure 4c shows a gate drive circuit with a shifted reference voltage level for the control signals that is suitable for the applications with complementary power MOSFETs with the following supply voltage:

$$V_{DD} < |V_{GS\max} + V_Z| \text{ and } V_{DD} < |V_{DS\max}| \quad (6)$$

Shown in Figure 4c, the gate driver has the ability to control turn-on and turn-off speeds independently for NMOSFET and PMOSFET. The R_G resistor allows adjustment of the MOSFET turn-on speed (R_{Gn} allows to adjust the delay time of the rising edges of the PWM signal, while R_{Gp} allows to adjust the delay time of the falling edges) independently. During turn-off, the antiparallel Schottky diode shunts out serial resistor R_G ; in addition, the gate charge is taken from the parallel C_B capacitor charged to the Zener voltage V_Z , providing turn-off speed enhancement. During the on-time of the switch, a small DC current flows in the level shifter, keeping the driver biased in the right state.

An original Class-BD audio amplifier with a balanced CM output, implemented on complementary MOSFET pairs and employing an extended PSC PWM modulation scheme, is shown in Figure 5a.

Figure 4. Class-BD audio amplifier with balanced CM output, using the extended NBDD PWM modulator and implemented on complementary MOSFET pairs: (a) Topology of the output stage. (b) Time domain waveforms at the amplifier outputs, and PWM control signals with delayed turn-on times for the NMOS and PMOS transistors. (c) Implementation of the turn-on delay times of the NMOS and PMOS. (d) Block diagram of the extended NBDD PWM modulator.

Figure 5b shows the voltage waveforms at the DM and CM outputs of the amplifier, as well as logical combinations of the control signals $\bar{S}_1$, $\bar{S}_2$ and $\bar{S}_3$ with delayed turn-on times for the NMOS and PMOS transistors. Additionally, in this case, the use of complementary transistors in the power stage significantly simplify their control because the gate drivers of all MOSFETs share a common ground $GND1$ and are directly driven from the extended PSC PWM modulator outputs.

Instead of shunting resistors R_b to set both outputs at $V_{DD}/2$ (as in Figure 2b), an additional H-bridge was created by M5, M7 and M6, M8 transistors; however, the lower and upper sides of the new H-bridge are connected to the same power supply $V_{DD}/2$ via oppositely polarized Schottky diodes. Two parallel branches of the serial-connected two NMOSFETs (M6, M8) or PMOSFETs (M5, M7) are connected parallel with the load, and are used to shunt the bi-directional inductive load current when M1–M4 are off and to set both outputs at $V_{DD}/2$. The same implementation of the turn-on delay times of the NMOS and PMOS transistors, as shown in Figure 4c, allows to adjust the delay time of the rising and falling edges of the PWM signal independently. The architecture presented in Figure 5a can be implemented using only NMOSFETs, but galvanic isolation in the transmission path of the control signals as well an isolated and floating bias power supply for gate drivers must be provided.

Figure 5. Class-BD audio amplifier with balanced CM output, using PSC PWM modulation scheme. (a) A new topology of the output stage. (b) Implementation of the turn-on delay times of the NMOS and PMOS. (c) Time domain waveforms at the amplifier outputs and PWM control signals with delayed NMOS and PMOS turn-on times (directly at the gates of these transistors). (d) Block diagram of the extended PSC PWM modulator.

3. Simulation and Measurement Results

SPICE simulations and experimental studies were used to compare the parameters of the proposed class BD amplifiers with a balanced CM output with a prototype, using an optimal NBDD modulation scheme. All Class-BD amplifiers were tested for two different switching frequencies: $F_{c1} = 328$ kHz or $F_{c2} = 164$ kHz, using with each switching frequency two different sets of load resistance as well as the parameter values of the LC output filter: (1) $R_L = 4 \Omega$, $L = 15 \mu\text{H}$, $C = 1.8 \mu\text{F}$; (2) $R_L = 8 \Omega$, $L = 30 \mu\text{H}$, $C = 1 \mu\text{F}$ [8].

Since the proposed amplifiers in Figures 4 and 5 are built on complementary MOSFETs, and the applied supply voltage $V_{DD} = 24$ V exceeds the $V_{GS\text{max}}$ voltage (inequality 6), it was necessary to use a voltage level shifting circuit with a Zener diode ($V_Z = 6.2$ V) to lower the control voltage from the gate driver output (with the exception of MOSFETs, whose sources are connected to the half voltage $V_{DD}/2$ —i.e., Virtual GND “0” V).

Figure 6a,b show the time waveforms of the PWM control signals generated in one selected period T_c , as well as the drain currents $I(M1:D)$ – $I(M4:D)$ and $I(M5:D)$ – $I(M8:D)$ of the power MOSFETs in Figures 4 and 5, respectively. Optimal turn-on delay times of the transistors were adjusted by selecting the resistance values R_{Gn} and R_{Gp} (Figures 4c and 5b).

In our design, for $R_{Gp} = 68 \Omega$ and $R_{Gn} = 150 \Omega$, we obtain the optimal turn-on delay times of the transistors and significant limitation of the shoot-through currents.

Figure 6. Time waveforms of the PWM control signals generated in one selected period T_c , and the drain currents of the power MOSFETs in the circuits shown: (a) in Figure 4, (b) and Figure 5, respectively.

Figure 7a–c shows the efficiency and the output power versus modulation index M as well as THD as a function of the signal frequency for three Class-BD amplifiers: Figure 7a, shown in Figure 1 with the conventional NBDD modulator; Figure 7b, shown in Figure 4 with the extended NBDD PWM modulator; and Figure 7c, shown in Figure 5 with the extended PSC PWM modulator. These characteristics were determined for two different switching frequencies, with two sets of load resistance value as well as LC output filter parameter values, for each frequency. As we can see, the output power characteristics of all three amplifiers are almost identical, while the efficiencies of the two proposed amplifiers,

containing four additional transistor switches to balance the CM outputs, are slightly lower to the efficiency of the prototype NBDD modulator amplifier, due to the additional power losses in the conduction states and in the switching processes of these additional transistor switches.

(a) Class-BD amplifier shown in Figure 1 with conventional NBDD modulator

(b) Class-BD amplifier shown in Figure 4 with extended NBDD PWM modulator

(c) Class-BD amplifier shown in Figure 5 with extended PSC PWM modulator

(1) —■— $R_L = 8 \Omega$; $F_c = 164 \text{ kHz}$
 (3) —▲— $R_L = 8 \Omega$; $F_c = 328 \text{ kHz}$

(2) —●— $R_L = 4 \Omega$; $F_c = 164 \text{ kHz}$
 (4) —▼— $R_L = 4 \Omega$; $F_c = 328 \text{ kHz}$

Figure 7. Efficiency and output power vs. modulation index M , as well as THD as a function of the audio signal frequency for three amplifiers shown (a) in Figure 1, (b) in Figure 4, and (c) in Figure 5, respectively.

As we can see in Figure 7, all tested amplifiers show, however, slight distortions at the DM outputs, caused by distorted switching sequences generated by the output stages of these amplifiers. Switching timing error in a gate signal, due to turn-on delay times of the transistors, in particular, has the most significant contribution of nonlinearity in DM output stages. Based on Figure 7a–c, we can observe the following interesting properties. The proposed Class-BD amplifiers have a slightly higher THD than the prototype amplifier in Figure 1 with the conventional NBDD modulation. This is because the proposed amplifiers are controlled by modulators generating control signals with extended timing, giving more timing errors added in each switching period T_c by the gate drivers, such as dead time, t_{on}/t_{off} and t_r/t_f . THD of all tested amplifiers is higher for the higher switching frequency $F_{c1} = 328$ kHz than for $F_{c2} = 164$ kHz because relative timing errors are greater for shorter switching period T_c .

For example, Figure 8a–c shows the simulated THD + N frequency responses in the band up to 30 kHz for the three tested amplifiers at two switching frequencies $F_{c1} = 328$ kHz and $F_{c2} = 164$ kHz, modulating frequency $f_m = 1$ kHz, modulation index $M = 0.95$, load resistance $R_L = 8 \Omega$, and filter parameters $L = 30 \mu\text{H}$ and $C = 1 \mu\text{F}$.

Figure 8. Cont.

(c) Class-BD amplifier shown in Figure 5 with extended PSC PWM modulator

Figure 8. Simulated THD + N frequency responses of three tested amplifiers in the band up to 30 kHz.

Figure 9 shows the voltage oscillograms measured at the following outputs of the proposed Class-BD amplifier with the PSC PWM modulator in Figure 5: right half bridge, left half bridge, DM output, and CM output before and after filtration. We obtain quite similar oscillograms for the Class BD-amplifier with the NBDD modulator in Figure 4. A comparison of the output voltages on the right half bridge, left half bridge and CM output, presented in Figures 5 and 9, shows that the real-time waveforms are distorted by overlapping spikes on the rising and falling edges of the PWM pulse in each switching period. The main source of these spikes are timing errors added in each switching period T_c by the gate drivers, such as dead time. The inevitability of timing errors is due to the fact that the turn-on delay times of the NMOS and PMOS transistors have to be implemented by independently adjusting the delay times of the rising and falling edges of the PWM driving signals. Even with equal turn-on delay times of the NMOS and PMOS, during the dead time, the inductor current in the output LPF turns on the body diode. During the next phase when the other side of the MOSFET starts to turn on at the end of the dead time, the body diode stays in a conducting state unless the stored minority carrier is fully discharged. This reverse recovery current tends to have a sharp, spiky shape and leads to unwanted distortion by overlapping spikes on the rising and falling edges of the PWM pulse in each switching period. However, the filtration of the appearing spikes at the CM output is very easy, even when the filter inductance L is very small, as is shown in the oscillogram in Figure 9.

(a) Left-half and right-half H-bridge outputs before (left) and after (right) filtration

Figure 9. Cont.

(b) Differential Mode output V_{OUT}^{DM} before (left) and after (right) filtration

(c) Common-Mode output V_{OUT}^{DM} before (left) and after (right) filtration

Figure 9. Oscillograms measured at the following outputs of the Class-BD amplifier in Figure 5: (a) Left-half and right-half H-bridge outputs, (b) DM output, (c) CM output (in the left column before, in the right column after filtration); $F_{c2} = 164$ kHz, $f_m = 10$ kHz; vertically: 1 div/5 V; horizontally: 1 div/5 μ s; $V_{DD} = 24$ V.

Figure 10 shows the PCBs of the tested Class-BD audio amplifiers with balanced CM output, implemented on complementary pairs HEXFET® Power MOSFET IRF9389PbF: (a) shown in Figure 4, using the extended NBDD PWM modulator; and (b) shown in Figure 5, using the extended PSC PWM modulator. To test a typical Class-BD amplifier in a H-bridge configuration with a classic NBDD PWM modulator (as shown in Figure 1 but with complementary MOSFETs), the main H-bridge of the amplifier in Figure 10a was used. To implement such a configuration, pins: drain-source of M5, M7 transistors should be galvanically connected, while M6 and M8 should be permanently open. Electronic components on PCBs have the same symbols as in Figures 4 and 5. Load resistances of 4 Ω , 65 W or 8 Ω , 35 W are attached to PCBs with short cables from the outside.

The following set of equipment was used to test the amplifiers:

- Rigol DG1032Z function generator;
- Rigol DSA832E spectrum analyzer, 9 kHz ~ 3.2 GHz;
- Hp 8593 agilent spectrum analyzer, 1 kHz ~ 2.9 GHz;
- DSO4254B advanced digital oscilloscope 4 $\times$ 250 MHz.

a)

b)

Figure 10. The PCBs of the tested Class-BD audio amplifiers with balanced CM output, implemented on complementary pairs HEXFET® Power MOSFET IRF9389PbF: (a) shown in Figure 4, using the extended NBDD PWM modulator; (b) shown in Figure 5, using the extended PSC PWM modulator.

4. Final Conclusions

Two original open-loop Class-BD audio amplifiers with balanced Common-Mode outputs were described and tested. The output stage of each proposed amplifier includes the typical H-bridge with four MOSFETs and four additional MOSFET switches that balance and keep the CM output constant. Each of the amplifiers employs the extended NBDD PWM or PSC PWM modulation scheme and was implemented on complementary power MOSFET pairs: HEXFET® IRF9389PbF.

Extensive simulation studies in SPICE and experimental studies have shown that the proposed Class-BD amplifiers have almost the same audio performance on the DM outputs as the prototype Class BD amplifier with the optimal NBDD modulation and, at the same time, have balanced constant voltage CM outputs, thus enabling the implementation of the true, filterless Class-BD amplifiers. The filtration of unwanted spectral components at

the DM output of the tested amplifiers is very easy because the frequency spectrum has no harmonics of the switching frequency, and no IM components around odd multiples of the switching frequency. Since these amplifiers simultaneously have balanced CM outputs, with a constant $V_{DD}/2$ voltage at this output, the output filter can be dramatically reduced, or rather eliminated, while significantly lowering radiative electromagnetic interference (EMI).

The implementation of the amplifier output stage on complementary MOSFET pairs is much easier than only on NMOSFET transistors because the gate drivers of all MOSFETs share a common ground GND1 and are directly driven from the NBDD or PSC PWM modulator outputs, the gate drivers are powered from the same voltage as the output stage, and the complementary MOSFET pairs do not need pairs of complementary control signals. To supply the proposed amplifiers with a voltage of 24 V, i.e., greater than $|V_{GSmax}|$ (according to the datasheet it is 20 V), it was designed and applied a gate drive circuit with a level voltage shifter with Zener diode for the control signals that is suitable for applications with complementary power MOSFETs with the following supply voltage: $V_{DD} < |V_{GSmax} + V_Z|$ and $V_{DD} < |V_{DSmax}|$. This gate drive circuit has also the ability to control turn-on and turn-off speeds independently for NMOSFET and PMOSFET.

Extensive experimental and simulation studies in SPICE have shown that the proposed class BD amplifiers have almost the same audio performance on the DM outputs as the prototype Class-BD amplifier with the optimal NBDD modulation.

The output power and the efficiency versus modulation index M , as well as THD as a function of the signal frequency, have been tested for two proposed Class-BD amplifiers and the prototype Class-BD amplifier with the optimal NBDD modulation (Figure 7) for the two switching frequencies, $F_{c1} = 328$ kHz and $F_{c2} = 164$ kHz, using, with each switching frequency, two different load resistances: $R_L = 4 \Omega$ and $R_L = 8 \Omega$.

The audio performance on the DM outputs of the three tested amplifiers, for the following:

- (a) $F_{c1} = 328$ kHz, $R_L = 4 \Omega$, $f_m = 1$ kHz, $M = 0.95$;
- (b) $F_{c1} = 328$ kHz, $R_L = 8 \Omega$, $f_m = 1$ kHz, $M = 0.95$;
- (c) $F_{c2} = 164$ kHz, $R_L = 4 \Omega$, $f_m = 1$ kHz, $M = 0.95$;
- (d) $F_{c2} = 164$ kHz, $R_L = 8 \Omega$, $f_m = 1$ kHz, $M = 0.95$;

are as follows:

1. Prototype Class-BD amplifier with conventional NBDD modulator:
 - (a) $P_L = 61.16$ W, $\eta = 97.01\%$, $THD = 0.683\%$;
 - (b) $P_L = 32.88$ W, $\eta = 97.80\%$, $THD = 0.635\%$;
 - (c) $P_L = 59.48$ W, $\eta = 97.37\%$, $THD = 0.102\%$;
 - (d) $P_L = 32.19$ W, $\eta = 98.29\%$, $THD = 0.078\%$.
2. Class-BD amplifier shown in Figure 4 with extended NBDD PWM modulator:
 - (a) $P_L = 56.71$ W, $\eta = 94.62\%$, $THD = 0.784\%$;
 - (b) $P_L = 31.01$ W, $\eta = 95.02\%$, $THD = 0.742\%$;
 - (c) $P_L = 56.93$ W, $\eta = 97.37\%$, $THD = 0.085\%$;
 - (d) $P_L = 31.35$ W, $\eta = 96.72\%$, $THD = 0.065\%$.
3. Class-BD amplifier shown in Figure 5 with extended PSC PWM modulator:
 - (a) $P_L = 57.80$ W, $\eta = 95.27\%$, $THD = 0.752\%$;
 - (b) $P_L = 31.01$ W, $\eta = 96.38\%$, $THD = 0.707\%$;
 - (c) $P_L = 57.16$ W, $\eta = 95.76\%$, $THD = 0.071\%$;
 - (d) $P_L = 30.53$ W, $\eta = 97.10\%$, $THD = 0.099\%$.

Comparing the above listed audio performance on the DM outputs of the three tested amplifiers, we can see that the proposed Class-BD amplifiers have lower efficiency of about 1 to 2% than the prototype Class-BD amplifier with the conventional NBDD modulation, due to higher conduction losses in a greater number of transistor switches in the output stages. They have also a slightly higher THD of about 0.1% than the prototype amplifier with the conventional NBDD modulation because they are controlled by extended

modulators, giving more timing errors added by the gate driver in each switching period T_c . THD of all tested amplifiers is higher by about 0.6% for the higher switching frequency $F_{c1} = 328$ kHz than for $F_{c2} = 164$ kHz because relative timing errors are greater for shorter switching period T_c .

Class-BDD amplifiers with CM balanced output can successfully use a not very high switching frequency (in our design $F_{c2} = 164$ kHz), resulting in higher efficiency and lower THD , even with a reduced LC output filter.

The proposed open-loop Class-BD audio amplifiers with balanced CM outputs are true, filterless Class-D amplifiers with significantly reduced electromagnetic radiation interference (EMI). In practice, due to imperfect waveforms of the voltages controlling the MOSFET transistors, spike pulses are generated at the CM output of the amplifier, which are easy to filter by the reduced LC output filter, even at a very low inductance L .

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