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Mechanism Analysis of Dynamic On-State Resistance Degradation for a Commercial GaN HEMT Using Double Pulse Test

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Abstract: The dynamic on-resistance (R_{ON}) behavior of one commercial GaN HEMT device with p-GaN gate is investigated under hard-switching conditions. The non-monotonic performance of dynamic R_{ON} with off-state voltage ranging from 50 to 400 V is ascribed to the "leaky dielectric" model. The highest normalized R_{ON} value of 1.22 appears at 150 and 200 V. The gradual increase and following maximum of dynamic R_{ON} are found when the device is exposed to a stress voltage for an extended stress time under 100 and 200 V, which is due to a much longer trapping time compared to detrapping time related to deep acceptors and donors. No obvious R_{ON} degradation, thanks to the suppressed trapping effect, is observed at higher V_{DS}. From the multi-pulse test, the dynamic R_{ON} is seen to be insensitive to the frequency. It is demonstrated that the leakage, especially under source and drain contact, is a key issue in the dynamic resistance degradation.

Keywords: gallium nitride (GaN); high electron mobility transistor (HEMT); dynamic on-resistance (R_{ON}); leakage; double pulse test (DPT)

1. Introduction

GaN-based power devices, such as high electron mobility transistor (HEMT), are promising in the field of high-frequency, high-power, low-loss converters [1]. Understanding its characteristics is very helpful for better using those devices in power electronics systems. However, the degradation of the dynamic on-state resistance R_{ON} after switching from high voltage off state hinders the practical application of these devices. Now, two physical mechanisms have been proposed to explain R_{ON} degradation. One is the trapped electrons [2,3] coming from the surface traps between the gate and drain area and/or the buffer traps under the two-dimensional electron gas (2DEG) channel induced by high electric field across the drain-to-substrate in the off state. The other is hot electrons [4,5], generated in the channel, which can be injected to and trapped at the surface or the buffer stack during the high voltage switching transients. Though several advanced device technologies, such as filed plate [6] and optimized buffer design [7], have been performed to release the current collapse, dynamic R_{ON} variation is still a big problem for currently commercial GaN devices. Previously, most reports focus on the device level analysis or research for material quality enhancement. In this case, the impact of dynamic on-state resistance should be fully investigated to predict the accurate performance of a GaN converter, and it is better not to use the static R_{ON} values for the evaluation of conduction loss.

The double pulse test (DPT) is a widely used methodology to achieve the dynamic R_{ON} of the power devices when switching under hard conditions [8–12]. The switching

transients of device under test (DUT) can be captured at the second pulse under desired voltage and current. Thus, the rise of junction temperature ascribed to the switching loss can be ignored. The impact on dynamic R_{ON}, including off-state time, off-state voltage, drain current, temperature, frequency, duty cycle and gate voltage, can be investigated by using this method. Moreover, DPT results can provide some guidance for converter design, such as switching frequency and dead-time selections, thermal management, and efficiency estimation [13,14]. The impact of gate characteristics [15], off-state voltages [14,16], and continuous operating mode has [17] already been discussed. The off-state time before the first gate pulse is one of the key parameters, which can affect the trapping effect and thus results in uncertainty of the R_{ON} value. However, few reports can be found to discuss this issue.

In this paper, the DPT evaluation method was carried out for further understanding of dynamic on-state resistance by investigating the impact of the off-state time before the first gate pulse, the off-state voltage and by the continuous switching operation with two frequencies. The DUT was a commercially purchased GaN normally-off device with a p-type GaN gate from GaN System (GS66504B [18]) with the typical R_{ON} of 100 mΩ.

2. Experimental Details

The test circuit schematic used in this paper is shown in Figure 1a, which is widely adopted DPT half-bridge configuration for hard-switching conditions. The control signals are well described previous works [11,17]. The clamping circuit [19] is introduced to avoid saturating the amplifier of the oscilloscope channel, and to ensure accurate results by maintaining the maximum vertical resolution. The method is based on a high voltage, fast-switching zero recovery SiC Schottky diode and a Zener diode. When the DUT is at the off state, which means there is a high voltage supplied (several hundred volts) between source and drain, the diode D3 is also at the off state under a reverse bias. The current flows through low power supply, resistance and a Zener diode. The measured voltage is clamped at the regulation value, which is much lower than the real DUT's off-state voltage. When the DUT is turned on, the real on-state voltage equals to the measured value subtracting the voltage drop on diode D3. The corresponding homemade test board is depicted in Figure 1b.
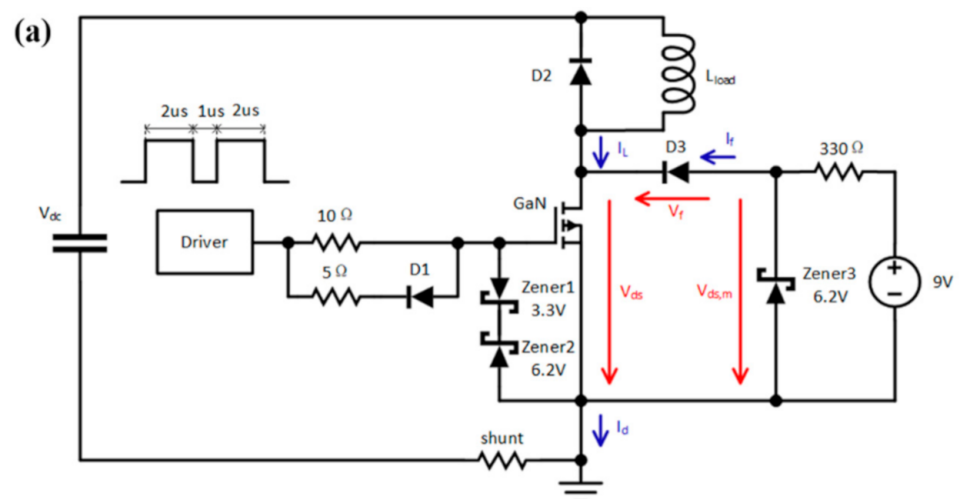

Figure 1. *Cont.*
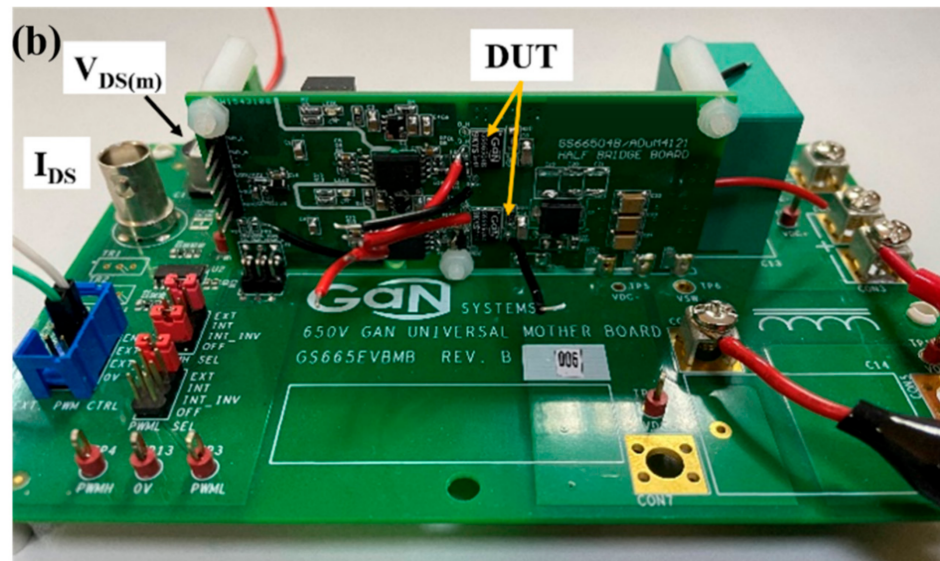
Figure 1. (**a**) Gallium nitride-high electron mobility transistor (GaN-HEMT) dynamic on-state resistance test circuit for hard-switching conditions with clamping circuit; (**b**) actual test board.

The practical testing system includes a DC power supply (HSPY-1000-01), an oscilloscope (Tektronix@MDO3054), an auxiliary power supply (KEITHLEY@2231A-30-3, Keithley Instruments, Solon, OH, USA), a function generator (Tektronix@AFG1022, Tektronix, Beaverton, OR, USA) and a test board.

The actual waveform of the DUT under 50 V off-state voltage is shown in Figure 2. The blue, light blue, purple and green lines indicate the gate voltage (V_{GS}), the drain voltage (V_{DS}), the drain current (I_{DS}) and the clamping voltage ($V_{DS(m)}$). Before t_0, the DUT is under high V_{DS} (ranging from 50 V to 400 V) for a controllable stress time. At t_0, the DUT switches to on-state until t_1, whose duration is 2 μs. At t_1, the current through the DUT increases to 5 A. After an interval of 1 μs, the DUT turns on again for another 2 μs under the second pulse. The device current rises to 10 A at the end of the second pulse. Then, the test finishes at t_3 when the DUT is switched off. The dynamic on-state resistance is measured and calculated at 1.96 μs during the second on-state time.
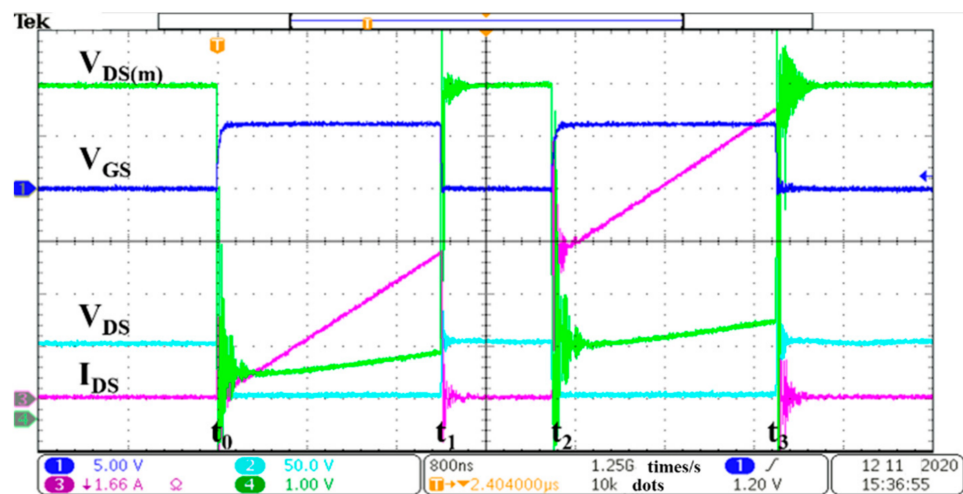

Figure 2. The real waveform of tested gate voltage (V_{GS}, blue line), drain and source voltage (V_{DS}, cyan line), measured V_{DS} (green line), and drain current (I_{DS}, purple line).

3. Results

Figure 3 displays the dynamic R_{ON} variation with different stress voltages ranging from 50 to 400 V; the step is 50 V. The I_{DS} keep the same at 10 A for each voltage, which is adjusted by the external inductor. The detailed value is given in Table 1. At each specific off-state voltage, the dynamic R_{ON} is tested three times. Additionally, for the accuracy, the test interval is 20 min to completely release the trapped electrons. The normalized R_{ON} is the value of measured dynamic R_{ON} values divided by the static on-resistance value extracted from output curves at room temperature.
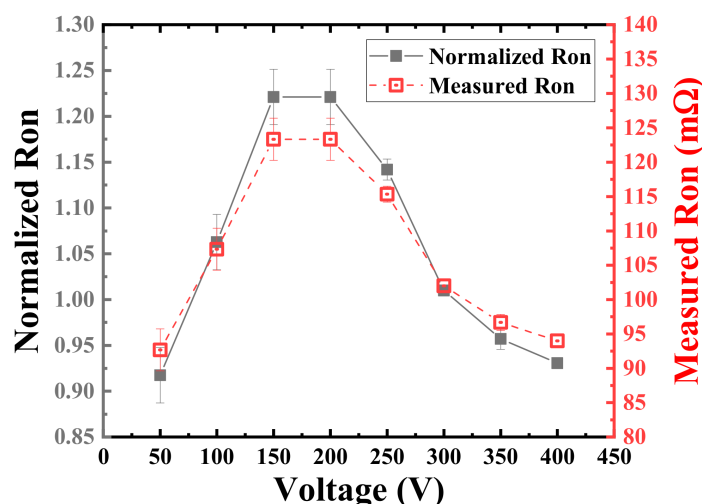

Figure 3. Normalized and measured dynamic on-resistance (R_{ON}) value at 1.96 µs after turn on for different voltage stresses by the double pulse test (DPT) method.

Table 1. Inductors corresponding to the different off-state voltages.

V_{DC} (V)	50	100	150	200	250	300	400
Inductor (µH)	20	40	60	80	100	120	160

The device has an evident dynamic R_{ON} increase as the voltage initially increases to 150 V, which is consistent with the common understanding of GaN HEMTs [14–17,19]. Additionally, the dynamic on-resistance degradation is not severe with the highest value of 1.23 at 150 and 200 V. The growing dynamic on-resistance under lower off-state voltage can be explained by the "leaky dielectric" model related with charge storage [20]. The leakage path, which exists between the source and drain contact and the highly resistive carbon-doped GaN layer, allows a hole current to flow from the drain contact into the C-doped layer and forms negatively charged regions at the unintentionally doped (UID)–GaN/C-doped GaN interface as the V_{DS} increases. This negative charge reduces the 2DEG density and leads to the increase in dynamic R_{ON}. Another fact for the dynamic on-resistance increases is the hot electron injection, which is due to the overlap of V_{DS} and I_{DS} under hard-switching conditions [4].

However, after experiencing a maximum with the range around 50 V, the dynamic R_{ON} starts to decline as the V_{DC} further increases. The descent rate is getting slower and slower. This non-monotonic phenomenon is different from the previous report under the hard-switching conditions [17]. In Reference [17], the authors found similar behavior in a GaN device with a hybrid drain-embedded (HD) structure [21], since the p–n junction in the HD structure endures a voltage drop caused by high channel current when the DUT switches on at a high V_{DS}. It can inject holed into buffer layer to alleviate the current collapse effect by releasing the trapped electrons during the high voltage stress, thus decreasing the dynamic R_{ON}. The point is that there is no HD structure in the tested DUT in this

paper despite the unknown detailed structure. However, some reasonable explanations can be proposed based on the same point of view (decrease in trapped electrons or increase in holes). The enhanced vertical leakage through the whole area between source and drain [20,22], trapping at donor defects [23], and the two-dimensional hole gas (2DHG) formed at the interface of C-doped GaN and strain relief layer [24] under high V_{DS} will result in a decrease in the number of trapped electrons that cause the reduction in dynamic on-resistance.

For the clarification of the voltage stress superposition effect on the dynamic R_{ON}, the time-dependent test is implemented as follows. In Figure 4, normalized R_{ON} is plotted versus increasing stressing time under four individual off-state voltages. The DPT is triggered every one minute at a fixed V_{DS}. The curves clearly show that the dynamic Ron degradation is more severe at lower voltage after a period of stress. One of the reasons is the long-time stressing operation which will lead to increased trapping during the off-state and the shorter detrapping time which occurs only during the on-state in each DPT test [4,10]. The accumulated trapping effect is ascribed to both reasons and leads to the increase in dynamic R_{ON}. Moreover, a longer trapping time constant associated with deep acceptors and donors as charge reservoirs [20] contributes to the gradual increase in the dynamic on-state resistance in the first 2–3 min.
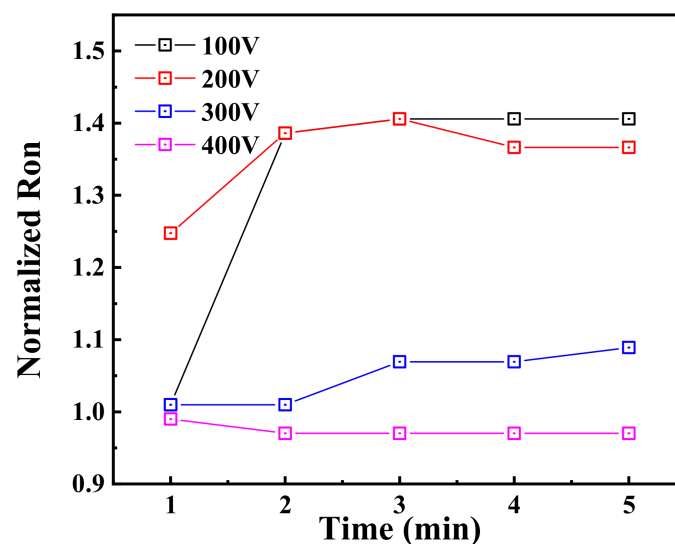

Figure 4. Normalized R_{ON} value for increasing stress times with the interval of 60 s at off-state voltage from 100 to 400 V.

The resistance increase under 300 V in 5 min is only 8%. At 400 V, the dynamic R_{ON} does not even vary with the extended stressing time. A similar phenomenon has been found in the earlier papers [4,25]. They associate this attribution with the field plate normally utilized in the enhancement-mode GaN HEMT devices. This is because the field plate, which is placed between the gate and drain, induces a lateral electric field and inhibits the electron trapping in this area, especially at higher drain and source voltage. Likewise, this suppression is less effective because lateral electric field weakens as the off-state voltage decreases.

Figure 5 shows that the dynamic R_{ON} increases with a shorter stress time interval of 10 s when the voltage is fixed at 100 V. It is seen that the dynamic on-state resistance of the DUT displays a gradually increased tendency, indicating that the trapping of electrons is a cumulative process. The phenomenon of this gradual increase can be explained as the response to the donor/acceptor in the UID and/or C-doped GaN layer caused by not only the intrinsic trap time constant but also the charge transport in the buffer stack [20], which takes longer time.
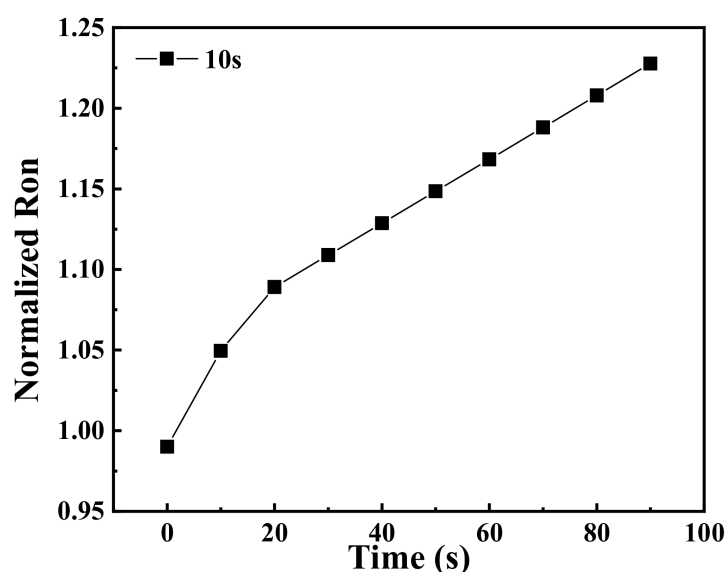
Figure 5. Normalized R$_{ON}$ value for increasing stress times with shorter intervals at 100 V off-state voltage.

In order to simulate the real working situation of the GaN HEMT device in a converter, the continuous operation was carried out to evaluate the dynamic on-resistance under two frequencies of 250 and 500 kHz. The actual waveform of 250 kHz under 100 V off-state voltage is shown in Figure 6. The heat dissipation, ascribed to conduction loss, can be estimated by the by $P = IR^2$. The current and dynamic on-resistance are 10 V and 100 mΩ, respectively. Take the duty cycle of 0.5 into account, the heat dissipation power is less than 5 W. So, the maximum temperature increase is 5 °C to the bottom side. Additionally, the total evaluation time is limited to 100 μs to avoid self-heating.

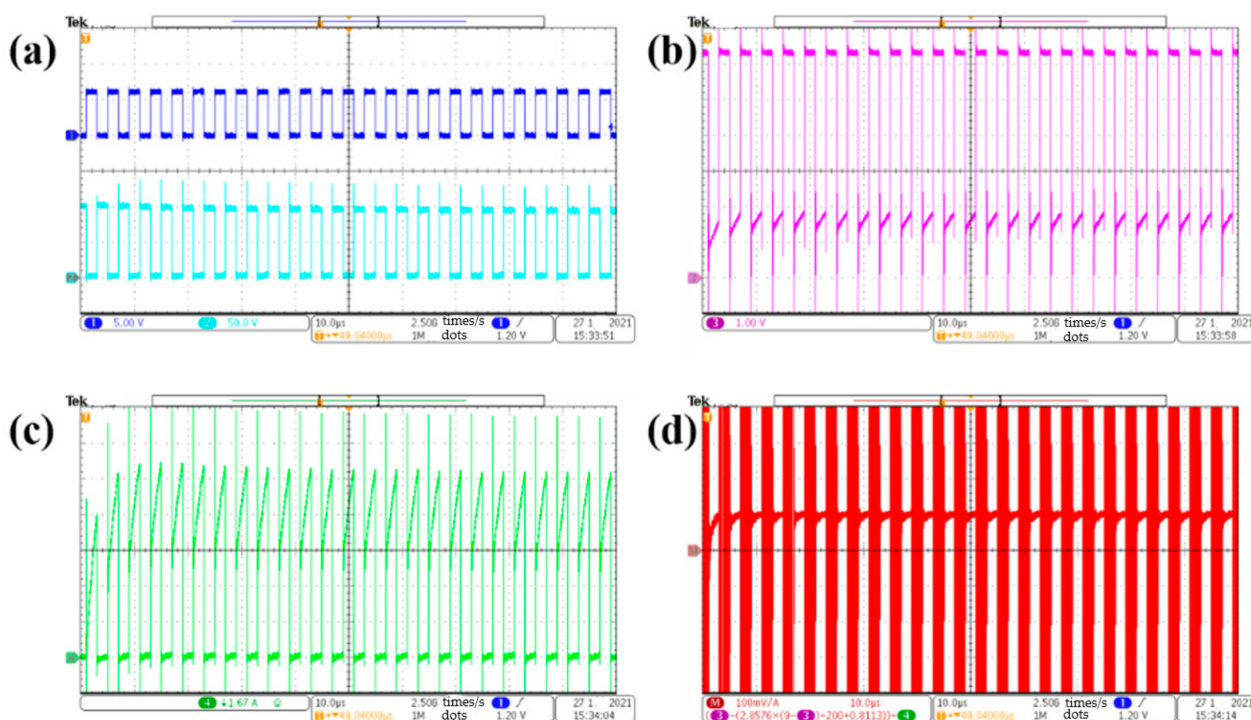**Figure 6.** The real waveform of a multi-pulse test at 100 V and 250 kHz: (**a**) V$_{GS}$ and V$_{DS}$; (**b**) V$_{DS(m)}$; (**c**) I$_{DS}$; (**d**) dynamic R$_{ON}$.

The measured dynamic R_{ON} is plotted in Figure 7 with the total continuous operation time. The multi-pulse test is implemented only for 100 V off-state voltage since the dynamic on-resistance performs a more severe increase. For both frequencies, the resistance increases in the first 10 μs and then gets to a nearly steady value with the increase in pulse number. The results of multi-pulse measurement are consistent with that of DPT [17]. Additionally, there is no difference in the steady value between 250 and 500 kHz, which means that the frequency does not affect the dynamic R_{ON}. It indicates that the trapping during the high-power switching and detrapping during the on-state reach an equilibrium in a very short time for a high-frequency switching operation. It can be interpreted by the deep level trap with a longer time constant. Unlike the test in Figure 4, the off-state time is 2 μs in each pulse, meaning the electrons do not have enough time to respond to the high frequency.
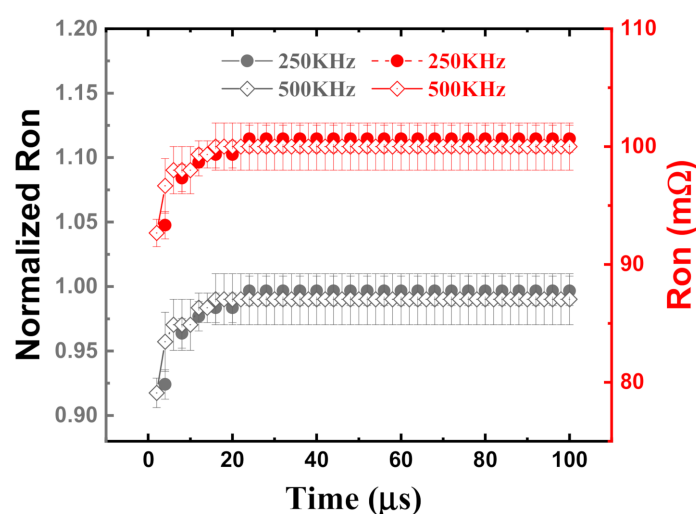

Figure 7. Normalized and measured dynamic R_{ON} value at 1.96 μs in every pulse under 250 kHz and 500 kHz.

It is well acknowledged that dynamic R_{ON} is more sensitive to frequency under hard-switching conditions attributed to hot electrons [26]. However, based on the results above, it is assumed that a leaky dielectric mechanism should contribute more to the increase in dynamic on-resistance in a voltage stress experiment, as discussed in Figure 3.

4. Conclusions

In this paper, we investigated the dynamic on-resistance behavior of one commercial GaN HEMT device with p-GaN gate under hard-switching conditions. The dynamic R_{ON} shows a non-monotonic performance, which initially increases to 1.22 times the static value and then decreases with the increasing off-state voltage. The stress time dependence of dynamic R_{ON} with various V_{DS} displays different characteristics. Only under lower V_{DS} does dynamic R_{ON} increase gradually and reach a saturated level. The electron trapping effect was weakened when the field plate was applied as the common technology in GaN HEMT, resulting in no obvious rise of R_{ON}. The multi-pulse test, matched to the practical application, implies little frequency correlation and dynamic resistance degradation. All the results suggest that the leakage in the dielectric plays an important role in the dynamic performance. More quantitative investigations should be implemented to fully understand the dynamic characteristics of GaN HEMT.

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Data Availability Statement: Experimental data is available upon request.

Conflicts of Interest: The authors declare no conflict of interest.

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