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Analytical Current–Voltage Modeling and Analysis of the MFIS Gate-All-Around Transistor Featuring Negative-Capacitance

Yeji Kim, Yoongeun Seon, Soowon Kim, Jongmin Kim, Saemin Bae, Inkyung Yang, Changhyun Yoo, Junghoon Ham, Jungmin Hong and Jongwook Jeon *

Department of Electrical and Electronics Engineering, Konkuk University, Seoul 05029, Korea; yeji98@konkuk.ac.kr (Y.K.); tjsdbsrms@konkuk.ac.kr (Y.S.); sw4292@gmail.com (S.K.); jongmin94kr@hanmail.net (J.K.); bsm9116@naver.com (S.B.); kyoung123123@naver.com (I.Y.); hero0056@naver.com (C.Y.); jhham5969@naver.com (J.H.); hjmin0208@naver.com (J.H.)

* Correspondence: jwjeon@konkuk.ac.kr; Tel.: +82-2-450-3494

Abstract: Recently, in accordance with the demand for development of low-power semiconductor devices, a negative capacitance field-effect-transistor (NC-FET) that integrates ferroelectric material into a gate stack and utilizes negative capacitive behavior has been widely investigated. Furthermore, gate-all-around (GAA) architecture to reduce short-channel effect is expected to be applied after Fin-FET technology. In this work, we proposed a compact model describing current–voltage (I–V) relationships of an NC GAA-FET with interface trap effects for the first time, which is a simplified model by taking proper approximation in each operating region. This is a surface potential-based compact model, which is suitable for evaluating the I–V characteristics for each operating region. It was validated that the proposed model shows good agreement with the results of implicit numerical calculations. In addition, by using the proposed model, we explored the electrical properties of the NC GAA-FET by varying the basic design parameters such as ferroelectric thickness (t_{fe}), intermediate insulator thickness (t_{ox}), silicon channel radius (R), and interface trap densities (N_{it}).

Keywords: negative capacitance (NC) FET; gate-all-around (GAA) FET; compact model

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1. Introduction

When the MOSFET (metal-oxide semiconductor FET) technology was reduced to around a 20 nm technology node, the off current increase caused by the short-channel effect made it difficult to utilize any more planar-type MOSFET device structures. For this reason, the ultra-thin semiconductor-on-insulator (UTSOI) structure that can effectively reduce the effect of the source–drain region on the channel region and the FinFET structure using a three-dimensional (3D) channel structure to improve gate controllability has been proposed to enable continuous scaling down of CMOS (complementary metal-oxide semiconductor) technology. However, the FinFET, having a multi-gate structure, has a limitation in scaling down at a technology node of 5 nm or less, so the introduction of a GAA type MOSFET structure is being considered to improve the gate control capability [1,2]. As well as such a multi-gate architecture, various device structures using a junction-less transistor structure or a channel material other than silicon have been proposed for various applications [3–6].

In addition to the introduction of new transistor architectures, reducing power consumption of the transistor has become a very important issue [7,8]. This is because the density of power consumption inside the semiconductor chip increases exponentially as the number of semiconductor elements integrated in a unit area increases. Such an increase in temperature in semiconductor chips causes the clock frequency of the CPU to be stagnant beyond a certain frequency (~3 GHz), making it a big bottleneck for improving CPU performance [9]. In addition, energy-saving ultra-low-power semiconductor technology is urgently required for semiconductor technology for Internet of Things (IoT) applications to

build an ultra-connected society [10]. So, various transistor technologies have been proposed to solve the problem of power consumption density, which increases exponentially as the number of semiconductor technology nodes decreases. Representative examples of low-power semiconductors are NC-FET [11–13] and tunneling-FET (T-FET) [14–16]. For transistor-level integrated circuit design, it is essential to develop a compact model based on transistor device physics to simulate electrical characteristics such as current–voltage of integrated circuits in electronic design automation (EDA) software such as SPICE. Compact models based on threshold voltage (V_{th}) of transistor devices have been widely used for a long time, but recently, compact models based on channel surface potential with improved convergence and linearity characteristics have been developed and widely used. Representative examples of V_{th} -based and surface potential-based models are the BSIM4 (Berkeley short-channel IGFET model) and BSIM-CMG (common multi-gate), respectively [17,18].

Recently, an NC GAA-FET having a metal-ferroelectric-insulator-semiconductor (MFIS) type has been investigated by introducing NC characteristics to a gate stack as a next-generation semiconductor in a GAA transistor [19,20]. In addition, it has been reported that interface traps at the Si–SiO₂ interface can result in the degradation of transistor performance (e.g., sub-threshold swing) [21], the process-variable ΔV_{th} [22], and negative bias temperature instability (NBTI)-induced ΔV_{th} [23]. This interface trap effect has been considered important from before in silicon GAA-FET without ferroelectric material, and compact modeling methodologies have been proposed [24]. Therefore, as mentioned, an accurate physical-based model is required for the design of integrated circuits of NC GAA-FETs with consideration of interface traps. Amol D. Gaidhane et. al. presented a comprehensive current–voltage model of NC GAA-FET based on the channel surface potential [25]. The model proposed by Amol D. Gaidhane et. al. combines the previously presented GAA-MOSFET model [26–30] with a Landau–Devonshire (LD) Equation that describes the NC properties of ferroelectric materials to obtain the surface potential approximately, and solves the current Equation based on the surface potential. Although previous work [25] has accurate results, the complexity of formulas makes it difficult for semiconductor device and circuit designers to have an intuition to the electrical characteristics of NC GAA-FET through the derived model equation. In addition, the effect of interface traps was not considered.

In this work, simple and analytical current–voltage equations of NC GAA-FET in each operating region, such as linear, saturation, and sub-threshold regions, are derived, and the proposed model, for the first time, takes the interface traps at Si–SiO₂ of NC GAA-FET. In addition, by using the proposed model, the device electrical behaviors according to the basic device design parameters such as t_{fe} , t_{ox} , R , and N_{et} were explored.

2. Method of Calculating Surface Potential of NC-GAA FET

The considered NC GAA-FET is shown in Figure 1 as an undoped channel and cylindrical GAA structure. Source and drain regions are highly doped, ignoring parasitic resistance effects in these regions. The gate stack consists of a metal gate-electrode/ferroelectric/bottom insulator/semiconductor where the bottom insulator layer is SiO₂. Following the gradual channel approximation (GCA) and considering cylindrical coordinates, the general one-dimensional Poisson’s Equation of the intrinsic channel region of NC GAA-FET can be expressed as

$$\frac{d^2\varphi}{dr^2} + \frac{1}{r} \frac{d\varphi}{dr} = \frac{q}{\epsilon_{si}} n(r) \quad (1)$$

where q is the electron charge, ϵ_{si} is the permittivity of the silicon channel, and $n(r)$ is the free carrier charge density, which is expressed as $n(r) = n_i \exp(q(\varphi - V_n)/kT)$. In this density equation, n_i is the intrinsic carrier concentration, V_n is the electron quasi-Fermi potential, k is the Boltzmann constant, and $\varphi(r)$ is the electrostatic potential. Equation (1) satisfies the following boundary conditions: $d\varphi/dr(r=0) = 0$ and $\varphi(r=R) = \varphi_s$, where φ_s is the surface potential. According to the GCA, V_n is constant along the r -direction, i.e., $V_n = V_n(y)$. Equation (1) can be solved analytically as in Equation (2), which is the

same as the result of the GAA FET presented in previous works [15,26–29] without a ferroelectric layer.

$$\varphi(r) = V_n - \frac{2kT}{q} \ln \left(\frac{R}{2\beta} \sqrt{\frac{q^2 n_i}{2kT\epsilon_{Si}}} \left(1 - \frac{\beta^2 r^2}{R^2} \right) \right) \quad (2)$$

where R is the radius of the silicon channel, and β is the dimensionless intermediate parameter related to φ_s through the secondary boundary condition. The voltage balance condition of NC-GAA FET is written as $V_{gs} = V_{fb} - \frac{Q_{it}}{C_{ox}} + \varphi_s + V_{fe} + V_{ox}$, where V_{gs} is voltage across the gate-to-source, V_{fb} is the flat-band voltage, Q_{it} is the interface trap charge, V_{fe} is voltage across the ferroelectric layer, and V_{ox} is voltage across the dielectric layer between the ferroelectric layer and silicon channel. According to Landau–Devonshire theory, V_{fe} can be expressed in terms of mobile charge density, Q , as

$$V_{fe} = a_0 Q + b_0 Q^3 \quad (3)$$

where the coefficients a_0 and b_0 are related to the Landau parameters (a and b) of the ferroelectric material for a cylindrical gate, and they are expressed as [25]

$$a_0 = 2aR \cdot \ln \left(1 + t_{fe}/(R + t_{ox}) \right) \quad (4)$$

$$b_0 = 2bR^3 \cdot \left(1/(R + t_{ox})^2 - 1/(R + t_{fe} + t_{ox})^2 \right) \quad (5)$$

where t_{ox} is the thickness of intermediate insulator layer and t_{fe} is the ferroelectric thickness. In addition, V_{ox} can be expressed as $V_{ox} = Q/C_{ox}$ where $C_{ox} = \epsilon_{ox}/(R \ln(1 + t_{ox}/R))$.

Figure 1. (a) Three-dimensional scheme of the NC-GAA FET; (b) cross-section of the NC-GAA FET.

Firstly, according to Gauss' law, the mobile charge density, Q , can be determined, using Equation (2) as an intermediate parameter. Then the voltage balance equation can be formulated as Equation (7). This modeling methodology of the surface potential was used in [25], and this work also utilizes it and tries to write it down repeatedly to avoid confusion.

$$Q = \epsilon_{Si} \left. \frac{d\varphi(r)}{dr} \right|_{r=R} = \epsilon_{Si} \frac{2kT}{q} \frac{2\beta^2/R}{1 - \beta^2} \quad (6)$$

$$V_{gs} - V_{fb} + \frac{Q_{it}}{C_{ox}} - \varphi_s = \left(a_0 + \frac{1}{C_{ox}} \right) Q + b_0 Q^3 \quad (7)$$

Therefore, the formula for β related to the surface potential can be obtained as in Equation (8) by substituting Q of Equation (6) into Equation (7).

$$\ln\beta - \ln(1 - \beta^2) + m\left(\frac{\beta^2}{1 - \beta^2}\right) + n\left(\frac{\beta^2}{1 - \beta^2}\right)^3 = G \quad (8)$$

where $G = \left(\frac{q}{2kT}\right)(V_{gs} - V_{fb} + \frac{Q_{it}}{C_{ox}} - V_n) - \ln\left(\frac{2}{R} \sqrt{\frac{2kT\epsilon_{si}}{q^2 n_i}}\right)$, $m = \left(a_0 + \frac{1}{C_{ox}}\right)\frac{2\epsilon_{si}}{R}$, and $n = b_0\left(\frac{2\epsilon_{si}}{R}\right)^3\left(\frac{2kT}{q}\right)^2$. Since Equation (7) is not a closed form equation, it can be solved analytically through numerical calculation to obtain an accurate solution for β , or by using advanced mathematical techniques such as the Lambert-W function [30] and asymptotic equations [25]. In this work, β was obtained by introducing an asymptotic equation and a smoothing function. In this paper, we consider only acceptor-like trap states. Interface trap charge, Q_{it} , can be written as $Q_{it} = -q \cdot N_{et} \cdot f(E_t)$, where $f(E_t)$ is occupation probability of an acceptor-like trap with energy level, E_t is energy of single interface charge trap, and N_{et} is interface trap density per unit surface. By defining $E_{t-i} = E_t - E_i$ and using $\varphi_s = -(E_i - E_F)/q$, interface trap charge can be obtained as Equation (10), where E_i is the intrinsic fermi level energy and E_F is fermi level energy.

$$f(E_t) = \left(1 + \exp\left(\frac{E_t - E_F}{kT}\right)\right)^{-1} \quad (9)$$

$$Q_{it} = -q \cdot N_{et} \cdot \left[1 + \exp\left(\frac{E_{t-i}}{k_B T}\right) \exp\left(-q \frac{\varphi_s - V_n}{kT}\right)\right]^{-1} \quad (10)$$

Finally, we can solve surface potential φ_s by using a self-consistent method, as shown in Figure 2, which is a similar method to previous papers of [24] that calculate the surface potential considering the interface trap in a device structure without a ferroelectric layer.

Figure 2. Flowchart for surface potential and interface trap charge of NC-GAA FET using self-consistent calculation.

3. Analytical Drain Current Model for NC-GAA FET

We can obtain the current equation by using the drift-diffusion current equation: $I_{ds} = \mu_{eff}(2\pi R)QdV/dy$. For convenience, we define $\alpha = 1 - \beta^2$. Integrating this equation

from the source to the drain and changing from the function of V to the function of α , we can obtain a different expression of the drift-diffusion current equation:

$$I_{ds} = \mu_{eff} \frac{2\pi R}{L} \int_0^{V_{ds}} Q(V) dV = \mu_{eff} \frac{2\pi R}{L} \int_{\alpha_s}^{\alpha_d} Q(\beta) \frac{dV}{d\alpha} d\alpha \quad (11)$$

where L is the channel length, μ_{eff} is the effective mobility, and α_s and α_d are solved from Equation (8) corresponding to $V = 0$ and $V = V_{DS}$, respectively. Note that $dV/d\alpha$ can be expressed as a function of α by differentiating Equation (8). Substituting these factors in Equation (11), integration can be performed analytically to yield

$$I_{ds} = \frac{8\pi\mu_{eff}\epsilon_{Si}}{L} \frac{kT}{q} \left[\frac{-q \cdot N_{et}}{C_{ox}} \{f(\alpha_D) - f(\alpha_S)\} + \frac{kT}{q} \{g(\alpha_D) - g(\alpha_S)\} \right] \quad (12)$$

where new functions, $f(\alpha)$, $g(\alpha)$, are defined in Equation (10) as

$$f(\alpha) = \frac{-da + a - 1}{da^2 - a + 1} - \frac{2d \tan^{-1}\left(\frac{2da-1}{\sqrt{4d-1}}\right)}{\sqrt{4d-1}} \quad (13)$$

$$\text{where } d = \exp\left(\frac{E_{t-i}}{k_B T}\right) \left(\frac{R}{2} \sqrt{\frac{q^2 n_i}{2kT\epsilon_{Si}}}\right)^2 \quad (14)$$

$$g(\alpha) = -\frac{2}{a} - \ln(a) + m\left(-\frac{1}{a^2} + \frac{2}{a}\right) + n\left(\frac{6}{a} - \frac{9}{a^2} + \frac{6}{a^3} - \frac{3}{2a^4}\right) \quad (15)$$

Following the approach of D. Jimenez [28], we can derive the analytical drain current Equation with closed-form by carefully checking the fluctuation of $h(a)$ and a , which has different values at each operation region; $h(a)$ is LHS of Equation (8).

(1) Linear region above threshold

In this region, $h(a_S), h(a_D) \gg 1$, thus $a_{S,D} \sim 1$. Hence, the term $-m/a_{S,D}^2 - 3n/2 a_{S,D}^4$ in $g(a_{S,D})$ becomes dominant, respectively. As a result, the drain current Equation is derived as

$$I_{ds} = \frac{8\pi\mu_{eff}\epsilon_{Si}}{L} \frac{kT}{q} \left[\frac{-q \cdot N_{et}}{C_{ox}} \{f(\alpha_D) - f(\alpha_S)\} + \frac{kT}{q} \left\{ -\frac{m}{a_D^2} - \frac{3n}{2 a_D^4} + \frac{m}{a_S^2} + \frac{3n}{2 a_S^4} \right\} \right] \quad (16)$$

(2) Saturation region above threshold

In this region, $h(a_S) \gg 1, h(a_D) \ll -1$, thus, $a_S \sim 1, a_D \sim 0$. Hence, the term $-m/a_S^2 - 3n/2 a_S^4$ in $g(a_S)$ and the term $-\ln(a_D) - 2/a_D$ in $g(a_D)$ become dominant. As a result, the drain current Equation is derived as

$$I_{ds} = \frac{8\pi\mu_{eff}\epsilon_{Si}}{L} \frac{kT}{q} \left[\frac{-q \cdot N_{et}}{C_{ox}} \{f(\alpha_D) - f(\alpha_S)\} + \frac{kT}{q} \left\{ -\ln(a_D) - \frac{2}{a_D} + \frac{m}{a_S^2} + \frac{3n}{2 a_S^4} \right\} \right] \quad (17)$$

(3) Subthreshold region

In this region, $h(a_S), h(a_D) \ll -1$, thus $a_S, a_D \sim 0$. Hence, the term $-\ln(a_{S,D}) - 2/a_{S,D}$ in $g(a_{S,D})$ becomes dominant. As a result, the drain current Equation is derived as

$$I_{ds} = \frac{8\pi\mu_{eff}\epsilon_{Si}}{L} \frac{kT}{q} \left[\frac{-q \cdot N_{et}}{C_{ox}} \{f(\alpha_D) - f(\alpha_S)\} + \frac{kT}{q} \left\{ -\ln(a_D) - \frac{2}{a_D} + \ln(a_S) + \frac{2}{a_S} \right\} \right] \quad (18)$$

Finally, to obtain the unified current equations, we use the smoothing function as

$$I_{ds}(I_{ds1}, I_{ds2}, \epsilon) = \frac{2}{A} \left[I_{ds1} + I_{ds2} + \sqrt{(I_{ds1} + I_{ds2})^2 - A \cdot I_{ds1} \cdot I_{ds2}} \right] \quad (19)$$

where $A = 4 - \epsilon$ and $\epsilon \in (0,1)$. In this work, a long-channel ideal characteristic model was developed using a channel length of 1 μm . By adding various short-channel effects (e.g., drain-induced barrier lowering, threshold voltage roll-off, velocity saturation, and so on)

to the developed baseline model, it can be applied to devices with the channel length of several to tens of nanometers.

4. Results and Discussion

Table 1 shows the key dimensions and material parameters of NC GAA-FET used in the experiments. By using these parameter values, we can validate the regional-based current–voltage model and investigate electrical behaviors of NC GAA-FET in this section. In Table 1, N_{sd} is the doping density in source and drain regions in Table 1. As the source and drain regions are assumed to be heavily doped with N^+ over 10^{20} cm^{-3} , effects such as voltage drop due to parasitic resistance are neglected. Thus, 0 and V_{ds} are applied to $V_n(y)$ at the source end and drain end in Equations (1) and (2), respectively. This method is the same approach used for compact modeling intrinsic channel regions in previous papers [15,19,24–29,31].

Table 1. Parameter symbols and values.

Symbol (Units)	Value	Ferroelectric Parameter [31]
$L(\mu m)$	1	
$R(nm)$	8–12	$a = -3 \times 10^9 \text{ m/F}$ in Equation (4)
$t_{fe}(nm)$	3–8	$b = 6 \times 10^{11} \text{ m}^5/\text{C}^2\text{F}$ in Equation (5)
$t_{ox}(nm)$	1–5	which is corresponding coercive field
$V_{fb}(V)$	−0.3	$E_c = 1.15 \text{ MV/cm}$ and remnant
$\mu_{eff}(cm^2V^{-1}s^{-1})$	300	polarization $P_r = 5 \mu\text{C}/cm^2$
$N_{et}(cm^{-2})$	$0-1 \times 10^{12}$	
$N_{sd}(cm^{-3})$	$>10^{20}$	

The derived model is a surface potential (φ_s)-based model, and it can be calculated from Equation (8) followed by asymptotic equations. Figure 3a–d show φ_s as a function of t_{fe} , t_{ox} , R , and N_{et} . As shown in Figure 3a, the surface potential increases as t_{fe} increases, which is due to the improved capacitance matching between the ferroelectric layer and the intermediate insulator. Similarly, when the capacitance between the ferroelectric layer and the intermediate insulator deviates due to t_{ox} variation from the well-matched state, it can be seen that the voltage amplification characteristic decreases, as shown in Figure 3b. In addition, as shown in Figure 3c, although R also affects the surface potential, when 40% change based on $R = 10 \text{ nm}$, only a slight change in the surface potential is observed. Therefore, the effects of t_{ox} and t_{fe} are more important than R when designing the NC GAA-FET. Lastly, Figure 3d shows the effect of N_{et} . The surface potential increases as N_{et} increases, but if N_{et} is smaller than a certain value, we can observe that small changes occur. These surface potential characteristics directly affect the channel current characteristics shown in Figures 4–7. In Figures 4–7, symbols are the results of applying the complicated current–voltage model from the surface potential by the numerical analysis method proposed in the previous work [25], and the line shows the regional-based current–voltage model proposed in this work. As can be seen in Figures 4–7, it can be seen that the proposed model in the entire operating regions of the NC GAA-FET describes the complicated current–voltage model well. Figure 4a,b show the current–voltage characteristics in low drain bias (linear region) and high drain bias (saturation region) under various t_{fe} conditions, respectively.

Figure 3. Electrostatic surface potential versus gate-to-source voltage (a) varies with ferro-electric material thickness; (b) varies with oxide thickness; (c) varies with radius; and (d) varies with interface trap density per unit surface.

Figure 4. Comparison of drain current versus gate-to-source voltage between proposed model and numerical calculation when ferro-electric thickness varies with $t_{fe} = 0, 3, 5, \text{ and } 8 \text{ nm}$ ($R = 10 \text{ nm}$, $t_{ox} = 1 \text{ nm}$); (a) low drain bias; (b) high drain bias.

Figure 5. Result of drain current versus gate-to-source voltage when oxide thickness varies with $t_{ox} = 1, 3$, and 5 nm ; (a) low drain bias; (b) high drain bias.

Figure 6. Result of drain current versus gate-to-source voltage when radius varies with $R = 8, 10$, and 12 nm ; (a) low drain bias; (b) high drain bias.

Figure 7. Result of drain current versus gate-to-source voltage when interface trap density per unit surface varies with $N_{it} = 5 \times 10^{10}, 1 \times 10^{11}, 5 \times 10^{11}, 1 \times 10^{12}$; (a) low drain bias; (b) high drain bias.

As with the surface potential characteristic, it can be seen that the sub-threshold swing is improved due to the voltage amplification characteristic when it is increased up to $t_{fe} = 8\text{ nm}$. Therefore, lower off current and improved operating speed can be expected at the same power supply voltage (V_{DD}). This can be clearly confirmed by comparing current–voltage behaviors of $t_{fe} = 0\text{ nm}$ (GAA FET characteristics without ferroelectric

layer) and $t_{fe} = 8$ nm. Figure 5 shows the current–voltage characteristic when t_{fe} is fixed and t_{ox} is increased from 1 nm (a reference state well matched with a ferroelectric layer). As t_{ox} becomes thicker, as shown in Figure 3b, the voltage amplification effect due to the NC characteristic and the current characteristic decrease due to the increase in effective oxide thickness are observed. Figure 6 shows the current–voltage characteristics when t_{fe} and t_{ox} are fixed with the voltage amplification optimized and R increased. As R increases (decreases), there is no significant change in surface potential, as shown in Figure 3c, but the current increases (decreases) due to the effect of increasing (decreasing) the total channel width ($2\pi R$). Figure 7 shows the current–voltage characteristics when t_{fe} , t_{ox} , and R are fixed and N_{et} is increased. As N_{et} increases (decreases) the current increases (decreases) at low gate-to-source voltage and decreases (increases) at high gate-to-source voltage.

Figure 8 is the result of comparing the model proposed in this paper with the model proposed in the previous paper of [25]. The previous result is a I–V model formula applicable to all operating regions based on surface potential calculation, and the proposed model has a complex form without considering the interface trap. On the other hand, in this work, the surface potential is calculated by considering the interface trap, and a simplified current equation is proposed according to the operating region, and an integrated model is developed by using a smoothing function. Therefore, I–V characteristics due to variations in t_{fe} , t_{ox} , and R without interface traps can be compared with the previous results of [25]. However, the I–V characteristics according to the variation of the interface trap cannot be compared with the previous results of [25]. As shown in Figure 8, it was confirmed that the comparison result had an error of about 4–6% from that of the previous results of [25] according to the variation of various device geometries, and the computational efficiency was improved by about 13–24%. Figures 9 and 10 are the results of analyzing transconductance (g_m) and transconductance generation factor (TGF) using the developed model by changing various geometry (t_{ox} , t_{fe} , and R) and trap density (N_{et}) characteristics of NC GAA-FET. It was confirmed that the developed model can predict the first-order differential characteristics through the g_m simulation results shown in Figure 9. TGF emphasizes how effectively the drain current is used to achieve better transconductance, and the variation of TGF with V_{GS} is shown in Figure 10. When V_{GS} increases, the TGF characteristics decrease near the threshold voltage, then increase rapidly, and then decrease monotonically in the strong inversion region.

Figure 8. Cont.

(c)

	Simulation Time	AVG. RMS error (%)
(a)	13.36% ↓	4.755
(b)	23.78% ↓	6.035
(c)	22.79% ↓	4.165

(d)

Figure 8. Comparison of I_{DS} – V_{GS} prediction results between the previous work [25] and this work for various geometry cases; (a) $t_{fe} = 8$ nm, $t_{ox} = 3$ nm, $R = 10$ nm, (b) $t_{fe} = 8$ nm, $t_{ox} = 1$ nm, $R = 10$ nm, (c) $t_{fe} = 5$ nm, $t_{ox} = 1$ nm, $R = 10$ nm, and (d) summary of simulation time and average root-mean-square (RMS) error.

(a)

(b)

(c)

(d)

Figure 9. Characteristics of transconductance (g_m) for various geometries; (a) t_{ox} , (b) R , (c) t_{fe} , and trap density (d) N_{et} .

Figure 10. Characteristics of transconductance generation factor (TGF) for various geometries; (a) t_{ox} , (b) R , (c) t_{fe} , and trap density (d) N_{et} .

5. Conclusions

In this work, we proposed a method to obtain the surface potential and an analytical current–voltage model of NC GAA-FET. The proposed model considers GAA cylindrical coordinates, negative capacitive effect, and interface trap at the same time. It is a channel potential-based model that calculates the surface potential between the silicon channel and the intermediate insulator. Using the obtained channel potentials and the operation regional approach, a useful and simple drain current–voltage model equation is derived by taking the appropriate approximation in each transistor’s operating region (linear, saturation, and sub-threshold regions). The proposed model shows high consistency when compared with the previous comprehensive model. In addition, the electrical properties of NC GAA-FET were investigated by varying key device parameters such as ferroelectric thickness, intermediate insulator thickness, silicon channel radius, and interface trap density per unit surface.

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