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Design Strategies and Architectures for Ultra-Low-Voltage Delta-Sigma ADCs

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Abstract: The design of ultra-low voltage analog CMOS integrated circuits requires ad hoc solutions to counteract the severe limitations introduced by the reduced voltage headroom. A popular approach is represented by inverter-based topologies, which however may suffer from reduced finite DC gain, thus limiting the accuracy and the resolutions of pivotal circuits like analog-to-digital converters. In this work, we discuss the effects of finite DC gain on ultra-low voltage ΔΣ modulators, focusing on the converter gain error. We propose an ultra-low voltage, ultra-low power, inverter-based ΔΣ modulator with reduced finite-DC-gain sensitivity. The modulator employs a two-stage, high DC-gain, switched-capacitor integrator that applies a correlated double sampling technique for offset cancellation and flicker noise reduction; it also makes use of an amplifier that implements a novel common-mode stabilization loop. The modulator was designed with the UMC 0.18 µm CMOS process to operate with a supply voltage of 0.3 V. It was validated by means of electrical simulations using the Cadence™ design environment. The achieved SNDR was 73 dB, with a bandwidth of 640 Hz, and a clock frequency of 164 kHz, consuming only 200.5 nW. It achieves a Schreier Figure of Merit of 168.1 dB. The proposed modulator is also able to work with lower supply voltages down to 0.15 V with the same resolution and a lower power consumption despite of a lower bandwidth. These characteristics make this design very appealing in sensor interfaces powered by energy harvesting sources.

Keywords: ADC; delta-sigma modulator; energy-harvesting; inverter-like; ultra-low power; ultra-low voltage

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1. Introduction

Recent developments in the field of Internet of Things (IoT) applications have encouraged the research for systems that are capable of working with very low supply voltages consuming very little power [1–3]. The energy harvesting scenario is undoubtedly among the most interesting ones: It involves devices that are capable of gathering energy from the surrounding environment. The energy sources could be thermal jumps, radiations, vibrations, and biochemical reactions, just to mention a few. Among the most captivating harvesters we may find are biofuel cells, which can behave at the same time as an energy source, with power densities up to 1 mW/cm^2, and a self-powered physiochemical sensor [4,5]. However, biofuel cells typically provide supply voltages in the range of 0.3–0.5 V. A DC-DC converter may be useful to enhance the supply voltage for the electronic interface, thus mitigating the design effort. Nevertheless, it does not represent the optimal choice in every scenario: The main reasons are the area occupied by the inductors in inductive boost converters or, alternatively, the limited efficiency of switched capacitor converters [6], besides the generation of a potential non-compatible with the human body [7]. Therefore,

designing circuits that can directly work with very low supply voltages is of primary importance. However, integrated circuit design becomes extremely challenging, in particular for CMOS analog circuitry: In these conditions, many or all transistors must operate in a sub-threshold region and the available drain-source voltage is just sufficient to place them at the boundary of triode region. Furthermore, the limited voltage headroom rules out the most popular topologies. Dedicated design techniques have been proposed, such as overdrive boosting [8], clock boosting [9], body biasing, and/or bulk-driven circuits [10–12]. A common approach in Ultra-Low Voltage (ULV) design consists in employing inverter-based circuits [13,14] is that if properly biased, the standard CMOS inverter acts as a voltage amplifier. Furthermore, it represents a good compromise among power consumption, speed, and noise performances. However, it has also some disadvantages, such as a low DC gain, lack of a non-inverting input terminal, and high sensitivity to Process, Voltage, and Temperature (PVT) variations.

In recent years, the interest in low voltage Analog-to-Digital Converters (ADCs) has considerably grown [15–17]: For example, we may find fully synthesizable (i.e., completely implementable with standard cells) Successive Approximation Register (SAR) ADCs designed for a supply voltage as low as 0.5 V [18]. SAR converters represent a popular solution when the required resolution is not too stringent, achieving supply voltages even down to 0.2 V [19] with very competitive power consumption. However, when the required resolution starts to increase and moderate signal bandwidths are required, as in readout interfaces for wearable sensors, Delta-Sigma ($\Delta\Sigma$) modulators may represent a more competitive choice. The single bit topologies, for instance, manage to achieve a great linearity without strict requirements of passive device matching (i.e., of area consumption). Many different architectures have been presented in literature for low and ultra-low supply voltages [20–25]; in this context, inverter-based modulators represent one of the preferred choices [8,9,26]. Despite this, finite DC gain effects, typical of inverter-based $\Delta\Sigma$ modulators, have not been fully explored yet.

In this work, we discuss some relevant modulator issues such as gain error, arising of dead-zones, degradation of the noise shaping function, low-frequency noise, and offset which may heavily affect the accuracy and the resolution of the converters, especially in ultra-low voltage scenarios. In order to overcome the above-mentioned issues, we propose an ULV, Ultra-Low Power (ULP), 2nd order, single-bit, Fully-Differential (FD), inverter-based $\Delta\Sigma$ modulator. It employs an FD inverter-like amplifier with a novel Common-Mode (CM) Stabilization Loop (CMSL), which was recently proposed in [27] and here, we see its first application. Another key innovation of the proposed modulator is the use of a recently-introduced [28] Switched Capacitor (SC) integrator capable of producing relatively high DC gains even when it is synthesized with very low-gain inverter-like amplifiers. This integrator, that was already employed in single-ended $\Delta\Sigma$ modulators [9,29], offers also the advantage of offset and flicker noise reduction obtained by means of Correlated Double Sampling (CDS).

The rest of this paper is organized as follows. Section 2 describes the finite gain error and other issues related to the design of ULV $\Delta\Sigma$ modulator. Section 3 presents the complete architecture of the $\Delta\Sigma$ modulator, while Section 4 describes the results estimated by means of electrical simulations. Finally, conclusions are drawn in Section 5.

2. Non-Idealities in ULV $\Delta\Sigma$ Modulators

Ultra-low voltage operation imposes severe limitations on the design of analog circuits. With the typical values of MOSFET threshold voltages Vth, working with supply voltages as low as a few hundred millivolts makes weak inversion and subthreshold region unavoidable. In these operating regions, MOSFETs show very low transition frequencies, despite the optimum current efficiency (g_m/I_D) [30]. As a consequence, design of ULV amplifiers with target specifications of both bandwidth and DC gain may be very complex. In this scenario, the use of single-stage amplifiers in SC circuits (as the SC integrators in $\Delta\Sigma$ modulators) results in low accuracy, due to the low-voltage headroom that is not

compatible with cascoded stages and gain boosting techniques, thus preventing to reach sufficiently high DC gain. On the other hand, multi-stage amplifiers represent a very popular choice due to the relaxation of DC gain requirements on each single stage [31]. Nevertheless, they require compensation networks [32] and higher power consumption, which in typical SC circuits are not justified by the need to drive large resistive loads.

In SC ΔΣ modulators, the DC gain may limit the converter accuracy and resolution through gain error, dead-zones, and degradation of the noise shaping function of the modulator. With conventional supply voltages, the DC gain of the integrators (tied to the amplifier DC gain) is generally high enough to make these adverse effects secondary. Conversely, in ultra-low voltage operating conditions, integrator gains may drop to just a few tens, making finite gain effects a real concern. For this reason, it is mandatory to estimate the required DC gain by means of preliminary behavioral simulations. Many works in the literature deal with high-level modeling of ΔΣ modulators, trying to describe as accurately as possible the non-idealities that most affect the bottom-level design [33–36]. In this section, we will describe some results closely related with the ULV design space, in particular concentrating on the effects of amplifier DC gain on the modulator performances.

A linearized model of a 2nd order Cascade of Integrator FeedBack (CIFB) modulator with no feedforward paths is depicted in Figure 1, where a_1, a_2, b_1, and c_1 represent the coefficients of the specific modulator topology. V_{o1} and V_{o2} represent the state variables of the ΔΣ modulator, i.e., the output of the Discrete-Time (DT) integrators. V_{n1} and V_{n2} represent the referred-to-input noise and offset voltages of the two integrators, while V_{nq} represents the quantization noise introduced by the single-bit ADC present in the modulator loop, here replaced by a constant gain k. DT integrators are modeled with their z-domain transfer functions, following the approach presented in [37], including the gain error (λ) and the phase error (p) of the integrator due to amplifier finite DC gain, respectively, evaluated for a common architecture of parasitic-insensitive SC integrator [38]:

$$\begin{cases} \lambda_1 = \frac{1}{1+\frac{1}{A_1}(1+a_1)} \\ p_1 = \frac{1+\frac{1}{A_1}}{1+\frac{1}{A_1}(1+a_1)} \\ \lambda_2 = \frac{1}{1+\frac{1}{A_2}(1+a_2+c_1)} \\ p_2 = \frac{1+\frac{1}{A_2}}{1+\frac{1}{A_2}(1+a_2+c_1)} \end{cases}, \quad (1)$$

where A_1 and A_2 represent the finite DC gain of the amplifier employed in the first and the second SC integrator, respectively.

An ad hoc discrete-time simulator of a 2nd order ΔΣ modulator was realized with the *NumPy* module for numerical computing of the Python language and used to evaluate the gain error, the dead-zone amplitude, and the increment of quantization noise due to the finite DC gain of the two integrators. DC performances have been evaluated by averaging the output bitstream over a large number of clock cycles such that the obtained resolution is finer than the DC errors that we want to estimate.

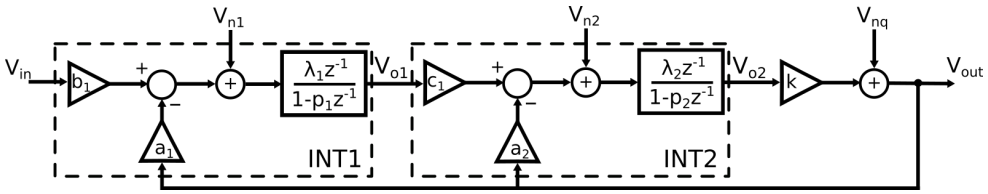

Figure 1. Linearised, z-domain model of a 2nd order ΔΣ modulator that includes finite DC gains and noise.

2.1. Gain Error

Among the well-known issues related to finite DC gain, gain error in ΔΣ ADCs has never been investigated, to the best of our knowledge. ΔΣ ADCs owe most of their popularity to audio and telecommunication applications, where gain errors do not represent a main concern. This may be the reason why a work that analyzes the gain error of a ΔΣ ADC has not been presented in the literature yet. However, different considerations must be argued for low-frequencies data acquisition systems. Whereas gain accuracy of instrumentation amplifiers represents a fundamental requirements, gain error of ΔΣ ADCs employed in sensor interfaces is often ignored, notwithstanding its contribute to the accuracy of the whole readout chain. For this reason, considering the relevance of this inaccuracy source in ultra-low voltage circuits, some insights on the gain error of ΔΣ converters are given in this Section.

Let us start considering the linearized block diagram depicted in Figure 1, from which the modulator Signal Transfer Function in the z domain $STF(z)$ can be straightforwardly evaluated. We are interested in phenomena occurring in DC operations, therefore we need to consider the effects of the finite DC gain of the two integrators on the STF for $z = 1$. In particular, the gain error ε_G is the difference between the $STF(z = 1)$ for infinite gains A_1 and A_2 and the actual $STF(z = 1)$. Considering that the former is unitary, we obtain the following relationship:

$$\begin{aligned} \varepsilon_G &= 1 - STF(z = 1) \\ &= \frac{ka_2A_2 + c_1 + a_2}{kc_1A_1A_2 + ka_2A_2 + c_1 + a_2} \\ &\simeq \frac{a_2}{c_1A_1}. \end{aligned} \tag{2}$$

In the final approximation given in Equation (2), we made the assumption that $A_1, A_2 \gg 1$, which is reasonable even for inverter-based circuits. It is important to highlight that, by this approximation, ε_G is a function of only A_1 and of coefficients a_2 and c_1. Figure 2 shows the gain error curves for different values of A_1, A_2, confirming the very slight dependence of ε_G on A_2. Moreover, two families of curves can be distinguished for the two different sets of coefficients indicated in the figure.

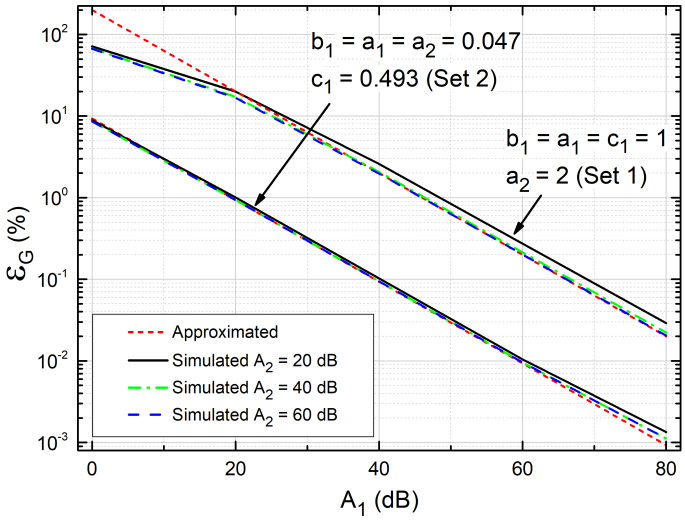

Figure 2. Gain error versus 1st integrator DC gain, approximated and simulated for different DC gains of the 2nd integrator and two different sets of coefficients.

The choice of these values is here briefly discussed. A first set ($a_1 = b_1 = c_1 = 1$, $a_2 = 2$) can be easily calculated from the linearized z-domain model of Figure 1 starting from the approximation of infinite DC gain (i.e., $\lambda_1 = \lambda_2 = p_1 = p_2 = 1$), in order to obtain

a flat STF and a Noise Transfer Function (NTF) with two zeros at the origin. However, with this set of coefficients (from now on indicated as "Set 1"), the modulator state variables V_{o1} and V_{o2} are not bounded to remain within the full-scale range $[-FS/2; FS/2]$ of the ADC, as shown in Figure 3. Since the full-scale range is typically equal or on the order of the supply voltage, this would imply large harmonic distortions due to the limited linear output ranges of the amplifiers employed in the integrators.

To overcome this issue, the modulator coefficients can be properly scaled in order to limit the state variables [39]. An example of scaled coefficients, here called "Set 2", is represented by $a_1 = b_1 = a_2 = 0.047$, $c_1 = 0.493$. It is worth mentioning that, working with low supply voltages and consequently low voltage headrooms, the attenuation introduced by the modulator coefficients becomes increasingly essential. The linear output range of an amplifier can be roughly considered to end at voltages where one of the output devices exits saturation region. Considering, for instance, a simple voltage amplifier as the CMOS inverter, the linear output range is limited by a saturation voltage V_{DSat} from both rails. V_{DSat}, which in strong inversion corresponds to the overdrive voltage $(V_{GS} - V_{th})$, can be assumed around $4U_t$ in weak inversion[40], where $U_t = kT/q$ is the equivalent thermal voltage, k is the Boltzmann constant, T is the absolute temperature, and q is the electron charge. $U_t \simeq 25$ mV at room temperature, then $V_{DSat} \simeq 100$ mV in weak inversion. Outside the linear output range, the output resistance rapidly decreases and consequently also the DC gain, increasing also the distortion introduced by the amplifier. For supply voltages approaching $2V_{DSat}$, the linear output range becomes increasingly narrow, thus forcing a more aggressive scaling of the modulator coefficients. The Set 2 introduced before, for example, has been obtained in order to have a state variable swing equal to 15% of the full-scale range, as confirmed by the histograms in Figure 3.

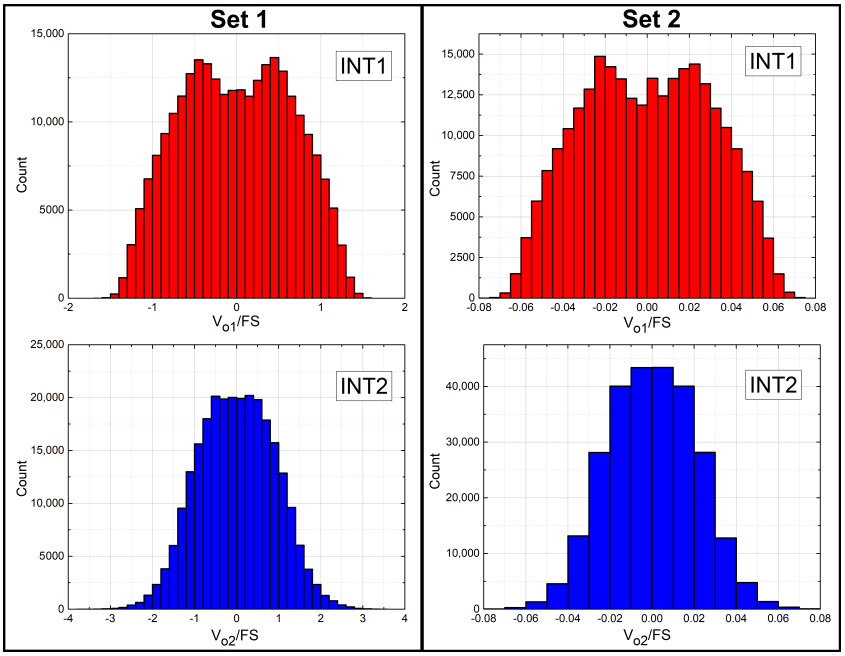

Figure 3. Histograms of the integrator outputs V_{o1} (**top**) and V_{o2} (**bottom**), normalized to the full-scale range of the ADC, for the two different sets of coefficients.

Actually, the coefficient sizing impacts not only on the converter linearity, but even on other parameters, for example on the gain error as shown in Figure 2. A lower ratio a_2/c_1 as in the case of the scaled coefficients used here, involves a lower gain error, as described also by Equation (2). Nevertheless, in order to achieve a negligible gain error for an ADC with moderate resolution, thus avoiding expensive calibration procedures, a DC gain of the first integrator higher than 40–50 dB is still needed in even employing the second set of coefficients.

2.2. Dead-Zones

As is known, the integrator DC gain also affects the width of Dead-Zones (DZs). Differently from the gain error, DZs depend significantly on the DC gain of both integrators in a 2nd order ΔΣ modulator [39]. It is worth noting that, even in this case, the modulator coefficients have an influence on the DZs. Figure 4a shows the DC characteristics of the modulator with the first set of coefficients, for $A_1 = 20$ dB and different values of A_2. For the curve with the lowest value of A_2, dead-zones are visible for several DC inputs. In the inset, the scaling of the dead-zone amplitude for increasing value of A_2 is visible. Figure 4b shows the amplitude of the dead-zone located around the middle of the converter input range, which is the widest of all the other dead-zones present in the ADC characteristics. Two families of curves are plotted for the two sets of coefficients previously discussed. With Set 2, for the same values of A_1 and A_2, the DZ is much smaller than in the case of Set 1. In both cases, however, the DZ is approximately inversely proportional to the product of A_1 and A_2. For this reason, if large DC gains A_1 are employed for gain error issues, relative low A_2 gains are allowed without running into significant distortion due to DZs, especially employing the scaled coefficients.

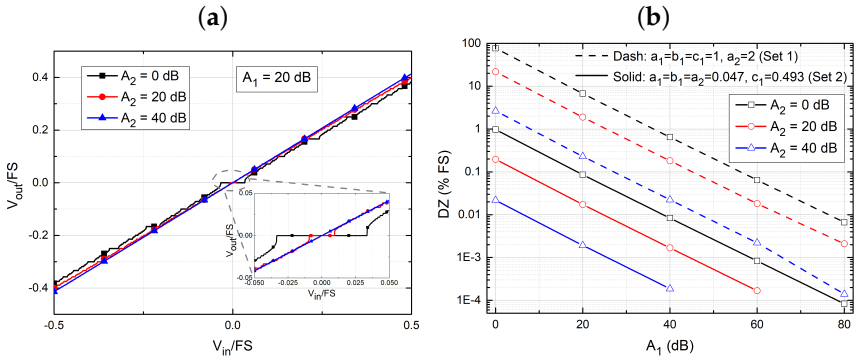

Figure 4. (**a**) DC characteristics for the first set of coefficients, for $A_1 = 20$ dB and different values of A_2, showing the presence of dead-zones. (**b**) Dead-zone amplitude as a percentage of the full-scale vs. amplifier gains for two different sets of coefficients.

2.3. Quantization Noise

A phase error in the integrators due to their limited DC gain causes the shifting of the two zeros in the NTF, thus increasing the overall quantization noise power. Figure 5 shows the SNDR of a 2nd order modulator, with a -2 dB_{FS} input tone and an OverSampling Ratio (OSR) of 128 for the two different sets of coefficients already discussed.

Considering the curves obtained employing Set 1, the maximum values of SNDR are reached for values of DC gains A_1 and A_2 higher than 60 dB. Conversely, the scaled coefficients of Set 2 allows for achieving the same values, but with a lower DC gain of both integrators. It is worth mentioning that for the lowest values of A_1 and A_2, especially with Set 1, dead-zones contribute to worsen the SNDR.

Even if the scaled coefficients guarantee better performances in terms of DC gain, dead-zones, and quantization noise suppression, mitigating the effect of finite DC gain of the amplifiers, it is not advisable to rely only on the values of the coefficients. Since the modulator coefficients are typically implemented as capacitive ratios in the SC integrators, too small values may be particularly detrimental for the modulator performances. When the converter resolution is limited by thermal noise, the absolute value of the input capacitors, responsible for the signal sampling, is sized according to kT/C noise specification. This is particularly critical in ULV scenarios, where the signal range is limited by the decreasing supply voltage and then, targetting the same resolution, the requirements on the converter noise becomes stricter. Consequently, small modulator coefficients enlarge the values of the feedback capacitors of the SC integrators, thus impacting on area and power consumption.

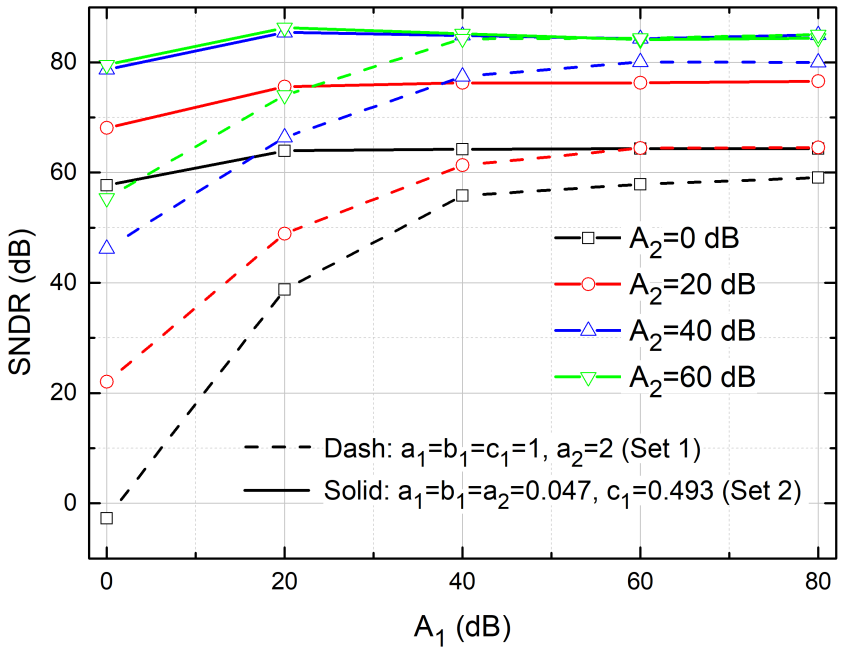

Figure 5. SNDR versus 1st integrator dc gain, simulated for different DC gains of the 2nd integrator and two different sets of coefficients.

2.4. Low-Frequency Noise and Offset

Error sources V_{n1} and V_{n2} of Figure 1 affect the converter performances through two different $NTFs$, which can be evaluated analogously to the traditional NTF for the quantization noise V_{nq}, considering the linearized block diagram of Figure 1 [41]. While offset and noise of the first integrator are not attenuated by the modulator response, the contributions of the second integrator are intrinsically high-pass filtered, thus giving negligible contributions in the signal bandwidth. For this reason, dynamic offset cancellation techniques, such as CHopper Stabilization (CHS) and correlated double sampling, are typically applied only to the first integrator. CHS represents a popular approach in ΔΣ modulators [12], thanks to the possibility of exploiting the digital low-pass decimator filter cascaded to the modulator, which also rejects to the offset ripple by proper choice of the chopping frequency and OSR. However, CHS modulation introduces several drawbacks, among which the worse settling time due to the parasitic capacitances of the demodulator switches. A typical solution is to place the chopper demodulator at non-dominant poles, as at the sources of the common-gate stage in the cascode structure [42]. In single-stage ULV and ULP amplifiers, where demodulation can be realized only at the output nodes, characterized by very high output resistance, CHS may have detrimental effects on the resulting DC gain of the amplifier. The SC integrator presented in [28] combines a CDS mechanism with a novel topology aimed at reducing the transfer function sensitivity to the amplifier DC gain, thus alleviating the above-mentioned issues related to ΔΣ modulators.

3. ΔΣ Modulator Architecture

A block diagram of the modulator is depicted in Figure 6. It is a 2nd order, single-bit, inverter-based, fully-differential topology: There are two integrators (INT1 and INT2), a 1-bit ADC and a 1-bit Digital-to-Analog Converter (DAC). A second order architecture was chosen because it represents a good compromise among resolution increase and simplicity; in addition, it is intrinsically stable.

The modulator was designed for an ultra-low supply voltage $V_{DD} = 0.3$ V. We will now analyze every single block in more detail.

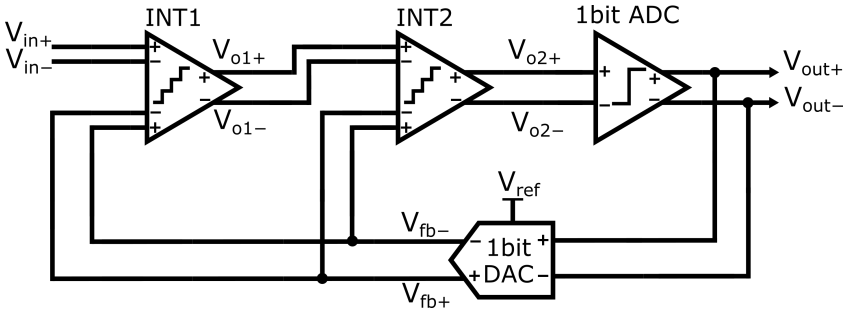

Figure 6. Block diagram of the fully-differential ΔΣ modulator.

3.1. Integrators

For the first integrator INT1, we adopted the topology of Figure 7 [28]. This architecture was already used in single-ended ULV ΔΣ modulators [9,29], but not yet in a FD implementation.

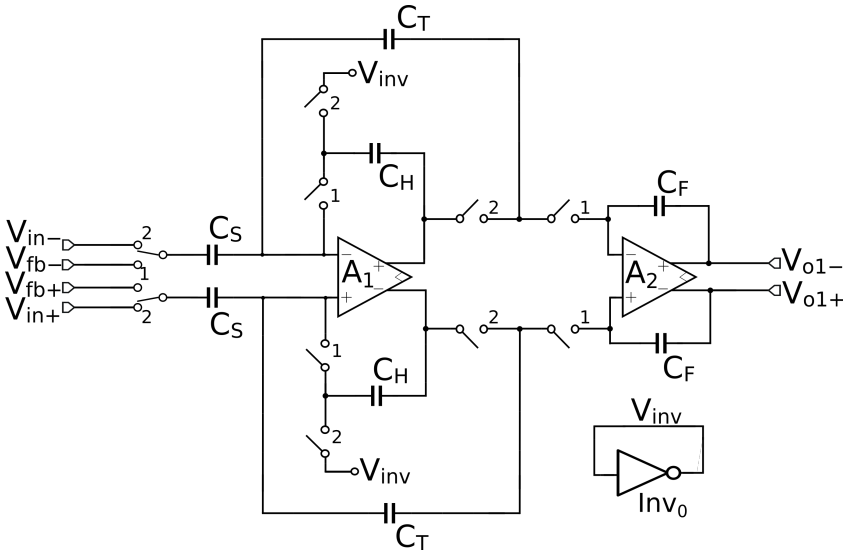

Figure 7. Fully-differential, inverter-based, high DC gain architecture adopted as the first integrator.

Every switch is closed during the phase corresponding to the number near to it, while A_1 and A_2 are inverter-based FD amplifiers that will be described later.

Due to the symmetry of the circuit, it is possible to restrict the analysis to the lower half. The input capacitor C_S samples V_{in+} and V_{fb+}, at the end of clock phases 2 and 1, respectively. A charge proportional to $(V_{fb+} - V_{in+})$ flows into C_T during phase 2. In the following, phase 1, the charge stored in C_T is transferred to C_F in the second stage, which behaves as an accumulator. This produces an increment of the output voltage V_{o1+}, so that an integration step is completed. Thanks to the C_H contribution, which holds the voltage at the output of the first amplifier during phase 1 avoiding its reset, the charge transfer is a little sensitive to the DC gain of the first amplifier, as proposed in [43]. Considering also the second stage, the integrator produces an overall DC gain proportional to the cube of the gain of the single amplifier [28]. This aspect makes this SC topology particularly interesting for ULV ΔΣ modulators, thus relaxing the requirements on the DC gain of the employed amplifiers. Even single-stage inverter-like topologies with short channel lengths, with DC gain on the order of tens or lower, can be usefully exploited. Another advantage of the proposed integrator is the mentioned CDS technique, capable of rejecting the offset and reducing the flicker noise of both the amplifiers, improving low frequency accuracy and resolution.

As widely explained in the previous section, converter gain error depends almost exclusively on the first integrator. Moreover, since the dead-zone amplitudes and the zeros'

shift in the NTF depend on the product of both A_1 and A_2, the high-gain SC integrator has been employed only for the first integrator. Even noise and offset requirements for the second integrator are more relaxed, thus no dynamic offset cancellation techniques are needed. For all these reasons, it was possible to adopt a simpler topology for the second integrator, such as the parasitic-insensitive one [38] as depicted in Figure 8 in its FD version. Due to the different coefficients a_2 and c_1 implemented in the SC integrator, the number of input sampling capacitors is doubled.

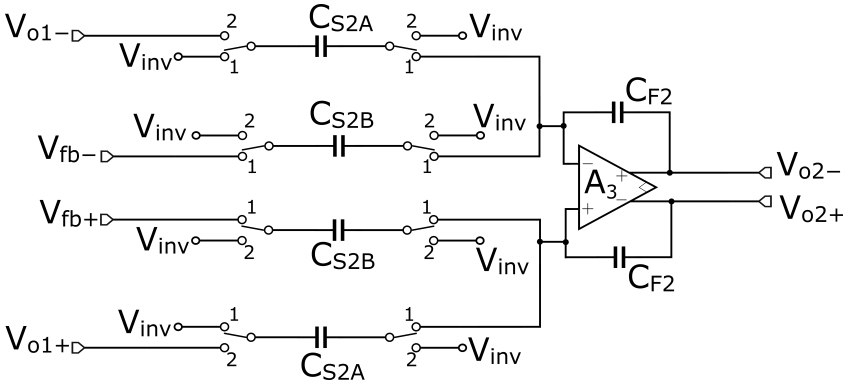

Figure 8. Fully-differential, inverter-based topology adopted as the second integrator.

Finally, a simple diode-connected inverter (Inv_0) generates the constant bias voltage V_{inv} depicted in Figure 7. This voltage is connected to C_H during phase 2, in order to minimize the voltage excursion of C_H bottom terminal in the transition between the two clock phases; it is also employed in the second integrator INT2 as a reference common-mode voltage.

3.2. ADC and DAC

The ADC and the DAC are 1-bit architectures, visible in Figure 9a,b, respectively. The 1-bit ADC internal to the modulator is simply a comparator. The input signal is pre-amplified by the input inverters, then the two inverters in a latch fashion exploit the positive feedback to take the decisions and regenerate the full-logical values for the output bitstream. The 1-bit DAC is simply the cascade of two inverters, where the first one acts as an inverting buffer and the second one provides the differential feedback voltages V_{fb+} and V_{fb-}. V_{ref+} and V_{ref-} represent the differential reference voltages of the modulator. In this work, we opted for a ratiometric converter; in this way, V_{ref+} and V_{ref-} correspond to the supply voltage and ground, respectively.

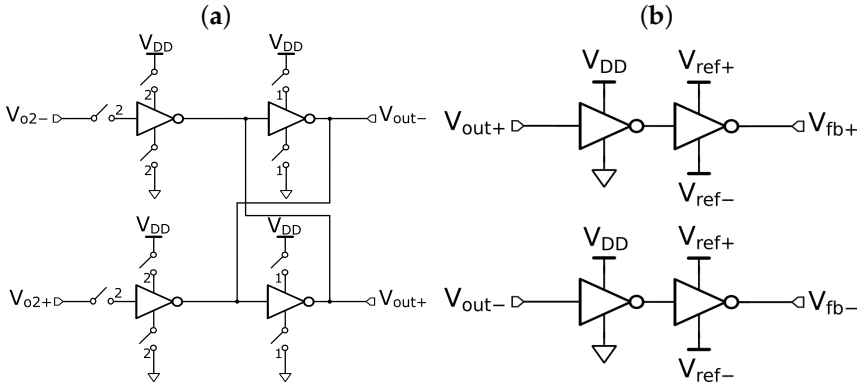

Figure 9. 1-bit ADC (**a**) and DAC (**b**) schematics.

3.3. Clock-Boosting Circuit

The switches of the circuit were mostly implemented as complementary pass-gates. The ULV domain is detrimental for the on-resistance of the MOSFETs in the triode region.

Increasing the aspect ratio to reduce the pass-gate on-resistances impacts the linearity performances of the circuit due to larger parasitic capacitances and charge injection issues. This design takes advantage from a clock-boosting technique capable of level-shifting both the high and the low levels of the clock signals driving the pass-gates. The circuit is visible in Figure 10 and a more detailed analysis is provided in [9].

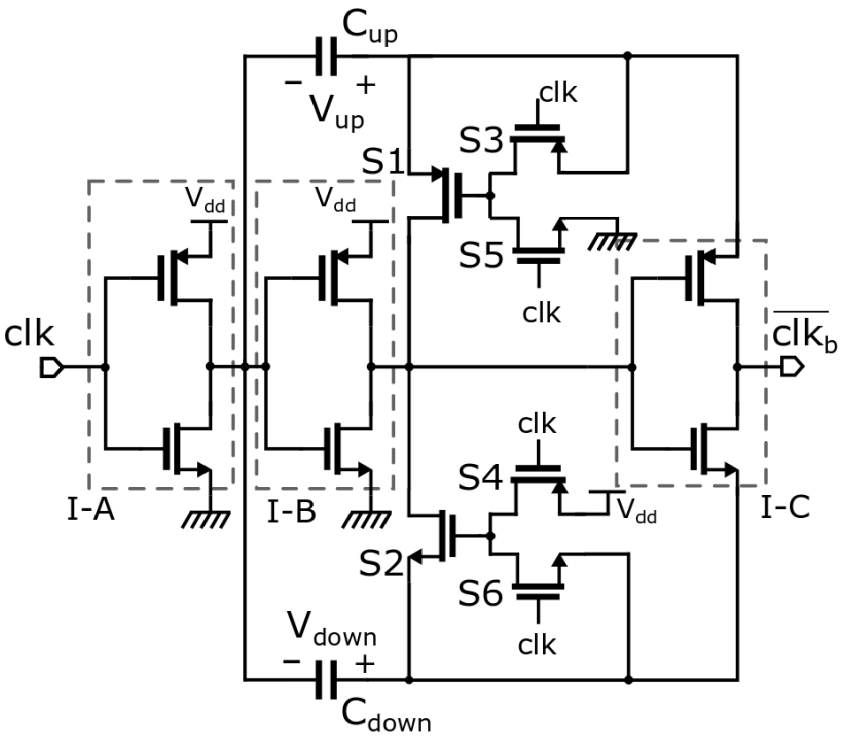

Figure 10. Transistor-level view of the clock-boosting circuit.

3.4. Inverter-Based Amplifier

As already stated, the CMOS inverter may be used as a replacement of a voltage amplifier, as demonstrated in [9]. A FD version of the inverter-like amplifier requires that its output CM is stabilized, in order to prevent possible drifts and, consequently, a degradation of the output Differential-Mode (DM) range. A well-known solution is represented by the Nauta transconductor [44], but many others are available in the literature [45]. In this work, we adopted the amplifier recently proposed in [27], which has an increased output linear range with respect to other solutions. Its schematic view is shown in Figure 11. It was employed in both INT1 and INT2 for A_1, A_2, and A_3.

Inv_1 and Inv_2 are the inverters that process the input differential signal and are nominally identical. The other inverters $Inv_{3\text{-}9}$ are part of the stabilization loop. Again, for symmetry purposes, Inv_3 needs to match Inv_4, and the same applies for Inv_5 and Inv_6.

The CMSL was thoroughly analyzed in [27]; here, we will briefly summarize its principle of operation. Assuming ideal matching between the inverters, the loop does not affect the output DM, apart from an attenuation of the output resistance due to the presence of $r_{o,5}$ and $r_{o,6}$. Inv_3 and Inv_4 produce a voltage V_x that, as far as small signals are concerned, depends only on the output CM. Then, Inv_7 and $Inv_{5/6}$ close the loop. Even in the case of large output differential modes that are going to affect node V_x, the feedback loop has a very small impact on the differential mode gain, since $Inv_{5/6}$ produce only common-mode effects. Inv_8 and Inv_9, instead, act as load for $Inv_{3/4}$ and Inv_7, respectively, in order to reduce the loop gain and avoid instability. This is needed because there are two loops formed by the cascade of three inverters, that are $Inv_{3\text{-}7\text{-}5}$ and $Inv_{4\text{-}7\text{-}6}$.

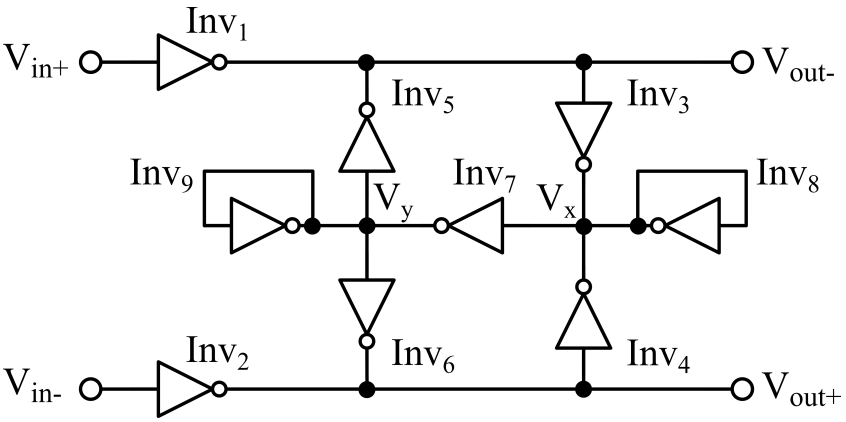

Figure 11. Schematic view of the inverter-based, fully-differential amplifier with the common-mode stabilization loop.

Figure 12 shows the simulated Bode diagrams and the dc characteristics, with a supply voltage of 0.3 V and 0.15 V. The amplifier DC gain, already lower than 20 dB at $V_{DD} = 0.3$ V, is around only 12 dB at $V_{DD} = 0.15$ V. The Gain-BandWidth product (GBW) is also reduced by nearly a factor of 10, due to the exponential dependence of the quiescent current on V_{DD}. The input-output differential characteristics at the two different supply voltages depicted in Figure 12 show that, besides the different gain around $V_{id} = 0$ V, the linearity range of the amplifier is also obviously smaller at the lowest supply voltage.

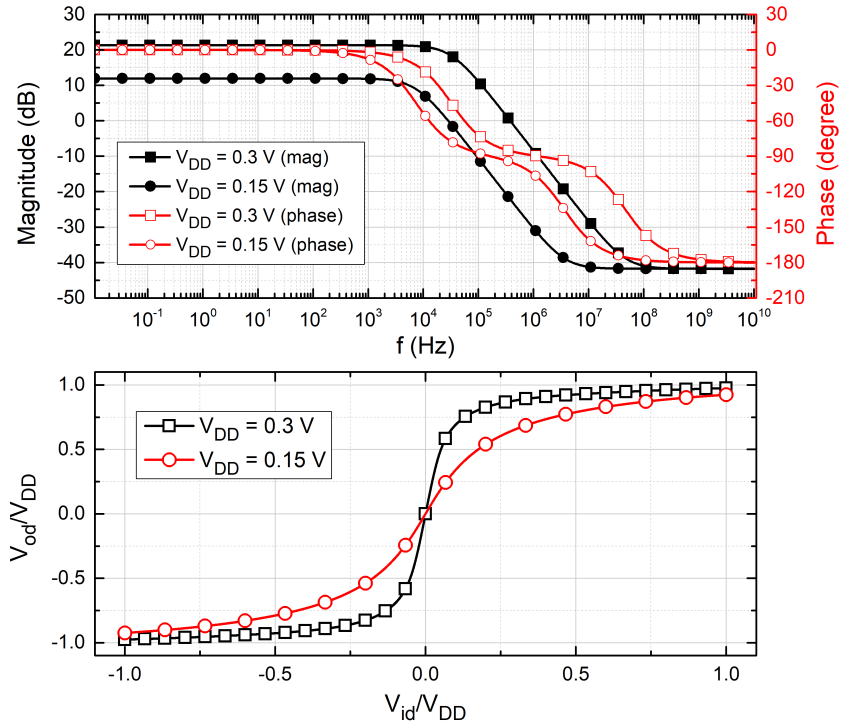

Figure 12. Magnitude and phase Bode diagrams of the inverter-based amplifier, with a load capacitance of 1 pF (**top**) and DC input-output differential characteristics (**bottom**) at V_{DD} = 0.3 V and V_{DD} = 0.15 V.

3.5. Device Sizing

The modulator was designed with the 0.18-µm UMC CMOS process, with the device parameters shown in Table 1. Minimum channel lengths were adopted in order to improve speed performances. Body biasing for pMOS transistors of the inverter-like amplifiers was employed to enhance the maximum operating frequency; in particular, their bodies

were connected to ground in order to reduce their threshold voltages and consequently moderate the request for high aspect ratios, typically larger than the nMOS to counteract the lower mobility. The same technique is not suitable for the nMOS devices, due to the absence of a p-well isolated from the substrate in the used technology. Thanks to the clock-boosting circuit, it was possible to assign a reasonably low width to the pass-gates, thus keeping under control charge injection issues, as well as the parasitic capacitances. As for the amplifier inverters Inv_1 and Inv_2 of Figure 11, instead, high aspect ratios are needed to reach a sufficient GBW. The other inverters $Inv_{3\text{-}9}$ were sized with the same strategy described in [27]. The diode-connected inverter Inv_0, which provides the constant bias voltage V_{inv} (close to $V_{DD}/2$), is a scaled version of $Inv_{1,2}$.

Table 1. Sizes of MOSFETs of the modulator.

Device	L_p [nm]	W_p [µm]	L_n [nm]	W_n [µm]
Amplifier Inverters:				
• $Inv_{1,2}$	180	12.5	180	12.5
• $Inv_{3,4}$	180	1.25	180	1.25
• $Inv_{5,6}$	180	6.25	180	6.25
• $Inv_{7,8,9}$	180	0.5	180	0.5
Reference Inverter Inv_0	180	2.5	180	2.5
DAC Inverters	180	12.5	180	12.5
Comparator Inverters	180	12.5	180	12.5
Comparator Pass Transistors	180	1.25	180	1.25
Pass Gates	180	1.92	180	0.96

The capacitors represent the main contribution to the estimated total area occupation of the modulator. We tried to keep them as small as possible, but with some limitations. The value of the sampling capacitors C_S of the first integrator impact directly on the converter thermal noise. Another constraint is represented by the ratios C_S/C_F, C_{S2B}/C_{F2}, and C_{S2A}/C_{F2}, sized equal to $b_1 = a_1$, a_2, and c_1, respectively. The coefficient set used in this design corresponds to the Set 2 discussed in Section 2. Their values are summarized in Table 2, resulting in an estimated area of 0.03 mm^2, obtained by summing up the area occupied by all components, excluding the interconnections. Note that, in the technology used in this work, active devices can be placed below the Metal-Insulator-Metal (MIM) capacitors, which turn out to be the dominant factor. For this reason, the area estimation of the proposed ADC coincides with the capacitor area. C_{up} and C_{down} were not included in this area estimation, because they are not properly part of the modulator: The clock boosting circuit, in fact, may be shared among several blocks in a complete ULV data acquisition system. They are equal and were set to 1 pF.

Table 2. The sizes of the capacitors.

C_S [fF]	C_T, C_H, C_F [pF]	C_{S2A} [fF]	C_{S2B} [fF]	C_{F2} [pF]
200	4.25	47	493	1

4. Simulation Results and Discussion

The modulator was validated by means of electrical pre-layout simulations performed with Cadence Spectre™; in particular, transient noise simulations have been performed in order to also take into account electrical noise. In all simulations, the supply voltage and OSR were set to 0.3 V and 128, respectively, if not otherwise specified. The bitstream was processed by a VerilogA decimation filter to extract the output codes. We will call PI a modulator where, for the first integrator, a standard parasitic-insensitive architecture [38] is employed, with the amplifier, the sampling capacitor, and the capacitive ratios kept unchanged. The performances of the PI modulator will be compared with our proposed

modulator, in order to highlight the benefits of the high-gain SC integrator depicted in Figure 7.

The spectrum of the output bitstream is plotted in Figure 13, where the input is a sinusoidal waveform with frequency 80 Hz and peak-to-peak (p-p) amplitude 450 mV. The clock frequency is set to 164 kHz. The SNR and SNDR resulted to be 76.7 dB and 73.1 dB, respectively. The Total Harmonic Distortion (THD), defined as the ratio between the distortion and the input signal power P_{THD}/P_{IN}, was about −75 dB. Excluding the clock-boosting circuit, the power consumption P_D was equal to only 200.5 nW. The Schreier Figure of Merit (FoM) can be calculated as:

$$FoM = SNDR + 10\log\frac{B_W}{P_D} = 168.14\,dB, \tag{3}$$

which is among the best ones of ULV ΔΣ modulators.

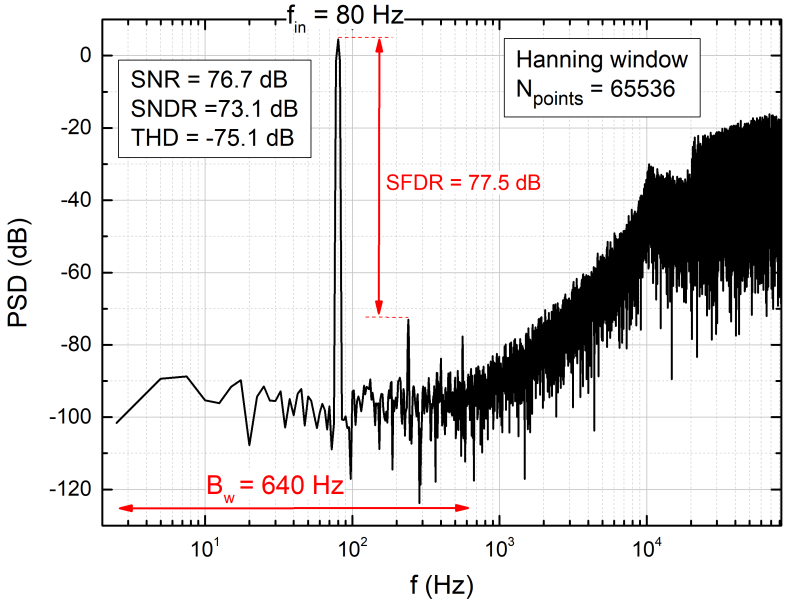

Figure 13. Output bitstream spectrum at V_{DD} = 0.3 V, with a clock frequency of 164 kHz, a sinusoidal input signal at 80 Hz with a p-p amplitude of 450 mV.

The DC transfer function was also extracted, in order to assess the gain error ε_G: The results are visible in Figure 14. In the proposed architecture, ε_G resulted to be 60 times lower than in the PI modulator, being equal to just 0.014%. The gain error improvement is consistent with the low DC gain sensitivity of the employed SC integrator, that is inversely proportional to the cube of the inverter-like amplifier DC gain. Furthermore, a temperature sweep was conducted and Figure 15 shows the results of this simulation. The dissipated power has an exponential dependence with the temperature, as expected by the weak inversion bias region of the inverter-based amplifiers. For the same reason, the amplifier bandwidth has a similar exponential behavior with temperature, explaining the worsening of the modulator dynamic performances at the lowest temperatures.

The Power Supply Rejection Ratio (PSRR) has been tested by superimposing a sinusoidal waveform with a 10-mV amplitude at different frequencies on the nominal supply voltage, not affecting the reference voltages V_{ref+} and V_{ref-}. Each point of the PSRR curve plotted in Figure 16 is evaluated by averaging over the PSRR values obtained from 200 Monte Carlo (MC) runs. Nominal simulations, in fact, are useless to estimate the actual PSRR of the circuit, due to the symmetry of the FD modulator. The error bars represent the minimum and the maximum PSRR values obtained from the 200 MC runs, for each ripple frequency. Moreover, considering the ratiometric operation of the ADC, we performed an additional test by feeding the input with a constant fraction (50%) of the supply voltage. In

the ideal case, this should result in a constant output code (50% of full scale). The actual variation estimated by varying V_{DD} across the interval 0.27–0.33 V was lower than 0.08% of full scale, proving that low sensitivity to supplies voltage variations.

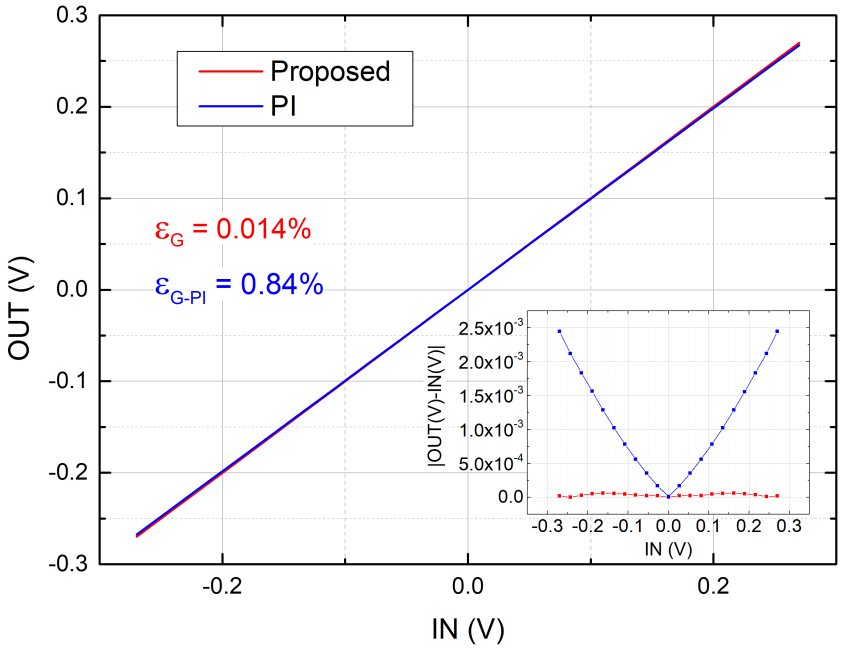

Figure 14. Input-output DC characteristic of the proposed modulator vs. PI modulator. The inset shows the comparison between the absolute errors of the two modulators.

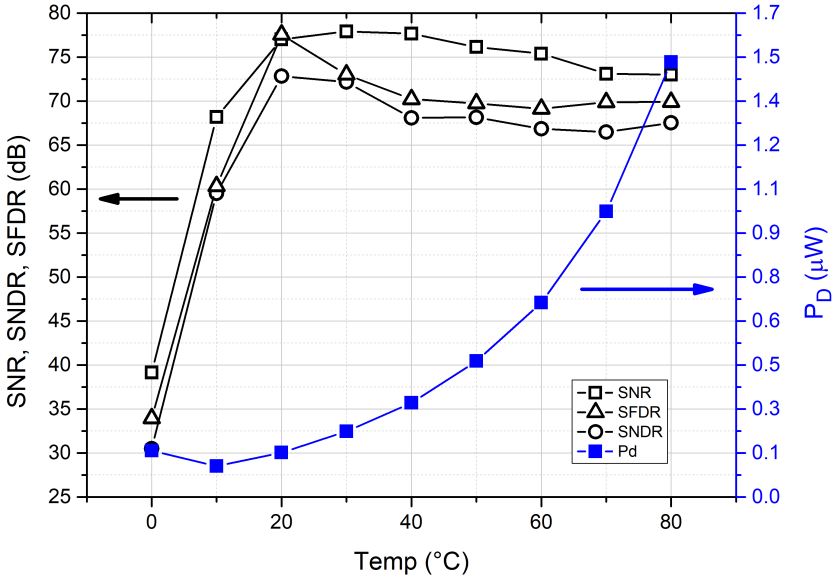

Figure 15. SNR, SNDR, SFDR, and dissipated power vs. temperature, with V_{DD} = 0.3 V, a clock frequency of 164 kHz, a sinusoidal input tone at 80 Hz with an amplitude of 0.75V_{DD}.

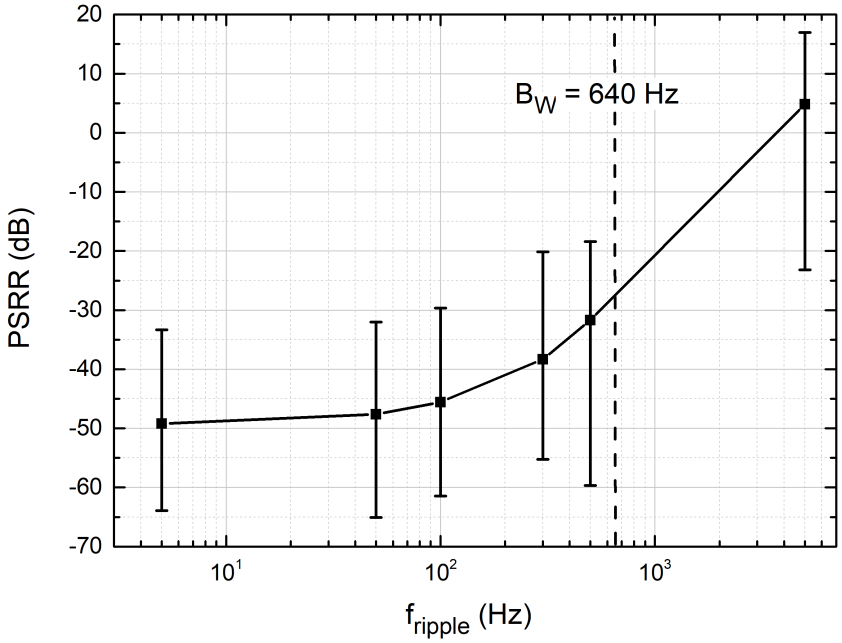

Figure 16. PSRR vs. ripple frequency, with a nominal supply voltage of 0.3 V, a ripple amplitude of 10 mV, and a clock frequency of 164 kHz. The plotted curve is evaluated by averaging the results over 200 MC runs. The error bars represent the interval of PSRR values obtained from the MC runs for each ripple frequency.

MC simulations were also performed to evaluate the offset of the modulator. The offset mean value estimated over 200 MC runs is 16 µV, and the standard deviation σ is 0.47 mV. A histogram that describes this spread is depicted in Figure 17, where it is also shown how the offset changes for the PI modulator. In the latter case, the standard deviation increases by a factor greater than 5.7, demonstrating the effectiveness of the CDS technique intrinsically operated by the first integrator.

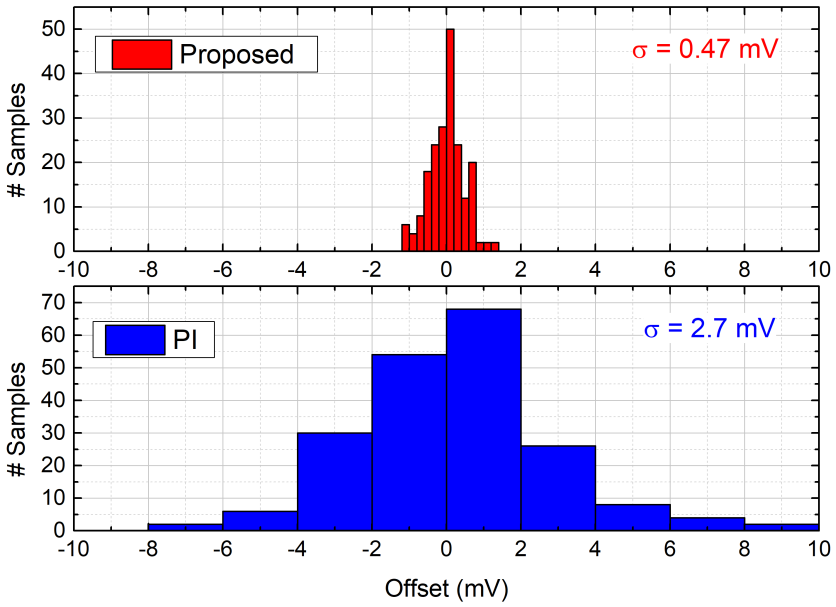

Figure 17. Comparison of offset spread over 200 MC between our architecture and the PI modulator V_{DD} = 0.3 V.

Table 3 summarizes the spread of the most relevant parameters over corner variations. Due to the sub-threshold operation of the devices, the amplifier bias current exhibits very

large relative variations against process spread (mainly due to threshold voltage variations), strongly affecting the maximum operating frequency. For this reason, the frequencies at which the parameters in Table 3 have been determined are different for each corner. It is worth noting that, in the SS corner, the modulator dissipates less power but is capable of working with a sampling frequency around four times lower than in the typical corner. Analogous considerations explain the performances in the FF corner, while the condition of Slow NMOS/Fast PMOS represents the worst case in terms of distortion.

Table 3. Performance spread over corner variations at V_{DD} = 0.3 V.

	TT	SS	FF	FNSP	SNFP
f_S [kHz]	164	41	655	82	82
SNR [dB]	76.7	83.9	76.6	72.1	77.4
SNDR [dB]	73.1	63.2	64.6	68.4	59.2
SFDR [dB]	77.5	64.0	65.4	73.2	59.3
B_W [Hz]	640	160	2560	320	320
P_D [nW]	200	36	1100	210	192
FoM [dB]	168.1	159.8	158.2	160.3	151.4

The modulator was designed with the target supply voltage of 0.3 V, but it is interesting to check its performances with a much lower supply voltage. Figure 18 shows the output bitstream spectrum at V_{DD} = 0.15 V, when the input is a sinusoidal waveform with frequency 1 Hz and p-p amplitude 112.5 mV. The clock frequency is set to 2 kHz.

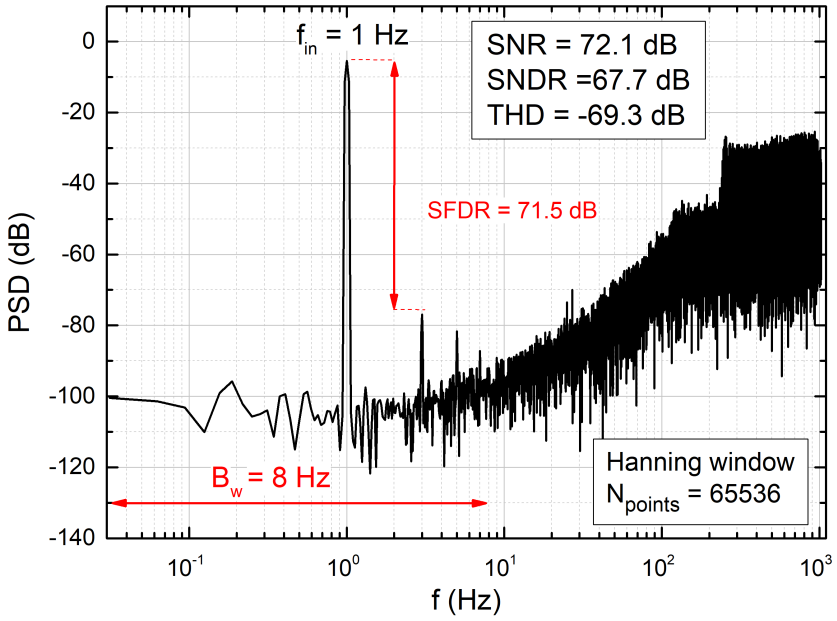

Figure 18. Output bitstream spectrum at V_{DD} = 0.15 V, with a clock frequency of 2 kHz, a sinusoidal input signal at 1 Hz with a p-p amplitude of 112.5 mV.

In these operating conditions, the modulator managed to achieve an SNR of 72.1 dB and an SNDR of 67.7 dB, with a power consumption of just 8.06 nW. The latter was reduced by nearly a factor of 25, but also the maximum clock frequency decreased (and thus the bandwidth). The resulting FoM was 158 dB, which is still a good value among ULV ΔΣ modulators. A temperature sweep was conducted also with V_{DD} = 0.15 V and the results are shown in Figure 19. The modulator behaviour is similar to the one shown in Figure 15 up to 60°C, where the dynamic performances start to drop due to the increase of the leakage currents, which disrupts correct operations of clock boosters. Concerning the effects of supply voltage variations, we fed the ADC input with a voltage equal to 50% V_{DD} and varied V_{DD} from 0.14 V to 0.16 V. The maximum variation of the output code across this

V_{DD} range was about 0.4% of full scale, revealing that reducing V_{DD} to this extremely low value increases the sensitivity to supply voltage.

Investigating the effects of process variations showed that, at V_{DD} = 0.15 V, it was impossible to find a sampling frequency where the ADC works properly, when SS, SNFP, and FNSP corners were considered. For these corners, correct operations of the modulator would require a further clock frequency reduction. Unfortunately, due to the leakage currents, the clock boosters are not capable of maintaining correct clock levels for such low frequencies. We focused on the worst case corner, the SS one, finding out that the lowest acceptable value of V_{DD} was 0.18 V. In Figure 20, we show the sampling frequency for the four supply voltage points. For each supply voltage/sampling frequency combination, we indicated also the SNDR. We could not find a convincing reason for the increase of SNDR at lower supply voltages (and slower sampling frequencies).

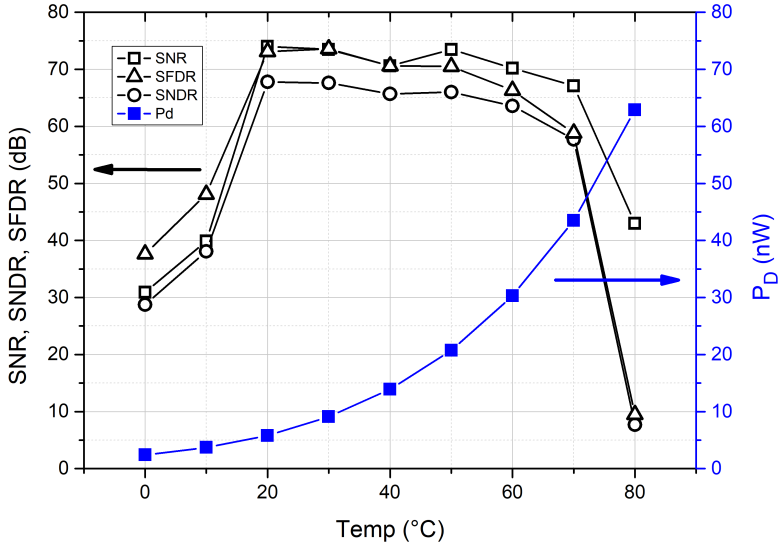

Figure 19. SNR, SNDR, SFDR, and dissipated power vs. temperature, with V_{DD} = 0.15 V, a clock frequency of 2 kHz, a sinusoidal input tone at 1 Hz with an amplitude of 0.75V_{DD}.

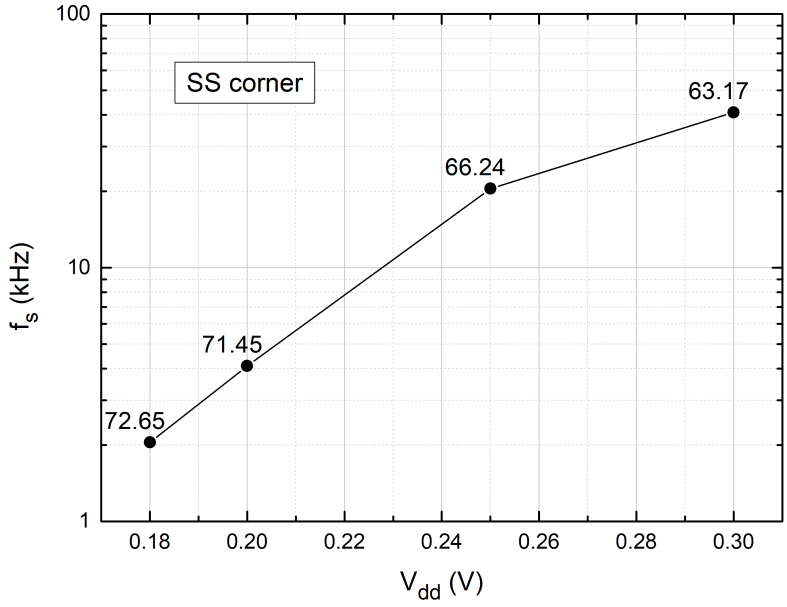

Figure 20. Maximum sampling frequency for 4 different supply voltages, in the SS corner. The label close to each point represents the SNDR of the modulator in the respective simulation conditions.

In a similar way to the case of higher supply voltage, we performed MC simulations to evaluate the offset of the modulator at V_{DD} = 0.15 V. The offset mean value estimated over 200 MC runs is −27.5 µV, and the standard deviation σ is 0.82 mV. Figure 21 shows the histogram of offset spread compared to the PI modulator, under the same supply voltage condition. As seen for V_{DD} = 0.3 V, the proposed modulator shows better performances compared to the solution employing the traditional integrator topology.

In order to predict the possible advances that can be obtained by means of the proposed architecture in the field of ULV data converters, the simulation results obtained in this work have been compared in Table 4 with other state-of-the-art ULV ΔΣ ADCs. Table 4 includes previous works on ΔΣ modulators based on different approaches, namely DT, Continuous-Time (CT), Voltage-Controlled Oscillator (VCO)-based, and Current-Controlled Oscillator (ICO)-based.

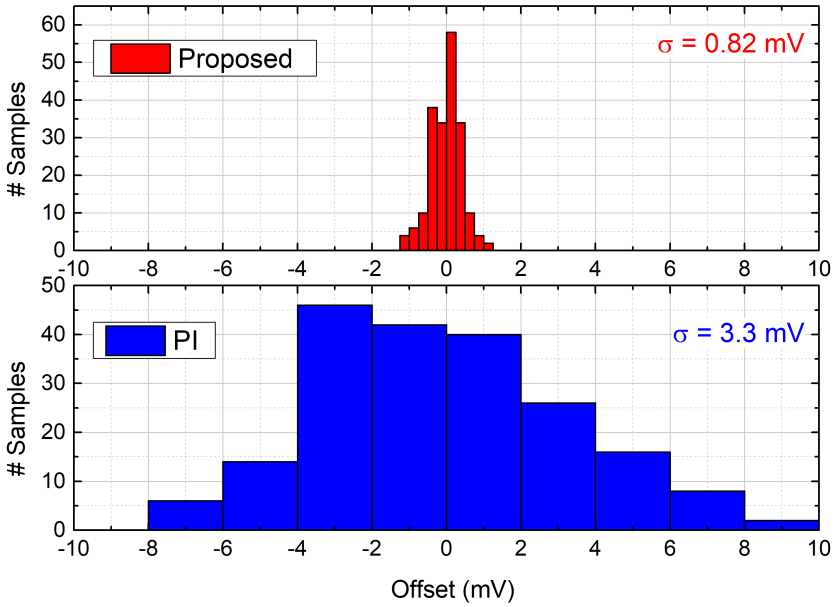

Figure 21. Comparison of offset spread over 200 MC between our architecture and the PI modulator at V_{DD} = 0.15 V.

Table 4. Comparison with the state of the art.

Device	This Work	[8]	[26]	[46]		[5]	[21]	[47]
Technology [nm]	180	130	180	130		65	65 LP	65
V_{DD} [V]	0.3	0.25	0.45	0.3		0.3	0.4	0.5
Architecture	DT 2	DT 3	CT 3	DT 4	CT 4	DT 2	DT 3	ICO 1
f_s [MHz]	0.164	1.4	10	2.56	6.4	0.256	0.75	10
B_W [kHz]	0.64	10	50	20	50	3	7.5	10
P_D [µW]	0.2005	7.5	28.72	79.3	26.3	0.181	12.7	0.276
SNR [dB]	76.7	64	71.24	74.6	68.7	64	64	58.2
SNDR [dB]	73.1	61	70.64	74.1	68.5	60	60.5	55.1
SFDR [dB]	77.5	70	82.43	83.4	82.6	-	-	-
Area [mm^2]	0.03 *	0.34	0.36	0.74	0.014	0.195	0.38	0.015
FoM [dB]	168.1	152.3	170.7	158	161.3	162.2	148.21	160.7

* Estimation performed considering the area of all the circuit devices, excluding interconnections.

From the comparison, it appears that the proposed architecture can produce values of the FoM very close to the best literature result [26], while being able to work with a considerably lower supply voltage. The total power consumption is also very close to the best figure [5] in Table 4, which makes the proposed modulator a promising solution for a large variety of energy harvesting applications and, in particular, for ultra-low voltage sources, as biofuel cells. It is worth highlighting that, while other works of Table 4 present

measurement outcomes, our results are projections based on electrical simulations, aimed at assessing the modulator functionality and its robustness with respect to PVT variations.

5. Conclusions

Important modulator issues such as gain error, dead-zones, degradation of noise-shaping function, low-frequency noise, and offset introduce severe penalties on the overall performances of ΔΣ ADCs. By means of high-level simulations, we discussed the impact of these non-idealities especially when related to ultra-low voltage scenarios, focusing on the effect of the integrator finite DC gain and the modulator coefficients. In order to counteract some of the above mentioned issues, we designed a ΔΣ modulator capable of working with ultra-low supply voltages, which takes advantage of a high-DC gain switched-capacitor integrator and a fully-differential inverter-like amplifier, both recently proposed. In the nominal corner, it reached an SNDR of 73 dB, with a clock frequency of 164 kHz and a dissipated power of only 200.5 nW, at a supply voltage of 0.3 V: The Schreier's FoM reached 168.1 dB. Its gain error was also estimated and resulted in just 0.014%, while the offset had a standard deviation of 470 μV. The benefits introduced by the employed switched-capacitor integrator topology with respect to a standard one were highlighted. Simulations over different process corners, temperatures, and supply voltage variations were used to estimate the spread of the main performance parameters, in particular showing some critical issues when coming to lower supply voltages, down to 0.15 V. The performances of this modulator make it extremely useful in the energy harvesting scenario, as, for example, in a biofuel cell-powered system.

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