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An Analog Voltage Similarity Circuit with a Bell-Shaped Power Consumption

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Abstract: This paper presents a voltage similarity circuit (bump circuit) based on a novel voltage correlator. The proposed circuit is characterized by a power consumption which depends on the similarity between the two inputs. The sensitivity of the bump circuit and the power consumption are at the highest values when the inputs are equal. As the similarity between the input voltages decreases, the total current consumption decreases with a bell-shaped behavior. The proposed bump circuit is very simple in design, made of a new voltage correlator circuit in combination with a differential pair and mimics the behavior of the classical bump circuit. The voltage correlator was implemented using AMS – 350 nm CMOS technology. Simulation and measurement results suggest that a low power consumption may be achieved if the circuit is used in applications where the input signals have large dissimilarity for most of the circuit operation.

Keywords: voltage correlator; analog similarity; bump circuit; low power; bell-shaped

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1. Introduction

Circuits performing mathematical and logical operations, have been a research subject for many years [1]. Electrical signals, i.e., currents and voltages are suited for this purpose and variety of circuits and systems are proposed throughout the years. Circuits based on operational Amplifiers [2,3] can perform operations, such as addition, integration, inversion, multiplication, exponentiation, logarithm, division, etc. Analog signal processing, however, suffers from inaccuracy and is more susceptible to noise compared to their digital counterparts. Today, digital signal processing has become the dominant method thanks to introduction of integrated circuits which allows for higher integration and clock speeds. Despite this fact, analog signal processors are often far more effective and simpler in design than their digital counterparts [4–6]. Finding similarity or correlation between two or more analog signals is a good example. Current correlators [7] are used to find the correlation between two currents and voltage similarity circuits to find the similarity between voltages. One of the simplest and well-known voltage similarity circuits is the bump circuit presented by Tobias Delbrück [8] in 1991. Voltage similarity circuits are widely used in analog systems, such as in ultra low power energy harvesters [9], neuromorphic systems [10], and biological inspired circuits [11]. One of the main challenges with these circuits are the relatively high power consumption as they must be active all the time. Different approaches exist to lower the power consumption, such as clocking and/or lowering the power supplies, optimizing transistor sizes, and/or decreasing the bias voltages to limit the currents in the circuits. All of these methods will affect the operation of the circuit and can potentially decrease the sensitivity. Lu et al. [12] presented a bump circuit with a power consumption of $18.9\text{ nW}@V_{dd} = 3\text{ V}$ using a novel pseudo-differential transconductor. This circuit requires additional complicated biasing circuitry which may make the design more challenging compared to the presented circuit. Pheng et al. [13] exploit the properties of multiple input floating-gate technique to realize a tunable bump circuit.

The main drawback with this circuit is that it needs a complicated digital circuitry for programming the floating gates. Other similarity circuits have also been presented which offer tunability [14–16].

This paper is an extended version of a previously published paper [17], which introduced the concept. In that paper, we presented a new voltage similarity circuit (bump circuit) where the power consumption depends on the input voltages. It can potentially have lower power consumption compared to the classic bump circuit with the same functionality. In this paper, we present measurements results from a 350 nm ASIC from AMS and compare these to simulations. Simulations are done using Cadence with 350 nm CMOS models from AMS. In addition, the gain and common-mode behavior of the circuit are analyzed and an example of a energy harvester system, which may take advantage of the proposed bump circuit is presented.

2. New Voltage Correlator Circuit

The proposed voltage correlator circuit is shown in Figure 1. The correlator circuit consists of two equal legs with diode-connected transistors $M3$ and $M4$ in series with transistors $M1$ and $M2$, respectively. The gates of transistors $M1$ and $M2$ are connected to the gate of diode-connected transistor at the opposite leg. If the voltages $V1$ and $V2$ are equal and high enough to keep $M1$ and $M2$ in triode, i.e., $V_{gs1,2} > V_{th} + V_{d1,2}$, both legs conduct equally, and the currents are at their maximum values.

Figure 1. The proposed voltage correlator, where the currents $I1$ and $I2$ approach their maximum values when voltages $V1$ and $V2$ become equal.

In this state, the currents $I1$ and $I2$ are roughly decided by the diode-connected transistors that are in saturation and can be approximated by

$$I_{1,(2)} = \frac{\beta_{3,(4)}}{2} (V1 - V_{d1,(d2)} - V_{th})^2, \quad (1)$$

where $\beta = \mu C_{ox}(W/L)$, and V_{th} is the threshold voltage. Assuming $M1$ and $M2$ are in deep triode, V_{d1} and V_{d2} can be given as

$$V_{d1,(d2)} = I_{1,(2)} \times R_{M1,(2)} = \frac{I_{1,(2)}}{\beta_{1,(2)}(V1(2) - V_{th})}, \quad (2)$$

where $R_{M1,2}$ are the channel resistances at deep triode, which may be approximated by

$$R_{M1,(2)} = \frac{1}{\beta_{2,(1)} \times (V2,(1) - V_{th})}. \quad (3)$$

As the voltages $V1$ and $V2$ across the two legs become different, the transistors will behave differently. If all the transistors in the circuit are equal in size, currents in both legs will remain almost equal. In this state, the currents are always limited by the leg with the lowest of the two voltages. If $V1$ increases and $V2$ decreases, the voltages across $M1$

and $M3$ increase, and $M1$ goes into saturation, and $M2$ goes into deeper triode region. According to Equation (3), the resistance of $M2$ decreases, and the voltage $Vd2$ approaches the ground value. In this state, $M4$ forms a current mirror with $M1$, which controls and limits the current $I1$ equal to $I2$, as shown in Figure 2. The body effect of $M4$ decreases as its source approaches ground. Similar behavior can be expected when $V2$ becomes larger than $V1$.

Figure 2. A simplified circuit when $V1$ becomes larger than $V2$. In this case, $M4$ is omitted as it is in deep triode ($V1 \gg V2$), and the circuit behaves as a simple current mirror.

As $V2$ decreases, $I1$ will decrease. If we ignore the channel modulation effect of $M1$, the current $I1$ can be expressed as:

$$I1 = I2 = \frac{\beta_4}{2}(V2 - V_{th})^2. \quad (4)$$

As explained earlier, the correlation between the two voltages $V1$ and $V2$ is through the current mirrors created between the two legs of circuit. The weighting between the transistors forming the current mirror will, therefore, control the amount of current in each leg. Figures 3 and 4 show how the voltages $Vd1$, $Vd2$ and the currents $I1$ and $I2$ are affected when the widths of the transistors $M1$ and $M2$ are increased from $1 \mu\text{m}$ to $10 \mu\text{m}$ simultaneously, and $M3$ and $M4$ are kept constant at $1 \mu\text{m}$. From the current simulation in Figure 3, we can see that the two currents are equal and at their maximum when $V1$ is approximately equal to $V2$ when all device widths are $1 \mu\text{m}$, i.e., the mirror is balanced. This figure shows that as the widths increase, the currents increase. When the mirror is formed due to difference between the voltages $V1$ and $V2$, the increased width increases the difference between the currents. Figure 4 shows as the widths increase, the voltages $Vd1$ and $Vd2$ are pulled closer to ground due to even larger ratio between the transistors in the current mirrors and higher conductivity in the transistors, i.e., less resistance. To summarize, the increased width has two important effects, one is that the resistance of the transistor in triode decreases, which makes the current mirror more ideal with less body effect and it makes the mirror unbalanced, i.e., the current in one leg becomes higher than the other one. As we will show later when this circuit is used in a bump circuit, an unbalanced current mirror is necessary to create the bump at the output current correlator.

The transistors in the simulations and measurements presented have lengths of 500 nm and widths of $1 \mu\text{m}$ if not stated in the text explicitly. Transistors $M1$ and $M2$ have widths of $15 \mu\text{m}$. The bias voltage V_{Bias} is set to 2.35 V , and V_{dd} is 3.2 V in both measurements and simulations if not stated explicitly in the text.

Figure 3. Simulation of currents $I1$ and $I2$ when the widths of the transistors $M1$ and $M2$ are increased from $1\ \mu\text{m}$ to $10\ \mu\text{m}$ simultaneously with a common-mode voltage of $V_{dd}/2$. The curves are normalized for the maximum value of the currents in the legs. The dashed curves are the sum of the normalized currents which has a bell shape.

Figure 4. Simulation results of voltages $Vd1$ and $Vd2$ when the widths of the transistors $M1$ and $M2$ are increased from $1\ \mu\text{m}$ to $10\ \mu\text{m}$ simultaneously.

Voltage Correlator Connected to a Differential Pair

By cascoding a PMOS differential pair to the voltage correlator as shown in Figure 5a, the functionality of these two circuits is combined. The currents through each leg of the combined circuit are denoted $Ic1$ and $Ic2$ and shown in Figure 6 as the black curves. This figure shows also the currents in the voltage correlator $I1$, $I2$ presented earlier as the blue curves and the currents in a differential pair denoted I_{diff1} , I_{diff2} as the red curves for comparison. The solid curves are the currents through the left leg, and the dashed ones are the currents in the right leg. The rapid decrease of current when the two inputs become equal is caused by the differential pair. From the simulation, we can see that currents $Ic1$, $Ic2$ follow I_{diff1} , I_{diff2} when the two input voltages are close to each other and follow the currents $I1$, $I2$ when the inputs become different.

Figure 5. (a) Stacking of a PMOS differential pair and the proposed correlator circuit. The behavior of currents $Ic1$ and $Ic2$ is a combination of the current behavior of the correlator and a differential pair. (b) Circuit model of the combined circuit when $V2$ increases and $V1$ decreases.

Figure 6. Simulation of the currents I_{c1} and I_{c2} in the circuits shown in Figure 5 as black curves. The currents in the circuit in Figure 1 and a differential pair with resistive load are also presented for comparison. The dashed curves are the currents through the right leg of the circuit, and the solid curves are the currents in left leg. All the curves are normalized by their maximum value.

When the inputs are equal, the transistors $M1$ and $M2$ are in deep triode and all other transistors are in saturation, i.e., voltages V_A and V_B will be just above threshold voltage. The current can be approximated as

$$I_{c1} = I_{c2} = \frac{\beta_{6(5)}}{2} (V_{dd} - V_2(1) - V_{th})^2. \quad (5)$$

As the difference between the inputs increases, the circuit will change its state. Assuming V_1 decreases and V_2 increases, the circuit can be represented as in Figure 5b. Transistors M_5 and M_2 go into triode and all the others in saturation. The current I_{c2} is then mirrored into I_{c1} . M_3 will act as a diode connected transistor with a voltage approximately equal to the threshold voltage across it. The current in this state can be approximated as

$$I_{c1} = I_{M1} = I_{M3} = I_{M5} = KI_{M6}, \quad (6)$$

where K is the ratio between the widths of the transistors forming the mirror $M1$ and $M4$. If we ignore the effect of this diode connected transistor, i.e. $M3$, and assuming that $M5$ is in deep triode, the circuit can be modeled in strong inversion as

$$\begin{aligned} I_{c1} &= \beta_5((V_{dd} - V_1 - V_{th})V_{DS}) \\ &= K \frac{\beta_6}{2} (V_{dd} - V_2 - V_{th})^2. \end{aligned} \quad (7)$$

Figure 7 shows the currents in circuit shown in Figure 5a when the widths of transistors $M1$ and $M2$ are increased from $1 \mu\text{m}$ to $10 \mu\text{m}$ simultaneously, and $M3$ and $M4$ are kept constant at $1 \mu\text{m}$. From the figure, we can see that the variations in currents due to the changes in the width of the transistors are smaller compared to the simulation in Figure 3, which is caused by the differential pair. The simulation shows the current I_{c1} and I_{c2} as solid and circled curves, respectively, and the total current in the circuit I_{tot} as dashed curves.

Figure 7. Simulation result of the circuit shown in Figure 5a. The widths of transistors M1 and M2 are increased from 1 μm to 10 μm simultaneously as marked by the arrows and M3 and M4 have a constant width of 1 μm . The total current I_{tot} , which is the sum of the two currents is shown as dashed curves with a clear bell shape.

3. The Proposed Bump Circuit

By correlating the currents I_{C1} and I_{C2} in the circuit shown in Figure 5a using a current correlator made of two series connected transistors, the circuit will become a voltage similarity (bump) circuit as shown in Figure 8a. This bump circuit will have a similar behavior as the classic bump circuit developed by Delbrück [8] shown in Figure 8b. The output current of the bump circuit in weak inversion and strong inversion are given in Reference [8,15], respectively.

Figure 8. Schematic of (a) the proposed bump circuit and (b) the classic bump circuit presented by Tobias Delbrück.

When the inputs are similar, the circuits in Figure 8a,b will behave similar and have the same current consumption. When the inputs become different, the current consumption of the classic bump circuit increases, while the proposed bump circuit will have a decreasing power consumption.

Figure 9 shows the voltages at the drain of the different pair for both bump circuits denoted V_A and V_B in Figure 8a and V_C and V_D for the classic bump circuit in the Figure 8b. Voltages V_A and V_B in the proposed bump circuit change their state from rail to rail as the input voltages cross each other, but V_C and V_D in the classic bump circuit change only between ground and the threshold voltage of the devices as they are connected as diodes. Voltages V_A and V_B can in some cases be regarded as a digital signal that changes its state when the inputs cross each other.

Figure 9. Simulation result of voltages V_A and V_B in Figure 8a and Voltages V_C and V_D in Figure 8b.

Figure 10 shows the simulation of the proposed bump circuit and the classic one when a differential voltage is applied to their inputs. The solid black and red colored curves marked I_{tot} are the total current consumption of the classic bump circuit and the new proposed circuit, respectively. The variation in current consumption of the proposed bump circuit follows a bell-shaped curve.

Figure 10. Comparison of the currents in the proposed bump circuit and the classic bump circuit. The black curves are the normalized currents in the classic bump circuit and the red curves the currents in the proposed circuit. The dashed curves are the output currents.

The total static power consumption for all the combination of the input voltages of the proposed bump circuit and the classic bump is illustrated as a 3-d graph in Figure 11a,b, respectively. It is clear from the simulation that the proposed bump circuit will achieve low power consumption when one or both of the inputs are close to V_{dd} , approximately above 2.5 volts in this simulation.

Figure 11. Total static current consumption for all the input voltage combinations for the proposed bump circuit (a) and the classic bump circuit (b). The ratio between the total static power consumption of the classic and the proposed power bump circuit is shown in (c).

The power consumed by the proposed bump circuit and the classic are compared and shown in Figure 11c. The relation between power of the two circuits increases exponentially with the increase in the difference between the input voltages. For the simulation in Figure 11c, it is as high as 5 orders of magnitude when the difference between the inputs approaches maximum.

The simulation in Figure 10 shows also the output currents I_{out} in both the classic bump circuit as dashed black curve and the proposed bump circuit as dashed red curve. When the input voltages V_1 and V_2 are equal, I_{out} is large and equal for both circuits. When the difference between the input increases, the output currents in both bump circuits decrease. In the classic bump circuit, the output current I_{out} is close to zero as the inputs become different, while in the proposed bump circuit, the output current becomes null only when the $|V_2 - V_1| \gg 0$. This difference is due to the fact that the sources of the diode connected transistors M_3 and M_4 in the proposed circuit are not completely grounded when the inputs are different, causing the output transistors to leak. This current leakage can be reduced by increasing the width of the transistors M_1 and M_2 to create a stronger ground as explained in Section 2. The effect of increasing the width of these transistors are shown in Figures 3, 4, and 7.

A well known non-ideality of the current correlator used in both circuits is the asymmetric bump at the output, which is caused by the fact that the series connected transistors M_8 and M_9 have different source voltages. This can be solved by adding an extra pair of transistors connected in parallel with M_8 and M_9 where their gate connections are interchanged as in References [12,14].

Common-Mode Behavior of Proposed Bump Circuit

The behavior of the proposed bump circuit, including its power consumption and the gain, is highly dependent on the input common-mode voltage. Figure 12 shows the sensitivity (S) of the proposed bump circuit at different common-mode voltages defined as

$$S = \frac{d(I_2 - I_1)}{d(V_2 - V_1)}. \quad (8)$$

The simulation results show that maximum gain is achieved at low common-mode voltages and decreases as the common mode voltage increases. This is expected due to larger currents in the circuit. This behavior would be opposite for NMOS input transistors, i.e., the gain would be at its maximum at higher voltages closer to V_{dd} .

Figure 12. The curves show the sensitivity of the proposed bump circuit when the two inputs have common-mode value increasing from 0 to V_{dd} . The bias voltage is 2.6 V in this simulation.

Figure 13 shows the power consumption of the proposed bump circuit at different input common-mode voltages. The figure shows the simulation when the inputs cross each other at common-mode voltage levels = 0 V, 0.5 V, 1 V, 1.5 V, 2 V, 2.5 V, and 3 V. This simulation shows that the power consumption increases as the similarity occurs at lower voltages. The change in the common-mode voltage also changes the width of the bell. To

be able to analyze this characteristic in more details, we measured the full width of half the maximum (*FWHM*) of the bell-shaped current consumption as shown in Figure 13. We used two different parameters to analyze the power consumption as function of the common-mode voltage, quality *Q* and efficiency *E*. *Q* is the blue dashed curve in Figure 14 and defined as

$$Q = \frac{CMV}{FWHM'} \quad (9)$$

where *CMV* is the common-mode voltage. The power efficiency is shown as the green curve and defined as

$$E = \frac{I_{peak}}{FWHM'} \quad (10)$$

where *I_{peak}* is the maximum current consumption at the common-mode voltage and is shown in the figure as the black solid curve. The analysis show that efficiency reaches its maximum at common-mode voltage = 2.6 V. The product of the *I_{peak}* and the *FWHM* is also shown as the dashed black curve which relates to the average power consumption. From these analyses, we can conclude that the circuit is more effective at common-mode voltages close to *V_{dd}*.

Figure 13. Simulation of total current for similarities between inputs at common-mode voltages 0 V, 0.5 V, 1 V, 1.5 V, 2 V, 2.5 V, and 3 V. The bias voltage is 2.6 V in this simulation. Arrows show the *FWHM* for each common-mode value.

Figure 14. The power effectiveness and consumption is depending on the common-mode voltage of the input signals. The circuit is most effective regarding the power consumption when the common-mode is close to *V_{dd}* = 3.2 V.

Table 1 compares the performance of the proposed circuit with other bump circuits described in the current literature.

Table 1. Comparison of bump circuits. <Nr of devices> in the table is the minimum number of devices needed to realize the circuit. Results from “[8]” in the figure below are from the presented work.

Ref.	This Work	[8]	[12]	[13]	[14]	[15]	[16]
Vdd (V)	3.2	3.2	3	2	5	± 2.5	5
Power (W)	256 n	256 n	18.9 n	na	na	na	na
Technology	350 nm	350 nm	500 nm	1.2 μm	500 nm	3 μm	ALD1106/7
Nr of devices	10	8	18	15	11	14	11

The main feature and novelty of the presented circuit is that power consumption is dependent on the input voltages. To our knowledge, no other circuit offers this feature. Furthermore, it is worth mentioning that the design presented in this work was not optimized for minimum power consumption; however, we have achieved power consumption in nano-watt region. As the power consumption may vary and is dependent on application, we have chosen to compare the static power consumption when inputs are equal, i.e., maximum power consumption at common-mode voltage at $V_{\text{dd}}/2$.

The power consumption of Reference [8] is similar with ours as shown in the table. This is because the circuit in Reference [8] is most similar to ours and the best one for comparison. We have simulated both circuits and presented the results in Figures 10 and 11. Table 1 shows the maximum power consumption of our circuit which decreases as the inputs become different as shown in Figure 11a, but, for Reference [8], the power increases as shown in Figures 10 and 11b. The minimum power consumption of our circuit is not easy to determine as it can approach 0 and lower than Reference [12] when the difference between the inputs becomes large enough.

4. Measurement Results

The proposed bump circuit was fabricated using 350 nm CMOS from AMS. Micrograph of the bump circuit including two buffers used at the outputs is shown in Figure 15a. In this implementation, the bump was given a separate power supply pad in order to measure the characteristic bell shaped power consumption of the circuit. The output buffers are connected to V_{out} and node V_A . V_B was omitted due to its symmetrical behavior. In the figure, all the circuit ports and some of the parts are marked with black text. In this chip, the transistors $M1$ and $M2$ have a width of 15 μm and all others a width of 1 μm .

Figure 15. (a) Micrograph of the chip produced using the 350 nm CMOS from AMS. Each node named in the picture is according to the circuit shown in Figure 8a. Buffer1 is connected to V_A and Buffer2 to V_{out} . (b) the measurement setup on PCB.

The chip was mounted on chip-carrier and bonded in-house as shown in Figure 15b. Keysight DSOX3024T oscilloscope was used to read the output values, Fluke 45 multimeters was used for current measurement and Agilent 33521A signal generators was used to generate the input signals. The system was powered using GW GPS-3030 power supply.

Figure 16 shows the measurement of the output voltage V_{out} and the node VA at 10 kHz frequency. The behavior of the circuit matches the simulation result shown in Figure 9, which is shown as the black dashed curve in the figure. The node VA (red curve) follows V_2 and is at its lowest value when the input V_2 is at its minimum value. The voltage V_{out} goes low when the inputs are equal. V_{out} does not reach ground. The reason for this is unknown, but we think it may be due to the type of pad we used, which doesn't have the correct ground value since the chip was a mixed design sharing pads with other circuitry.

Figure 16. Measurement results of VA and V_{out} at 10 kHz frequency. The dashed black curve is the simulation result with same parameters.

Figure 17 shows the measured power consumption of the proposed bump circuit when V_2 is grounded, and V_1 is increased from ground to V_{dd} . The blue curve is the measurement result, and the green is the simulation result. The measured current does not reach zero due to the leakages in the protection diodes in the pad. Figure 18 shows the power consumption when the V_1 is decreased to ground from $V_{dd}/2$ and V_2 increased from $V_{dd}/2$ to V_{dd} simultaneously. In this figure, we have also added the simulation result for the classic bump circuit for comparison. The two previous measurement result confirm the variation in the power consumption of the circuit as a function of the input voltages.

Figure 17. Measurement and simulation results of total power consumption when V_2 is 0 V and V_1 increases from Gnd to V_{dd} .

Figure 18. Measurement result of the total power consumption when V_1 decreases from $V_{dd}/2$ to zero and V_2 increases from $V_{dd}/2$ to V_{dd} simultaneously.

We could not measure the currents in each leg using the ASIC; therefore, all the circuits were implemented using the IC *CD4007UBE* from Texas Instruments. Using this IC did not allow for sizing the transistors for optimal design and the measurements only serve the purpose of proving the concept. To realize the different circuits, we had to use more than one chip. The circuit in Figure 1 was realized using two chips as shown in Figure 19b and tested by applying differential input voltages V_1 and V_2 in the range [2 V–6 V] with input common-mode voltage at $V_{icm} = 4$ V. Measurement results for this circuit are shown in Figure 20. These measurement results provide the same wave forms obtained by the simulations in Figure 3, i.e., minimum currents I_1, I_2 at the maximum distance between the two input signals ($V_1 = 2$ V, $V_2 = 6$ V, and $V_1 = 6$ V, $V_2 = 2$ V) and a maximum correlation of I_1 and I_2 when $V_1 = V_2 = 4$ V.

Figure 19. Pin numbers and connections diagram for the IC *CD4007UBE* to realize (a) the classic bump using 2 ICs (b) voltage correlator using 3 ICs and (c) the proposed bump connection using 3 ICs. Bulks of NMOS are connected to *GND* and PMOS to *VDD*.

Figure 20. Measurement results for the circuit in Figure 1. The differential input signals V_1 and V_2 are varied in a range [2 V–6 V] with a step of $|0.1$ V| and characterized by an input common-mode of 4 V.

Next, the measurement results for the circuit combining the correlator circuit and a different pair as shown in Figure 19a are shown in Figure 21. These measurement results also match the simulations shown in Figure 6. It is interesting to note that this behavior of currents in the two legs matches the one presented in Figure 7 for device widths equal to $1\ \mu\text{m}$ in the current mirror. The figure shows also the total power consumption of the classic bump circuit realized using the 3 ICs. We can see that the power consumption reduces by almost 72 percent compared to the classic bump when the difference between the input voltages is 4 V.

Figure 21. Measurement results for the proposed bump circuit with input differential pair. The differential input signals $V1$ and $V2$ are varied in a range [4 V–8 V] with a step of $|0.1 \text{ V}|$ and characterized by an input common-mode of 6 V. $V_{Bias} = 7 \text{ V}$.

5. Double Charge Pump Interface with Bump Circuits

In the low power interface for a energy harvesting double charge pump proposed in Reference [9], the authors use two bump circuits for activating and deactivating the flyback switch, as shown in Figure 22. Capacitors C_{var1} and C_{var2} work differentially and pump charges from the reservoir capacitance C_{res} to the series connected capacitors C_s and C_{s2} . As the charges are being pumped, the voltage across C_s and C_{s2} increase. C_{s2} is chosen much smaller than C_s and when the voltage across C_{s2} reaches the voltage at C_{res} , the bump circuit 1 activates the flyback switch which transfers the charges to C_{res} through the inductor L_{fly} . The voltage V_{s2} is shown in Figure 23 as the dashed black curve and V_{res} as the dashed blue curve. We compared the proposed bump circuit and classic one with each other for this application through simulation. The green and red solid curves are the current consumption of the proposed and classic bump circuits, respectively. The proposed bump circuit consumes almost 3.5 times less power consumption on average in this operation. After the switch goes on, the charges will flow from C_s to C_{res} . V_s approaches the voltage across the C_{res} , and the bump circuit 2 turns off the switch. This voltage change tends to be large and abrupt. This operation will take advantage of the variable power behavior of the proposed bump circuit. More detailed description of this charge pump is found in Reference [9].

Figure 22. Simplified schematic of a double charge pump that uses two bump circuits to control the switch in the flyback.

Figure 23. Comparison of the total currents absorbed by the classic bump circuit (red curve) with a average of $8.44\ \mu\text{A}$ and the proposed bump circuit (green curve) $2.33\ \mu\text{A}$ used in a double charge pump shown in Figure 22 as on detector. The black dashed line is the voltage V_{res} , and the blue dashed curves is the voltages V_{s2} .

6. Conclusions

In this paper, we presented a bump circuit, which finds the similarity between two voltages based on a novel voltage correlator. The proposed bump circuit offers the same properties of the classic bump circuit with the main difference that the current consumption approaches zero as the inputs become different. When the input voltages approach each other, currents flow increases, which also increases sensitivity. The simulations and measurements proved that the proposed bump circuit can use several orders of magnitude less power than classic bump circuit at maximum. Applications where similarity of two voltages is normally large, such as the low power interface for a charge pump presented, exploit the low power properties of the circuit at maximum. The proposed bump circuit was analyzed using simulation and measurements for proving the concept.

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