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A High Efficiency Linear Power Supply with Pure Sine Wave for High Voltage Test

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Abstract: The input part of the high-voltage test power supply is usually composed of switching devices; however, the pulse-type periodic interference caused by the switching devices makes the monitoring of the test power supply partial discharge more difficult. Therefore, this paper proposes a high-efficiency and distortion-free linear power supply based on piecewise-linearization with all N-type transistor. Under the same DC input, multiple power transistors are connected to different taps of the same transformer. By controlling the period of linear conduction of each power transistor in turn, we ensure that the power transistor works on the linear side (biased towards saturation) to reduce its conduction voltage drop and the output realizes sinusoidal piecewise linearization, so that the converter can greatly improve the system efficiency. After that, from the perspective of the lowest sum of the transistor loss, an optimization method for the design of the multi-winding transformer ratio at each stage is proposed. Finally, a power supply prototype based on four-piece linear converter with an output voltage of 220 V was built. The experimental efficiency reaches 87.03%, and, additionally, if the linear amplification is divided into more sections, the efficiency can be further improved.



Citation: Chen, B.; Gao, W.; Chen, Y.; Tian, C.; Zhou, Y.; Xue, G. A High Efficiency Linear Power Supply with Pure Sine Wave for High Voltage Test. *Electronics* **2021**, *10*, 18. <https://dx.doi.org/10.3390/electronics10010018>

Received: 31 October 2020
Accepted: 22 December 2020
Published: 24 December 2020

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Keywords: power conversion; high voltage test supply; high efficiency; power loss

1. Introduction

The construction of Ultra-High Voltage (UHV) power grids is inseparable from UHV electrical equipment, which must undergo various insulation detection tests before being put into operation in the grid system. To successfully carry out various high-voltage tests of electrical equipment, high-voltage test power supplies are required to supply high-voltage. Determining the insulation status of the test power supply and accurately pre-warning the insulation failure can effectively improve the safety and stability of its operation, and it is necessary to carry out the partial discharge test [1].

One of the types of high-voltage test power supplies is power transformers, among which step-up transformers are often used as intermediate transformers to match the voltage of the power supply and the voltage required for the test. At present, power electronic switching devices are widely used to generate high-power sine waves as the energy source input of the high-voltage test power supply, but at the same time, the use of switching devices will also increase the difficulty of measuring the partial discharge of the transformer. When the switching device is turned on or off, it will emit a pulse interference signal. If the interference cannot be effectively suppressed, this pulse-type periodic interference makes the signal-to-noise ratio and sensitivity of the online detection low, so it is impossible to effectively and accurately perform real-time partial discharge online monitoring. The commonly used methods of partial discharge interference suppression can improve the accuracy of measurement to a certain extent, but if the pulse-shaped periodic interference caused by switching devices is fundamentally avoided, the problem of difficult partial discharge detection can be solved. There is no pulse signal when the input power

supply based on the mechanism of the analog amplifier works, and the power device works in a linear state. Traditional linear power converters have the advantages of smooth output waveforms, close to standard sine waves, fast dynamic response characteristics and wide frequency bandwidth, but serious power consumption problems have become the technical bottleneck for their application in high power occasion [2,3].

Currently, the efficiency of linear amplifiers is mainly improved by switch-linearity hybrid power converter. Jin et al. [4–6] improve the efficiency and response speed of communication power by introducing a switching link in the linear amplifier. The linear amplifier compensates the waveform, and the switching link bears most of the power output. Qianzhi et al. [7,8] use the output of a switching circuit as the power supply for a linear amplifier. Both track the same reference signal source, and the output takes into account the characteristics of excellent waves and high efficiency. Liu et al. [9] combines a multilevel switch converter structure with a linear amplifier circuit, and it achieves the optimal performance of fast reference tracking and linear regulation efficiency, which enables the RF power amplifier circuit to achieve both linearity and efficiency in modern communication systems. This type of converter improves the accuracy of the output voltage waveform, but still has electromagnetic compatibility problems caused by switching noise.

Fujita et al. [10] proposes a diode-clamped high-efficiency linear amplifier topology, which uses a lower DC level to supply power when the output voltage is low. As the output voltage increases, the DC power supply automatically switches to a higher level. By reducing the difference between the output voltage and the DC power supply level, thereby it obviously improves the efficiency. Fujita et al. References [11,12] apply this amplifier to motor speed control and transmission systems, and good results can be achieved. However, the circuit structure is relatively complicated, and the utilization ratio of the semiconductor is low. The topology uses transistors in series and the P-type transistors must be used, which limits the further improvement of efficiency. Due to the capacity of the P-type transistor, the further increase of its output power is limited. The main way to improve the efficiency of linear power supplies is to reduce the transistor voltage drop. The above literatures have adopted different forms, some by introducing switching links, some by changing the form of input power supply, and some by using special topology to directly reduce the voltage drop.

The research on large-power linear converter is mainly a dual-supply complementary symmetrical power amplifier circuit, and that technology is quite mature. It is generally composed of a triode or field-effect transistor circuit, and is difficult to achieve high power output due to the circuit structure, P-type transistor parameters and low efficiency. To this end, researchers have proposed a bridge structure with complementary symmetrical parallel outputs composed of a large number of triodes [13,14]. The current output capability of the power amplifier is increased by increasing the number of triodes, but the size of the device becomes larger and the heat dissipation design is more complicated.

In order to pursue the characteristics of high-power output, conventional linear power devices such as BJT and MOSFET have been difficult to meet the demand. This paper intends to use Insulated Gate Bipolar Transistor (IGBT) as the power transistor. IGBT selection is not necessary, because on the one hand it can achieve linear operation, while on the other hand it can provide high voltage and large capacity [15,16]. Figure 1 shows the output characteristics of the IGBT. The area below the brown curve is the linear working workspace of the IGBT. When $v_{GE} < 9$ V, the saturation voltage drop v_{CE} is about 2.5 V. When the IGBT works in this nearby area, it not only retains the linear amplification characteristics, but also reduces the transistor consumption to the greatest extent. Based on this, the paper proposes a single-stage linear converter topology based on an all-N transistor, which achieves higher voltage and larger power output.

Ausgangskennlinienfeld IGBT-Wechselr. (typisch)
output characteristic IGBT-inverter (typical)

$I_C = f(V_{CE})$
 $T_{vj} = 150^\circ\text{C}$

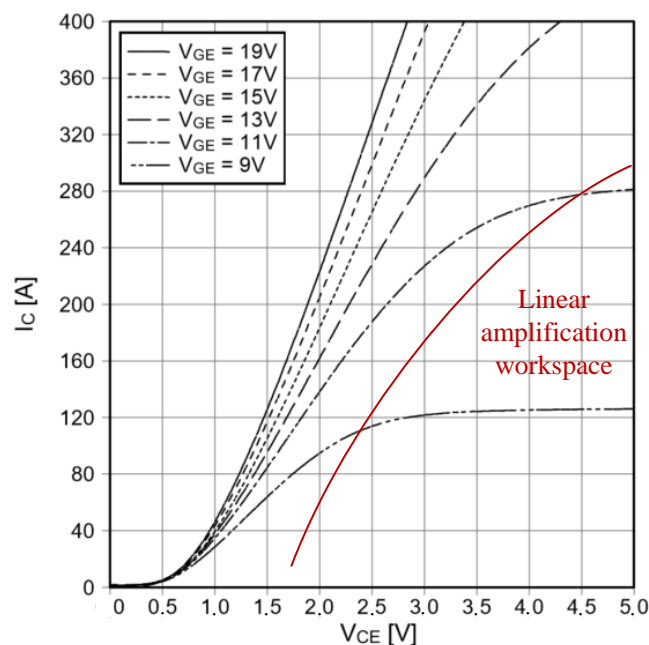


Figure 1. Output characteristic of the Insulated Gate Bipolar Transistor (IGBT).

This paper presents a high-efficiency and distortion-free converter based on piecewise-linearization with all N-type transistors (HDCPLN), which can be applied to a linear power supply. The linear voltage drop of the novel topology can also be reduced to the greatest extent without switching the converter part, and the power conversion efficiency can be improved. There is no need for the structure of multiple triodes in parallel, and a relatively simple structure can achieve greater power output. Based on a single-stage linear converter topology with all-N transistors, multiple power transistors are connected to different taps of the same transformer. By controlling the linear conduction angle of each power transistor in turn, the conduction transistor voltage drop is reduced, so that the converter can greatly improve the system efficiency. In addition, the third part of this paper proposes an optimization method for the design of the multi-winding transformer ratio at each stage from the perspective of the lowest sum of the transistor loss. Finally, the experimental results of a power supply prototype based on the principle of four-piece linear converter are given.

2. Single-Stage Linear Converter Based on All-N Transistor

2.1. Single-Stage Linear Power Converter Topology

A single-stage linear converter topology with all-N transistor is shown in Figure 2. When the control signal v_s is a standard sine, T_1 and T'_1 work complementarily and symmetrically. T_f and T'_f are used for energy feedback, and their control signals are the same as T_1 and T'_1 . The difference from the traditional Class-B power amplifier is that it is powered by the same DC power supply and is controlled by two voltage signals with a phase difference of 180° . The circuit uses the same type of power transistor and integrates the primary output through a double winding transformer, thereby the secondary side outputs a complete positive and negative half-cycle voltage waveform.

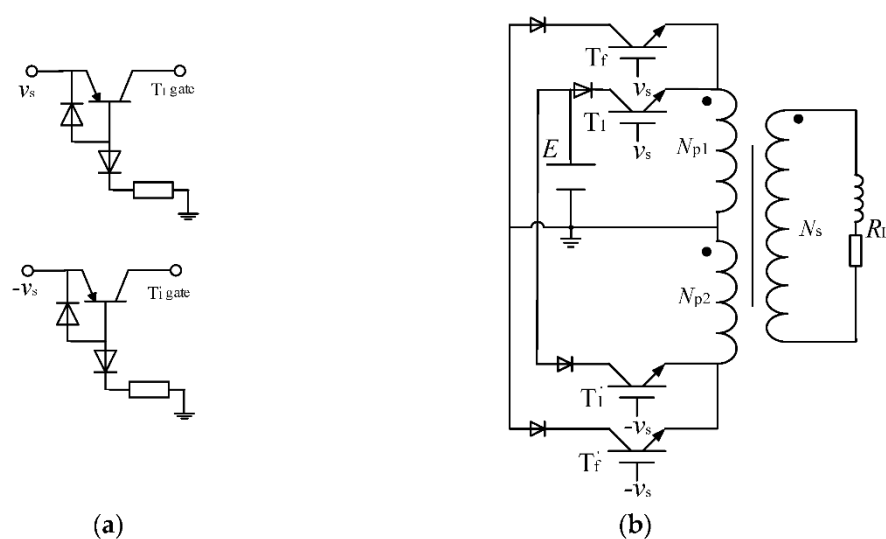


Figure 2. A single-stage linear converter topology with all-N transistor. (a) Control signal judgment circuit. (b) Main circuit topology.

The converter has four working phases in a cycle, and the conduction of the power transistor are shown in Table 1. Figure 3 shows the control signals and system output waveforms. The solid lines of v_s and $-v_s$ are actual T_1 and T_1' driving waveforms, and the dotted lines are actual T_f and T_f' driving waveforms.

Table 1. Conduction of transistor.

Load Voltage and Current Relationship	Linearly Conducting Transistor
Positive voltage and negative current (phase 1)	T_f'
Positive voltage and positive current (phase 2)	T_1
Negative voltage and positive current (phase 3)	T_f
Negative voltage and negative current (phase 4)	T_1'

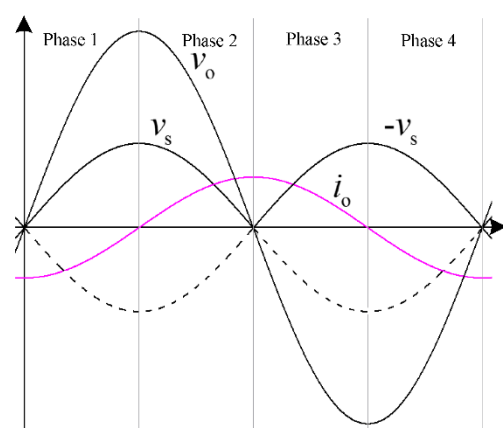


Figure 3. Input and output waveform diagram.

2.2. Working Principle

When the driving signals v_s , $-v_s$ are sine waves with equal amplitude and 180° phase difference, and the circuit works in a stable state, it is known from Table 1 that the output of the power converter has 4 working phases. The current path in each working stage is shown in Figure 4.

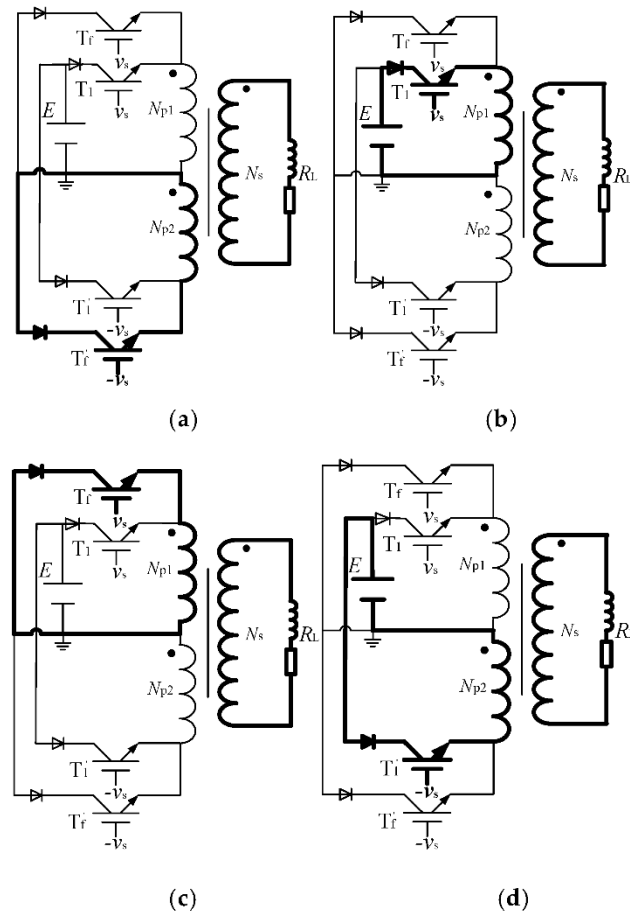


Figure 4. Decomposition of working process of power converter. (a) Positive voltage, negative current. (b) Positive voltage, positive current. (c) Negative voltage, positive current. (d) Negative voltage, negative current.

- (1) When the load voltage is positive and the current is negative, only the T_3' works, and the current path is shown in Figure 4a. Load voltage commutates, and T_1' without driving signal is in the off state. The input signal $-v_s$ is connected to the gate of T_3' , and T_3' is linearly conductive. T_1 and T_2 are cut off without a current path. The negative half-cycle waveform of $-v_s$ when the load current is negative is obtained without distortion on the primary winding N_{p2} . All the “.” are positive, and the load R_L bears positive voltage $(N_s/N_{p2}) \cdot -v_s$ through the transformer coupling.
- (2) When the load voltage is positive and the current is positive, only the T_1 works, and the current path is shown in Figure 4b. Load current commutes, and the driving signals v_s is greater than zero potential and connected to the gate of T_1 . T_2 is in the off state due to the opposite voltage and T_1 is linearly conductive. T_3' and T_4' are cut off without a current path. The positive half-cycle waveform of $-v_s$ when the load current is positive is obtained without distortion on the primary winding N_{p1} . All the “.” are positive, and the load R_L bears positive voltage $(N_s/N_{p1}) \cdot v_s$ through the transformer coupling.
- (3) When the load voltage is negative and the current is positive, only the T_2 works, and the current path is shown in Figure 4c. Load voltage commutes, and T_1 without driving signal is in the off state. The input signal v_s is connected to the gate of T_2 , and T_2 is linearly conductive. T_1 and T_3' are cut off without a current path. The negative half-cycle waveform of v_s when the load current is positive is obtained without distortion on the primary winding N_{p2} . All the “.” are negative, and the load R_L bears negative voltage $(N_s/N_{p1}) \cdot v_s$ through the transformer coupling.

- (4) When the load voltage is negative and the current is negative, only the T'_1 works, and the current path is shown in Figure 4d. Load current commutes, and the driving signals $-v_s$ is greater than zero potential and connected to the gate of T'_1 . T'_f is in the off state due to the opposite voltage and T'_1 is linearly conductive. T_1 and T_f are cut off without a current path. The positive half-cycle waveform of $-v_s$ when the load current is negative is obtained without distortion on the primary winding N_{p2} . All the “.” are positive, and the load R_L bears negative voltage $(N_s/N_{p2}) \cdot -v_s$ through the transformer coupling.

In order to obtain the expected output and avoid the occurrence of bias magnetism, generally take $N_{p1} = N_{p2} = N_p$, and the output voltage v_o

$$v_o = \frac{N_s}{N_p} \times v_s \quad (1)$$

The transformer is amplitude-second balance throughout the process, and the system reaches a stable state. However, due to the inherent shortcomings of push-pull linear power amplification, the ideal efficiency of A single-stage linear converter with all-N transistor is only 78.5% [17], which limits its application range.

3. HDCPLN Circuit Topology and Principle

3.1. Reasons for Improving HDCPLN Efficiency

Although the single-stage converter structure proposed above avoids the P-type transistor, it still belongs to the traditional class-B power amplifier in essence and the efficiency is still very low. Therefore, the idea of piecewise linearization is proposed in this paper. At each stage, different power transistors are controlled to be turned on linearly, so that the working transistor withstands very low voltage drop, which can greatly reduce losses.

On the basis of the structure proposed in the previous section, a multistage converter topology is proposed to achieve an all-N transistor high-efficiency converter. The two-stage circuit structure is taken as an example to explain the principle of HDCPLN efficiency improvement and the circuit working process.

The multistage signal sources are connected to the gates of the corresponding transistors via the on-off control circuit shown in Figure 5a according to the transformer ratio relationship. Figure 5b is the main circuit topology of the two-stage HDCPLN. On the basis of the single-stage linear converter structure, another input branch is added. Figure 5c shows the detailed control circuit block diagram. The multi-stage low-voltage signals are first amplified to the preset value, and then compared with each threshold potential. Then the signals are connected to the gates of the multi-stage power transistors to control its linear conduction. The low-voltage DC voltage is input through the collector, and the target waveform is finally output on the secondary side of the transformer.

As shown in Figure 5d, v_{s1} and v_{s2} are multistage driving signal sources, which input through the gates of T_1 , T_2 , and T_f respectively (the same can be seen, $-v_{s1}$, $-v_{s2}$ input through T'_1 , T'_2 and T'_f), where the dotted line indicates that the signal has not passed through the control circuit, the brown part is the actual driving waveform and the primary winding voltage is equal to the driving voltage. v_o is the final output voltage waveform of the secondary side of the transformer, i_o is the load current, and the DC voltage is E . It can be known that the commutation angles of the two-stage linear converter are respectively θ , $\pi - \theta$, $\pi + \theta$, and $2\pi - \theta$.

During the period from 0 to θ , the T_1 conducts linearly and the voltage drop is kept to a minimum among all transistors, and the other transistors are in a natural cutoff state. When the instantaneous voltage value of T_1 emitter reaches E , it automatically cut off. From θ to $\pi - \theta$, T_2 automatically turns on when it meets the optimal turn-on condition, and then iterates back and forth. The timing relationship of the linear turn-on is shown

in Table 2. T_1 and T_2 conduct linearly in steps within the positive half cycle of the output current. Similarly, T'_1 , T'_2 conduct linearly in steps within the negative half cycle.

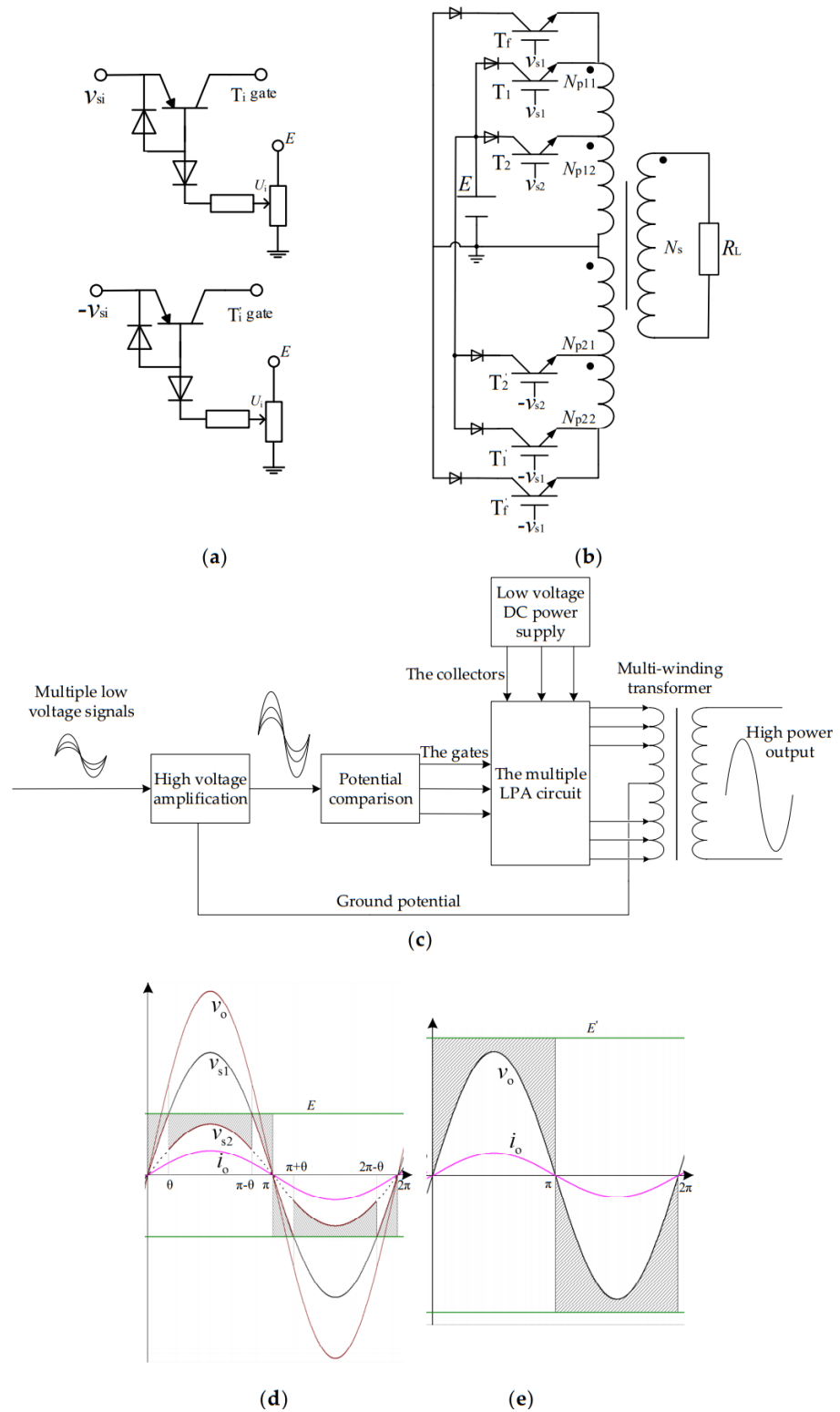


Figure 5. Operating principle of two-stage HDCPLN. (a) Control signal judgment circuit. (b) Main circuit topology. (c) Control structure diagram. (d) Work process. (e) Traditional amplifier work process.

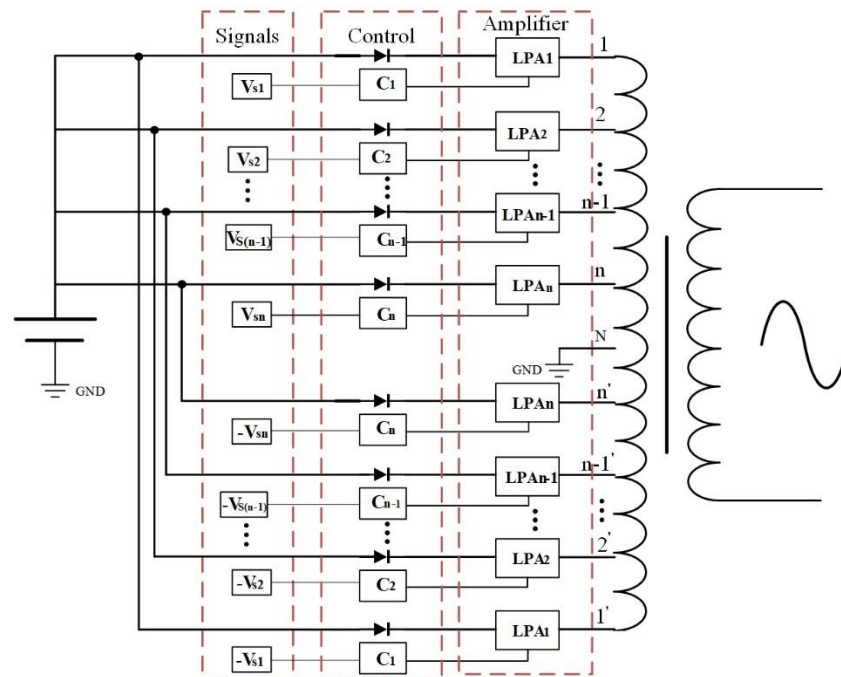
Table 2. Timing list of transistor turn-on linearly.

Linear Conduction Angle Interval	Transistor	Voltage Drop
$0 \sim \theta$	T_1	$E - v_{s1m} \sin \theta$
$\theta \sim \pi - \theta$	T_2	$E - v_{s2m} \sin \theta$
$\pi - \theta \sim \pi$	T_1	$E - v_{s1m} \sin \theta$
$\pi \sim \pi + \theta$	T_1'	$E - (-v_{s1m} \sin \theta)$
$\pi + \theta \sim 2\pi - \theta$	T_2'	$E - (-v_{s2m} \sin \theta)$
$2\pi - \theta \sim 2\pi$	T_1'	$E - (-v_{s1m} \sin \theta)$

Figure 5e is a schematic diagram of the traditional power amplifier operation. The shaded part is the transistor voltage drop, and the integral with the current is the transistor loss. In the positive and negative half cycles of the output current, the loss is borne by the same transistor respectively. HDCPLN always controls the voltage drop to a lower value, and the total power consumption is distributed to different transistors, which can improve the working efficiency to a certain extent.

3.2. HDCPLN Topology

The method of piecewise-linearization can improve the working efficiency as much as possible under the premise of transmitting the input waveform with high fidelity. The idea of this method is that multiple transistors are linearly conducted in a hierarchical manner, and only one transistor is on at any time and its voltage drop is minimal. Based on this principle, the topology of HDCPLN is shown in Figure 6. The n -stage HDCPLN is mainly composed of $2n$ -stage signal sources, piecewise-linearization control module, and n parallel single-stage linear converters based on all-N transistor and multi-winding transformer.

**Figure 6.** Circuit topology of HDCPLN.

The primary side of the multi-winding transformer has $2n$ windings with consistent directions, and they are connected end to end. Each connection point is used as the tap of the primary winding, and the center tap of the primary winding is used as the potential reference point of the power input on that side. The number of single-stage linear converters is the same as the number of taps of the multi-winding transformer. It can be known from the winding relationship that the taps $(1, 2, \dots, n)$ above the center tap and

the taps ($1', 2', \dots, n'$) are mutually different ends. During a cycle of output current, the transistor connected to the upper tap and the transistor connected to the lower tap are alternately conductive to form a push-pull circuit. The transistors connected to the taps with the same name end conduct linearly in stage in a half cycle of the output current, so as to ensure that the primary output voltage and the DC voltage E always maintain a small difference. By reducing the voltage drop during the linear conduction of the transistors at each stage, the loss during the energy transmission is reduced. The function of the piecewise-linearization control module is to change the point in time when the signal source at each stage is connected to the gate of the transistor.

Let the turns of the primary winding in circuit from stage 1 to stage n be $N_{p11}, N_{p12}, \dots, N_{p1i}, \dots, N_{p1n}; N_{p21}, N_{p22}, \dots, N_{p2i}, \dots, N_{p2n}$ ($N_{p1i} = N_{p2i} = N_{pi}$, $i = 1, 2, \dots, n$), the turns of the secondary winding is N_s , then the transformation ratio k_i is:

$$k_i = \frac{N_s}{N_{pi}} \quad (i = 1, 2, \dots, n) \quad (2)$$

The multistage sine wave signal sources are v_{si} ($i = 1, 2, \dots, n$). The multi-winding transformer superimposes the waveform of the output voltage on the primary side through different transformation ratios, thereby high voltage sine wave output from the secondary side of the transformer, v_{si} needs to satisfy the following equation:

$$v_{s1} \times k_1 = v_{s2} \times k_2 = \dots v_{si} \times k_i \dots = v_{sn} \times k_n \quad (3)$$

In the conduction control module, v_{si} needs to be greater than the comparison potential U_i so that it can be added to the gate of the corresponding IGBT. The setting of U_i directly determines the turn-on time of the IGBT in the number i converter. To ensure that each transistor can switch linearly on and off according to the timing, the expression of U_i is shown in Equation (4), where $U_1 = 0$ V.

$$U_i = \frac{k_{(i-1)}}{k_i} \times E \quad (i = 2, \dots, n) \quad (4)$$

The output voltage v_o is:

$$v_o = v_{si} \times k_i \quad (5)$$

According to Figure 5b, the commutation time of the HDCPLN can be obtained (ωt_j ($j = 1, 2, \dots, 4 \times (n-1)$)) as shown in Equations (6)–(8).

$$\omega t_j = \arcsin\left(\frac{V_{sim}}{E}\right) \quad (0 < \omega t_j < \frac{\pi}{2}; i = j = 1, 2, \dots, (n-1)) \quad (6)$$

$$\omega t_j = \pi - \omega t_{(n-1-j)} \quad (j = n, \dots, 2(n-1)) \quad (7)$$

$$\omega t_j = \pi + \omega t_{(j-2(n-1))} \quad (j = 2(n-1) + 1, \dots, 4(n-1)) \quad (8)$$

4. Efficiency Analysis and Optimization of HDCPLN

When HDCPLN is piecewise linearly conductive, the voltage drop and loss of the transistor can be further obtained in the case of obtaining the on-time period in each stage power converter. When the DC supply voltage E is constant, if the linear conduction angle of each transistor is infinitely small, the IGBT conduction voltage drop approaches the critical value of the linear working area. The consumption is almost negligible, then the efficiency of HDCPLN can be approximately equal to 1. The way for the linear conduction time to be infinitely small is to increase the number of stages to infinite, which is obviously impossible to achieve. It is only possible to use the HDCPLN structure with a limited number of stages to obtain higher efficiency. This section takes pure resistive load as an

example, calculates the working efficiency of HDCPLN, and optimizes the efficiency with the ratio k_i of the multi-winding transformer as a variable.

4.1. Efficiency Calculation of HDCPLN

If the time function of the target output voltage v_o is known to be $f(t)$ and the cycle is T , the relationship $f(t) = -f(t + 0.5 \times T)$ is satisfied, the load is R_L , and the DC supply voltage is E . The ratio of a multi-winding transformer can be expressed as:

$$k_i(t) = \begin{cases} k_1, & 0 < t \leq t_1 \\ \vdots \\ k_i, & t_{i-1} < t \leq t_i \\ \vdots \\ k_n, & t_{n-1} < t \leq t_n \end{cases} \quad (9)$$

Then the multistage driving signal sources v_{si} ($i = 1, 2, \dots, n$) are respectively:

$$v_{si} = \frac{f(t)}{k_i} \quad (10)$$

In addition, Equations (9) and (10) satisfy the following relationship:

$$\frac{f(t_i)}{k_i} = E \quad (11)$$

The current i of the number i transistor when it is turned on linearly is:

$$i_i = k_i i_o = k_i \times \frac{f(t)}{R_L} \quad (12)$$

In Equation (12), i_o represents the current on the load.

The total output power of HDCPLN is P_o .

$$P_o = \frac{1}{T} \int_0^T f(t) \times \frac{f(t)}{R_L} dt \quad (13)$$

Furthermore, the transistor losses P_{T_i} and $P_{T'_i}$ of each stage can be obtained.

$$P_{T_i} = \frac{1}{T} \int_0^T (E - f(t)) \times k_i \frac{f(t)}{R_L} dt \quad (14)$$

Since the conduction state of T'_i in the negative half cycle of the output current is exactly the same as T_i , P_{T_i} is equal to $P_{T'_i}$, then the total loss P_T is:

$$P_T = 2 \times \sum_{i=1}^n P_{T_i} \quad (15)$$

Then the theoretical working efficiency of HDCPLN can be found.

$$\eta = \frac{P_o}{P_T + P_o} \quad (16)$$

4.2. Ratio Optimal Design

The expected output voltage waveform is the standard sine of the amplitude V_{om} . Set the transformer ratio k_i as the variable. With the maximum efficiency of HDCPLN as the

goal, the optimal objective function under theoretical conditions can be obtained according to Equation (16).

$$\left\{ \begin{array}{l} \max \eta = \frac{P_o}{P_T + P_o} = \\ \frac{\frac{1}{2} \frac{V_{om}^2}{R_L}}{2 \times \sum_{i=1}^n \left(\frac{1}{\pi} \int_{\omega t_{(i-1)}}^{\omega t_i} \left(E - \frac{V_{om}}{k_i} \sin(\omega t) \right) \times k_i \frac{V_{om} \sin(\omega t)}{R_L} d(\omega t) \right) + \frac{1}{2} \frac{V_{om}^2}{R_L}} \\ \text{s.t. } \frac{V_{om}}{k_i} \sin(\omega t_i) = E \omega t_0 = 0 \quad \omega t_n = \frac{\pi}{2} \quad i \in [1, 2, \dots, n] \\ k_n E = V_{om} \\ k_{i-1} < k_i \end{array} \right. \quad (17)$$

In the Equation (17): the first and second constraints are equality constraints, and the upper and lower limits of the integral and the value of the number n ratio k_n of the transformer are given when solving the loss at each stage; The third is the ratio constraint between the primary and secondary windings at all stages.

Set the amplitude of the output voltage V_{om} equal to 310 V and the DC voltage E to 50 V. In the Matlab software environment, set different transformer winding numbers ($i = 2, 3, \dots$) in turn, and use genetic algorithm programming to solve the multivariate optimization problem of formula 17 with a single objective in consideration of constraints which include equal constraints and unequal constraints [18–20]. We can obtain the design strategy and corresponding optimal efficiency. As shown in Table 3, the efficiency of HDCPLN increases as the number of transformer ratios increases. The conventional design of multi-winding transformer ratio refers to that the voltages of the primary side tap are distributed at equal interval. Compared with the efficiency with the conventional transformer ratio design, the optimized results are significantly improved. The optimized three-segment power converter can reach the efficiency level of the conventional four-segment conversion. The efficiency of a four-stage HDCPLN using an optimized transformation ratio distribution can reach 91.49%, which is a 12.95% improvement over traditional class-B amplifiers.

Table 3. Transformer ratio design strategy and optimal efficiency.

Number of Ratios	Optimized Ratio Distribution	Efficiency with Conventional Design/%	Optimal Efficiency/%
1	6.20	78.54	78.54
2	6.20, 4.38	84.18	85.91
3	6.20, 5.10, 3.51	87.76	89.41
4	6.20, 5.44, 4.38, 2.99	89.69	91.49

In addition, if you want to further improve the working efficiency, you can increase the number of the windings and use more power converters in parallel. Analysis shows that variation of HDCPLN working efficiency with the number of transformation ratios is shown in Figure 7. It is necessary to make a trade-off between design cost and work efficiency. Although the efficiency increases with the increase in the number of power converters, the cost will undoubtedly increase as a result. This will also have some effects, such as the design cost and difficulty of multi-winding transformers, the cost of power transistors and the layout of radiators, the design of multiple independent control signals, and the internal layout design of the power supply. From Figure 7, it is easy to know that when the number of converters increases to a certain value, and the cost increases in proportion, but the efficiency increase is no longer obvious. When 8-stage converters are connected in parallel, a very high theoretical efficiency (95.24%) has been reached. After calculation analysis and comprehensive consideration, this is the best choice for large-scale applications of the novel linear power supply.

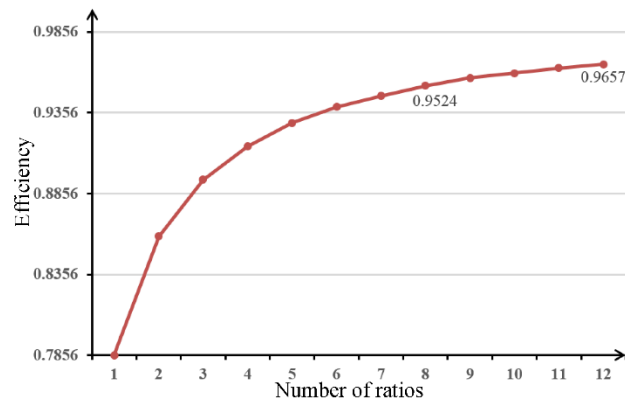


Figure 7. Variation of HDCPLN working efficiency with the number of transformation ratios.

5. Experimental Verification

In order to verify the correctness of theoretical research, a four-stage HDCPLN experimental prototype is designed and built in this paper. Figure 8 is a photo of the experimental platform, and the circuit parameters are shown in Table 4. Figure 9 shows the experimental results of the output voltage and current waveforms. The peak value of the load voltage is 310 V and the average power is 1 kW. Analysis of the data in Figure 9a shows that the total harmonic distortion coefficient (THD) of the load voltage and current are less than 1.5%, which achieves high-fidelity power amplification. In Figure 9b, i_i represents the current flowing through the center tap of the primary side of the multi-winding transformer. It is a continuous DC waveform, which is consistent with the theoretical analysis. Figure 9c shows the results obtained from the no-load test. i_f and i'_f represent the excitation current flowing through the T_f and T'_f branches of the transformer.

Figures 10 and 11 show the waveforms of the current and the output voltage of the primary side of the four-stage HDCPLN experimental prototype. i_{oi} and i'_{oi} represent the current flowing through the i -th power branch when the load current is positive and negative. v_{oi} and v'_{oi} respectively represent the output voltage of the i -th stage power converter on the primary side when the load current is positive and negative. It can be seen from Figure 10 that the output voltage of the primary side of each stage of the power converter satisfies the turns ratio relationship between the windings. It superimposes the waveforms output on the secondary side in sections to accurately output the expected load voltage.

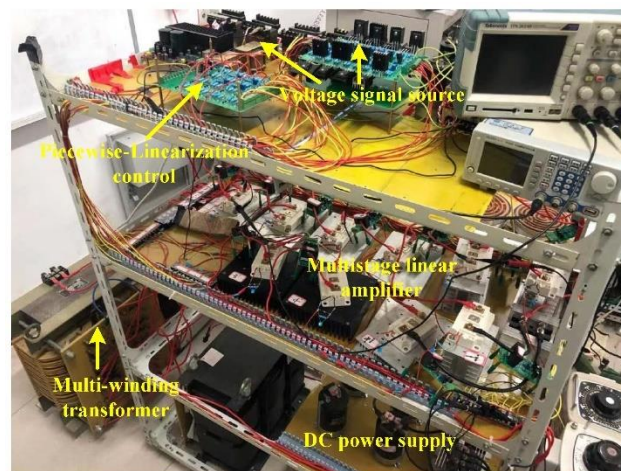
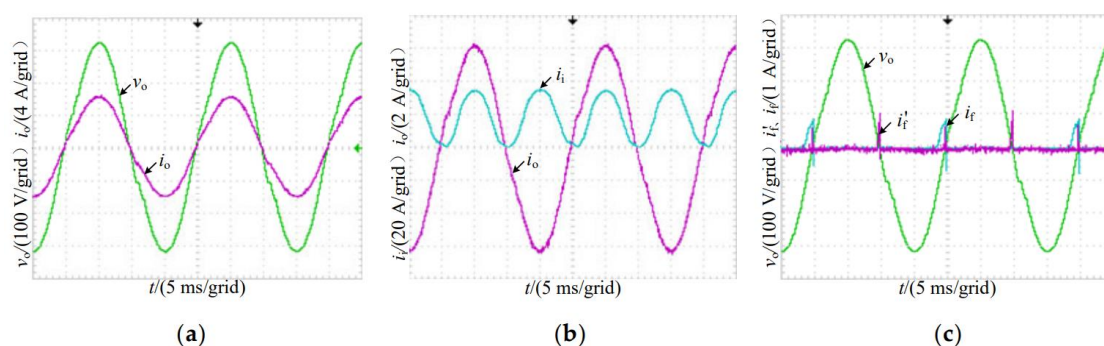
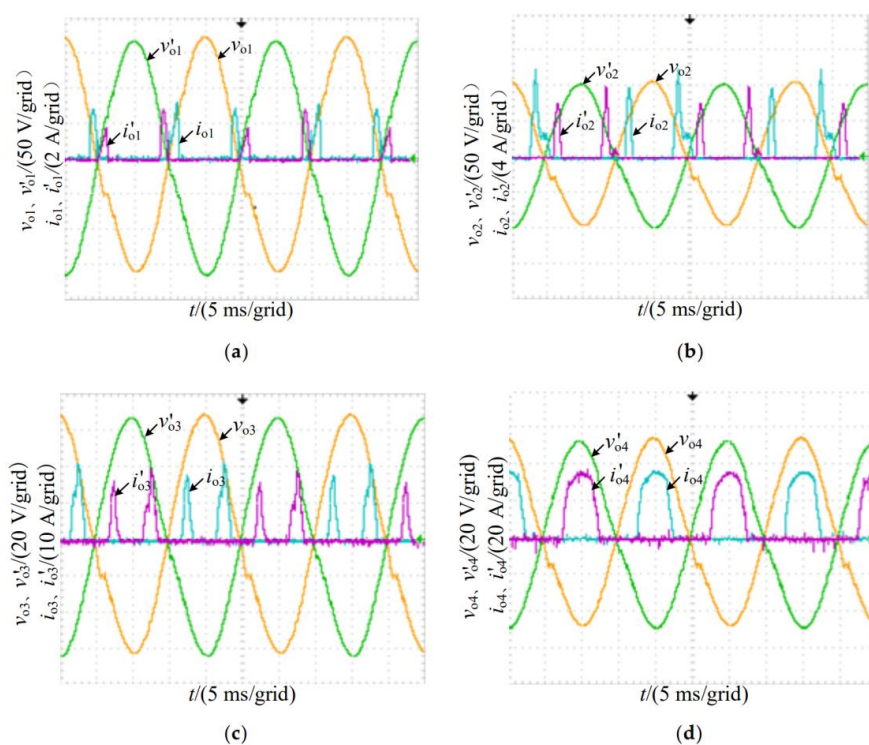


Figure 8. Experiment platform.

Table 4. The parameters of 4-stage HDCPLN.

Parameter	Value
First-stage ratio k_1	1.79
Second-stage ratio k_2	2.99
Third-stage ratio k_3	4.61
Fourth-stage ratio k_4	6.00
Load R_L/Ω	48.6
DC supply voltage E/V	53.2
First-stage drive signal v_{s1}/V	$\pm 178.6\sin(\omega t)$
Second-stage drive signal v_{s2}/V	$\pm 109.1\sin(\omega t)$
Third-stage drive signal v_{s3}/V	$\pm 72.2\sin(\omega t)$
Fourth-stage drive signal v_{s4}/V	$\pm 56.4\sin(\omega t)$
Transistor (IGBT) model	FF200R12KT4
Control triode PNP model	2SA1413

**Figure 9.** Output waveform of 4-stage HDCPLN. (a) Load voltage and current waveform. (b) Primary and secondary total current. (c) No-load voltage, excitation current.**Figure 10.** Voltage and current of each tap of transformer primary winding. (a) First stage voltage and current. (b) Second-stage voltage and current. (c) Third-stage voltage and current. (d) Fourth-stage voltage and current.

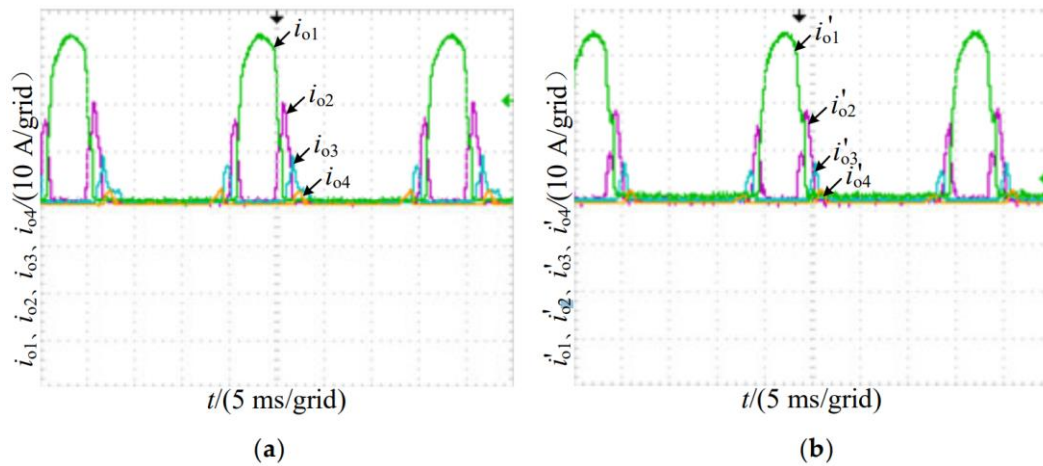


Figure 11. Current waveform of 4-stage HDCPLN. (a) Current on upper transistor at each stage. (b) Current on upper transistor at each stage.

Figure 11 shows the current waveform of the transistor in each period of time in the HDCPLN. It can be seen that the power transistors (IGBTs) at various stages can switch the on and off states according to the control strategy, and the multistage converter circuit is linearly conducted in sections according to the timing. However, there is an overlapping part in the power-on period of each stage. When two IGBTs are turned on linearly, there are two-stage power converters working in parallel. This parallel operation can ensure that the output waveform is not distorted during the switching time and reduce the current change rate of the transistor, but the disadvantage is that the loss is slightly increased.

The waveforms of the transistor voltage drops v_{cei} and v'_{cei} at all stages and the currents i_{oi} and i'_{oi} flowing through the transistor are shown in Figure 12. It can be seen that when each stage of IGBT is turned on linearly, its transistor voltage drop is in a low state, and the minimum value is close to the IGBT's saturation voltage drop. According to the waveform data in Figure 12, the transistor consumption of each stage can be obtained. The comparison result with the theoretical calculation is shown in Table 5. When calculating the theoretical value of the transistor loss, the default minimum value of the dynamic transistor voltage drop can reach zero. However, when the actual IGBT is turned on linearly, its turn-on voltage is greater than the saturation voltage drop. Therefore, the loss of each stage must be slightly larger than the theoretical data, and the experimental results meet the above rules. There are other losses with slight effects which cause difference between the working efficiency of the prototype and the theoretical value.

The current mainstream solutions for power supplies without partial discharge are linear power supplies, and so are the novel high-efficiency power supplies we proposed. After experimental analysis, the output waveform is almost pure sine wave without complex interference signals, which obviously meets the necessary conditions for no partial discharge. We have done a comparative analysis through series resonance experiments, and the output voltage is 200 kV. One of the experiments is a series resonance experiment on the proposed linear power supply. The second experiment is exactly the same as the first experiment, except that it uses the traditional mechanical contact voltage regulator to draw electricity directly from the grid, which is the control group. The two experimental processes are exactly the same, and the partial discharges during the two experimental processes are measured by a detector. In the two cases, the partial discharge measured by the detector is almost the same, one is 71.7 pC and the other is 71.8 pC, which shows that the linear power supply body does not cause additional partial discharge effects.

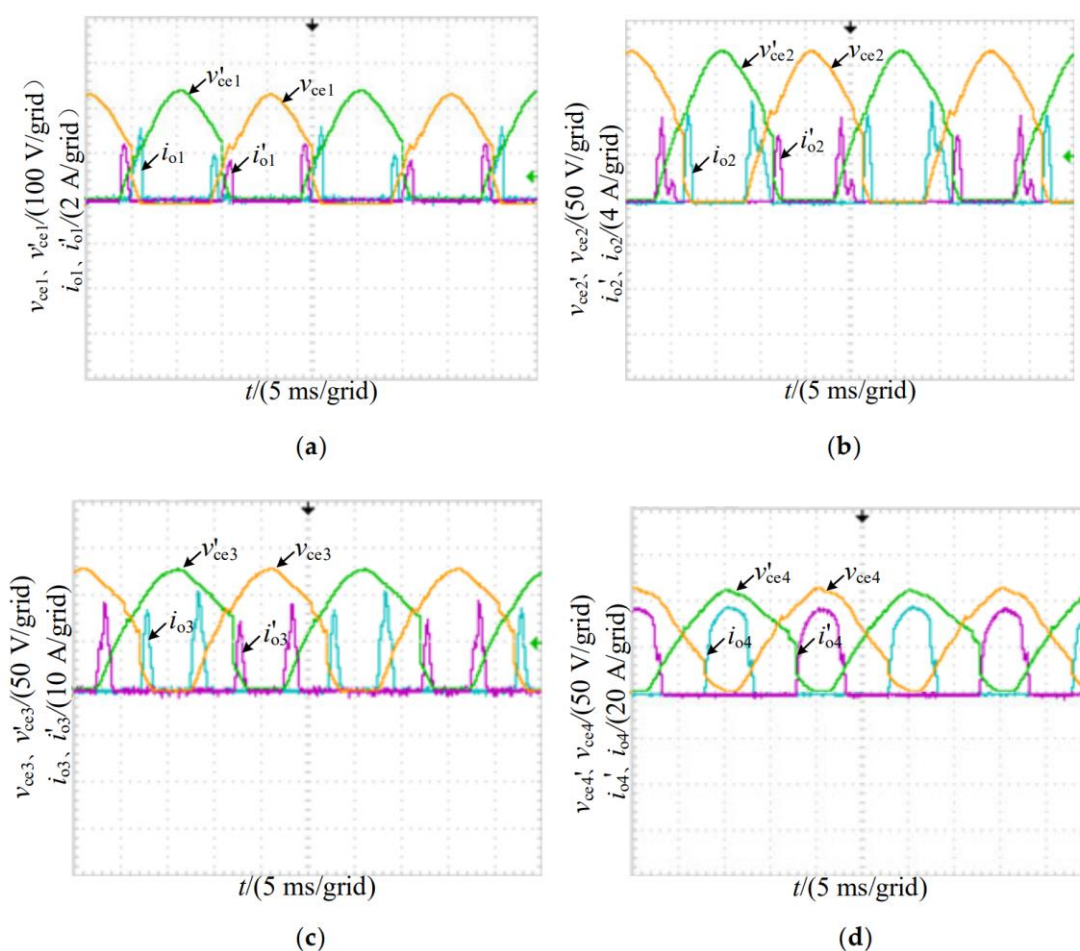


Figure 12. Voltage drop and current of power converter transistor at all stages. (a) First-stage transistor voltage drop, current. (b) Second-stage transistor voltage drop, current. (c) Third-stage transistor voltage drop, current. (d) Fourth-stage transistor voltage drop, current.

Table 5. Four-stage HDCPLN experiment and theoretical power loss comparison.

Category	Theoretical Calculation/W	Experimental Inquiry/W
First-stage loss	5.71	8.13
Second-stage loss	10.02	13.87
Third-stage loss	34.27	39.12
Fourth-stage loss	59.67	66.91
Total loss	109.66	128.03
Efficiency	90.12%	87.03%

6. Conclusions

The paper proposes a kind of high-efficiency linear power supply, whose power device works in the linear state. There is no pulse interference problem so that it can be used as the input part of high voltage test power supply. In application, the transformer in HDCPLN can replace the step-up transformer in the high-voltage test power supply, which can further reduce the volume of the test equipment. In addition, the novel power amplifier topology also solves the problem that traditional power conversion has low working efficiency and cannot achieve high power output due to the limitation of P-type transistor parameters. The converter input by a plurality of power amplifier modules connected in parallel, which are linearly conducted in a hierarchical manner. Only one transistor is on at any time and its voltage drop is minimal.

- (1) The topology based on above principle can achieve efficient power amplification.
- (2) The optimized multi-winding transformer ratio of the same number can further reduce transistor consumption, thereby improving efficiency.
- (3) The increase in efficiency increases with the number of segments.

In addition, the analysis of the experimental results found that there is a large difference between the transistor loss at each stage. A method of making it evenly distributed among the transistors with the lowest total consumption is worth further exploration.

Author Contributions: Methodology and Supervision, B.C., Y.C. and C.T.; Methodology, Y.Z. and G.X.; Writing—original draft, W.G.; Writing—review and editing, W.G. All authors have read and agreed to the published version of the manuscript.

Funding: This research received no external funding.

Data Availability Statement: The data presented in this study are available on request from the corresponding author.

Conflicts of Interest: The authors declare no conflict of interest.

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