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Review

A Recent Progress of Spintronics Devices for Integrated Circuit Applications

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Abstract: Nonvolatile (NV) memory is a key element for future high-performance and low-power microelectronics. Among the proposed NV memories, spintronics-based ones are particularly attractive for applications, owing to their low-voltage and high-speed operation capability in addition to their high-endurance feature. There are three types of spintronics devices with different writing schemes: spin-transfer torque (STT), spin-orbit torque (SOT), and electric field (*E*-field) effect on magnetic anisotropy. The NV memories using STT have been studied and developed most actively and are about to enter into the market by major semiconductor foundry companies. On the other hand, a development of the NV memories using other writing schemes are now underway. In this review article, first, the recent advancement of the spintronics device using STT and the NV memories using them are reviewed. Next, spintronics devices using the other two writing schemes (SOT and *E*-field) are briefly reviewed, including issues to be addressed for the NV memories application.

Keywords: integrated circuits; nonvolatile memory; spintronics; magnetic tunnel junction; spin-transfer torque; spin-orbit torque; electric field effect

1. Introduction

Large-scale integrated (LSI) circuits are a vital constituent for current information and communication technology equipment. Progress in the LSIs have been led by development of complementary metal-oxide-semiconductor (CMOS) technology relying on Moore's scaling law. However, the development of CMOS is now interrupted mainly by two serious issues. One is an increase of standby power and the other is Input/Output (I/O) bottleneck due to interconnection delay. The former issue originates from the volatile nature of the current memories in the LSIs in which the standby power becomes larger due to an increase of leakage current as the CMOS technology node is advancing. The latter issue is attributed to an elongation of global wire length due to an increase of the number of integrated elements in the LSIs. To address those issues, nonvolatile (NV) memories have been attracting a great deal of attention. Among the proposed NV memories, spintronics-based ones (magnetoresistive random access memories (MRAM)) are very attractive owing to their high-speed and low-voltage operation capability and high endurance, which are required for working memory usage [1–3]. In addition to those advantages, spintronics-based memories can be implemented in back-end-of-line (BEOL), a feature which enables one to address the I/O bottleneck as global wire length between memory and logic module can be reduced.

The proposed three writing schemes are spin-transfer torque (STT), spin-orbit torque (SOT), and electric field (*E*-field) effect on magnetic anisotropy or voltage-controlled (VC) magnetic anisotropy. The memory cell for STT-MRAM and VC-MRAM is a two-terminal structure and that for SOT-MRAM is a three-terminal structure as shown in Figure 1a,b, respectively. In the STT-MRAM, the memory cell with minimum cell size is composed of one magnetic tunnel junction (MTJ) and one selective MOS transistor (1T-1MTJ) as shown in Figure 1a. Note that there are many variations of the memory cell depending on applications. For writing, the current is applied to the MTJ from the transistor, which exerts a spin-transfer torque on the magnetization in the free layer of the MTJ [4,5]. In SOT-MRAM, a current is applied to the channel layer from the transistor located at the side of the channel layer underneath the MTJ and a torque is exerted on the magnetization in the free layer of the MTJ through spin Hall effect and/or Rashba–Edelstine effect [6–8]. For VC-MRAM, *E*-field (voltage) is applied to the free layer in the MTJ, which reduces or increases perpendicular magnetic anisotropy. The easy axis of magnetization transits from out-of-plane to in-plane or vice versa at a certain *E*-field. Above the *E*-field, the magnetization can be switched through precessional motion of magnetization along in-plane (out-of-plane) magnetic field.

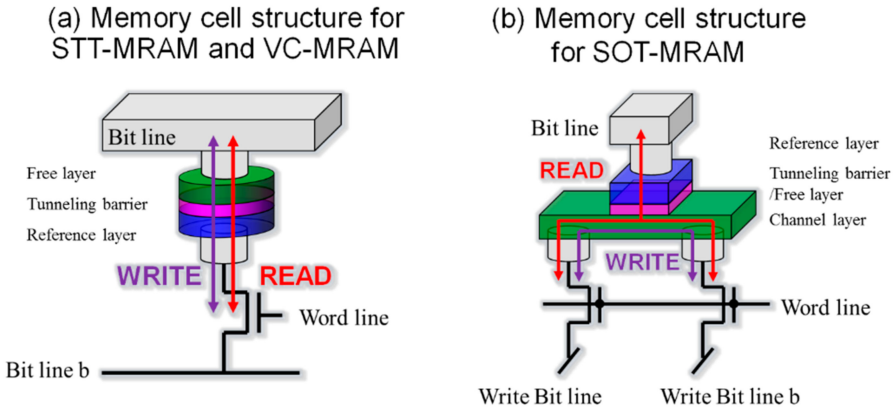


Figure 1. (**a**) Memory cell structure for STT-MRAM and VC-MRAM. The memory cell structure consisting of one magnetic tunnel junction (MTJ) and one transistor yields in minimum cell size. There are many variations for the memory cell structure depending on the applications, in particular, for the STT-MRAM. (**b**) Memory cell structure for SOT-MRAM, where one MTJ and two transistors are required at least.

There are three types of MRAM where different writing schemes are employed. In all the MRAMs, a magnetic tunnel junction is integrated as storage element. For reading operation, tunnel magnetoresistance effect is utilized, by which two distinct resistance levels can be obtained depending on magnetization configuration for free and reference layers, parallel and antiparallel states.

The STT-MRAM is the most studied and developed MRAM and is about to enter the market as major semiconductor foundries have announced the starting of risk of mass production in 2018. Although the STT-MRAM is about to enter the market, the other MRAMs have been also intensively studied [9]. This is because those two MRAMs, in principle, have higher potential in offering high-speed writing operation compared with the STT-MRAM.

In this review, first, we show benchmarking results for the STT-MRAM, SOT-MRAM, and *E*-field MRAM from the viewpoint of LSI applications (Section 2). In Section 3, we review the recent progress of STT-MRAMs mainly based on our efforts (Section 3.1) and briefly review the progress of SOT-MRAM and *E*-field MRAM including the issues to be addressed for NV memory applications (Sections 3.2 and 3.3).

2. Benchmarking Results for STT-MRAM, SOT-MRAM, and *E*-Field MRAM

In this section, we show benchmarking results for the STT-MRAM, SOT-MRAM, and *E*-field MRAM compared with eFlash and SRAM as CMOS-based memories. Table 1 shows the benchmarking

results [2,10–13]. Thanks to the simple memory cell structure for the STT-MRAM, the STT-MRAM has been developed for replacement of SRAM and eFlash. For SRAM replacement usage, the STT-MRAM enables one to reduce cell size and nonvolatility function, resulting in drastic reduction of standby power, without significant degradation of high-speed operation capability and endurance. For eFlash replacement, the STT-MRAM gives us lower write voltage, faster write speed, and better endurance without sacrificing nonvolatility.

SOT-MRAM and VC-MRAM are very attractive for SRAM replacement usage as, in principle, they have higher potential in offering high-speed writing capability than the STT-MRAM. However, there are a few issues in SOT-MRAM and VC-MRAM to be addressed for NV memory applications, which will be discussed later.

Table 1. Benchmarking results of STT-MAM, SOT-MRAM, and VC-MRAM as NV memories using spintronics devices compared with SRAM and eFlash as CMOS-based memories. The *F* denotes feature size of CMOS. Memory cell size is defined by *F*.

	SRAM	STT-MRAM for SRAM	eFlash	STT-MRAM for eFlash	SOT-MRAM	VC-MRAM
Cell size	160–200 F^2	70–100 F^2	40 F^2	50–60 F^2	160 F^2	50–60 F^2
Operation voltage (V)	0.6–1.2	0.6	≥10	0.6	0.6	2.2
Write current (A)	10^{-5}	10^{-5}	10^{-5}	10^{-5}	10^{-4}	10^{-5}
R/W time (ns)	≤2/≤2	5/10	10/20,000	25/200	5/≤2	10/≤2
Retention	Volatile	1 month	>20 years	15 years	≤10 years	1 month
Endurance (cycles)	10^{16}	10^{14}	10^5	10^8	10^{14}	-

3. Review for Recent Progress of STT-MRAM, SOT-MRAM, and *E*-Field MRAM

3.1. Recent Progress of STT-MRAMs for NV Memory Applications

STT-MRAMs are attracting much attention owing to their high potential for offering electronics with both low-power consumption and high performance. Recently, many researchers and fab companies have focused on STT-MRAM using CoFeB/MgO-based p-MTJ because STT-MRAM with the p-MTJ is the most promising emerging memory in terms of scalability, high write endurances, high operation speed, and CMOS BEOL process affinity. In this section, we review the material design concept in the advanced CoFeB/MgO p-MTJs with high thermal tolerance and high thermal stability. We also review the advanced patterning method of MTJ for high-density STT-MRAM.

3.1.1. MTJ Design with High Thermal Tolerance for STT-MRAM with CMOS BEOL Process Compatibility

In the MTJs with perpendicular easy axis (p-MTJs) for STT-MRAM, a high tunnel magnetoresistance ratio, low switching current, and high thermal stability are required at the same time. In addition, a large switching field compared to the free layer and a small stray field are required in the reference layer. For integration of STT-MRAM using standard CMOS BEOL process, those properties need to be maintained after annealing at temperature of 400 °C. In order to realize high performance p-MTJ using CoFeB/MgO system showing high tunnel magnetoresistance, a relatively high thermal stability factor, and low switching current [14], Sato et al. proposed MgO/CoFeB/Ta/CoFeB/MgO free layer structure (double CoFeB/MgO interface p-MTJ, d-MTJ) which has larger thermal stability factor than that of MgO/CoFeB/Ta free layer structure (single CoFeB/MgO interface structure, s-MTJ) while maintaining low write current [15–17]. We have demonstrated that our developed d-MTJ with a synthetic ferrimagnetic (SyF) reference layer has the capability to withstand annealing at 400 °C in the MTJ diameter down to 10 nm φ [18]. This structure has become de facto standard of p-MTJ.

In order to further improve the p-MTJ performance, one needs to understand the dominant factors in determining thermal tolerance of the p-MTJs. Here, we review our recent progress in the advanced p-MTJs for STT-MRAM. In particular, we describe the material design knowledge of (1) high thermal

tolerance by controlling boron composition of CoFeB free layer, (2) damage suppression by sputtering conditions, and (3) thermal tolerance of the reference layer by high-temperature annealing [19,20].

(1) High thermal tolerance by controlling boron composition of CoFeB free layer

To obtain high thermal tolerance, one needs to control diffusion of boron from CoFeB to the adjacent layer because boron concentration plays a crucial role in realizing perpendicular easy axis [18–33]. As shown in Figure 2a,c, all the s-MTJs showed an increase of TMR ratio up to a specific temperature, above which the TMR ratio degraded. The annealing temperature (T_a) where the maximum TMR ratio is observed in the s-MTJs increases with increasing x up to 35at%B. In s-MTJ with x = 40at%B, the TMR ratio drastically decreases at T_a = 400 °C, which may be related to the formation of a weak (001) texture in MgO/CoFeB stack with high B concentration [30]. On the other hand, as shown in Figure 2b,d, the TMR ratio of d-MTJs increases monotonically as T_a increases up to 400 °C. In d-MTJ with x = 25at%B, TMR ratio reaches to 131%. As x increases, higher T_a is required in order to get a higher TMR ratio. As seen above, the temperature dependence of TMR ratio in d-MTJ is significantly different from that in s-MTJ [29].

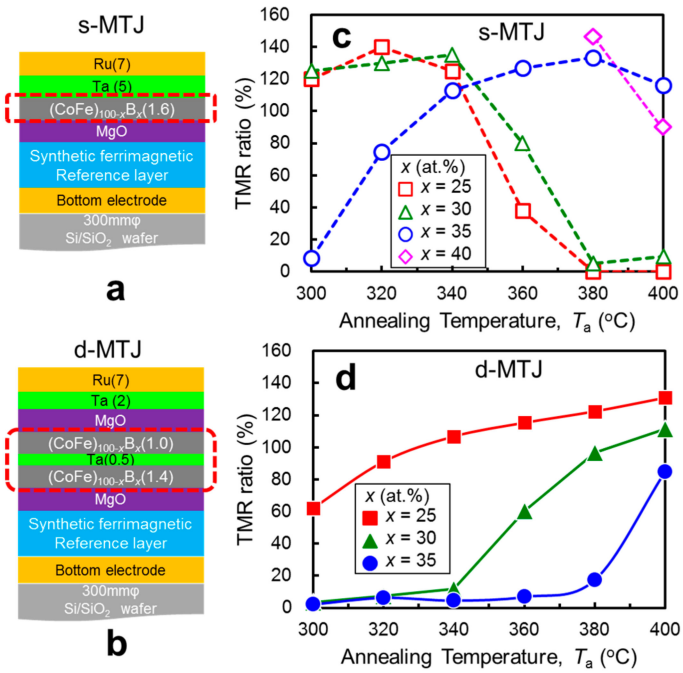


Figure 2. Schematic for single CoFeB–MgO interface MTJ (s-MTJ) (**a**) and double CoFeB–MgO interface MTJ (d-MTJ) (**b**) stack structures. Annealing temperature T_a dependence of tunnel magnetoresistance (TMR) ratio for s-MTJ (**c**) and d-MTJ (**d**) with B content of 25–40at. % in CoFeB free layer.

To understand the T_a dependence of TMR ratio for s-MTJ and d-MTJ shown in Figure 2, we evaluated effective anisotropy energy density $K_{eff}t^*$ from the areal difference between the out-of-plane and in-plane m–H curves as shown in Figure 3a. t^* is the effective magnetic layer thickness, which is obtained by subtracting the magnetically dead layer thicknesses from the nominal free layer thickness as shown in Figure 3b. Figure 4 shows typical $K_{eff}t^*$-t^* plots for the s-MTJ and the d-MTJ with x = 25, 30, and 35at.%B after annealing at T_a = 400 °C. Positive and negative values of $K_{eff}t^*$ means in-plane and perpendicular magnetic anisotropy, respectively. In both of s-MTJ and d-MTJ, $K_{eff}t^*$ tends to increase as t^* decreases. t^* indicating the positive value of $K_{eff}t^*$ becomes thick in the d-MTJ type compared with s-MTJ. The maximum $K_{eff}t^*$ for s-MTJ and d-MTJ annealed at 400 °C is obtained by x = 35 and x = 25, respectively. Thus, high TMR ratios are obtained in s-MTJ and d-MTJ because high perpendicular magnetic anisotropy is realized even in high-temperature annealing at 400 °C.

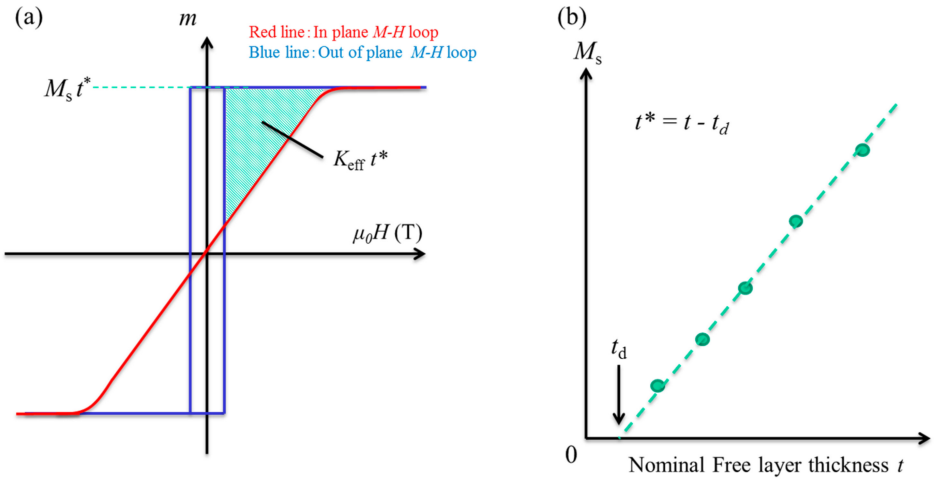


Figure 3. Magnetic moment per unit area versus in-plane and out-of-plane magnetic field (**a**) and saturation magnetization *M*s versus nominal free layer thickness *t* (**b**).

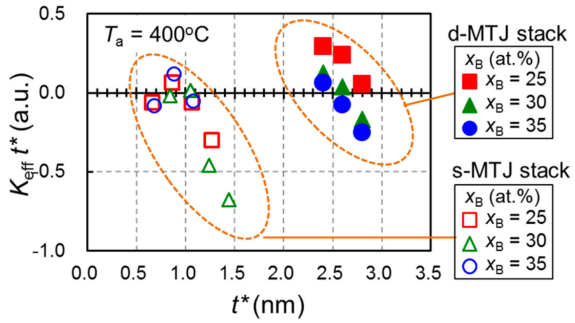


Figure 4. $K_{eff}t^*$ as a function of t^* for s-MTJ and d-MTJ with B content of 25–35at.% annealed at 400 °C.

In the CoFeB/MgO-based p-MTJ system, effective anisotropy energy density $K_{eff}t^*$ is determined by competition between interfacial anisotropy K_i and shape anisotropy ($-M_s^2/2\mu_0$ where M_S is saturation magnetization), as expressed in Equation (1).

$$K_{eff}t* = K_i - \left[(N_z - N_x)\frac{M_s^2}{2\mu_0} + K_b\right]t* \quad (1)$$

where K_i is interfacial anisotropy energy, N_z and N_x are demagnetization coefficients, K_b is bulk anisotropy energy. In Equation (1), the second term is shape anisotropy, proportional to M_s square. K_b is negligibly small in the system. Figure 5 shows B content dependence of saturation magnetization M_s evaluated from *M*–*H* curves for the s-MTJ and d-MTJ annealed at 400 °C. M_s of d-MTJ is suppressed to about half of that of s-MTJ.

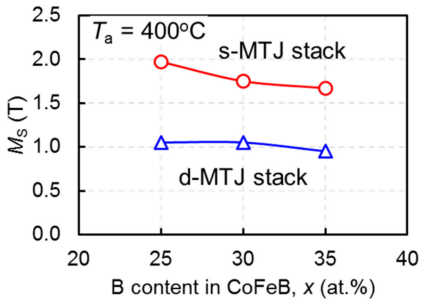


Figure 5. B content dependence of saturation magnetization M_s for s-MTJ and d-MTJ with B content of 25–35at% annealed at 400 °C.

From this measured M_s and Equation (1), in the s-MTJ, shape anisotropy is the dominant factor that determines perpendicular anisotropy because of larger M_s (larger shape anisotropy). On the other hand, in the d-MTJ, K_i is the dominant factor because of smaller M_s and larger K_i (about double that of s-MTJ thanks to double CoFeB/MgO interface). In order to improve perpendicular anisotropy, larger K_i and smaller M_s are desirable. However, with increasing B content in CoFeB, both M_s of CoFeB and K_i decreases [21].

The large difference in M_s between s-MTJ and d-MTJ is due to the difference in B diffusion state. As shown in Figure 6, the boron in the s-MTJ adsorbs into the Ta-capping layer. On the other hand, boron in the d-MTJ is located around the Ta insertion layer. The Ta insertion layer acts as a boron absorption layer. Also, the MgO-capping layer blocks boron diffusion from the CoFeB to the Ta-capping layer. As a result, in the d-MTJ, a large amount of boron remains in the CoFeB layer. This results in lower M_s in the free layer of d-MTJ than in that of s-MTJ. These results indicate that boron composition of the CoFeB layer after annealing is a critical factor to realize thermal tolerance for annealing at a temperature of 400 °C, which is a standard requirement for the integration with CMOS in back-end-of line process.

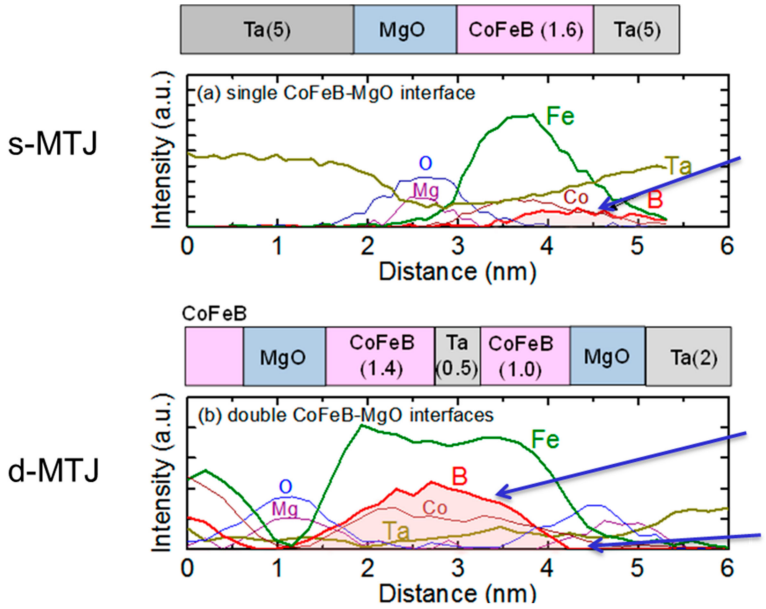


Figure 6. EELS line profiles of B, Fe, Co, Ta, Mg, and O elements for s-MTJ and d-MTJ annealed at 400 °C.

(2) Damage suppression by sputtering conditions

In the double CoFeB–MgO interface structure, a thin metal layer such as Ta, W, or Mo was inserted to absorb boron from the CoFeB layers (MgO/CoFeB/insertion layer/CoFeB/MgO) for high tunnel magnetoresistance (TMR) ratio and perpendicular anisotropy [15,16,29,33–44]. First, Ta was used as insertion material because Ta has a bcc crystal structure and is a good boron absorber, as mentioned above. Recently, tungsten (W) was also used as insertion material because W has a higher melting point, resulting in higher thermal stability [39,44].

It was reported that a degree of damage caused by the deposition of heavy metals (Ta or W) on the layer underneath them is generally dependent on sputtering gas species [45–47]. In fact, we have revealed that perpendicular anisotropy of the CoFeB–MgO system enhances by using Kr instead of Ar for Ta-capping layer deposition [48]. Because it is important to suppress damage during film deposition for realization of high-performance p-MTJs, it is required to engineer a deposition process for insertion layer resulting in high TMR ratio and high perpendicular anisotropy. Therefore, we evaluated the impact of sputtering condition of W layer in the free layer and the reference layer [49,50]. By using Kr or Xe gas instead of Ar gas for W deposition, TMR ratio and perpendicular anisotropy significantly

improved. Energy dispersive X-ray microscope analysis revealed that interdiffusion in the MTJ between, underneath, and on the W was suppressed by using Kr or Xe gas. High-energy recoiled Ar from W sputtering target bombarded the surface of W and underneath the layer. Penetrated Ar may cause large stress and defects in the film, resulting in larger interdiffusion in the film. In fact, Ar was observed in W(Ar) while Kr and Xe were not in W(Kr) and W(Xe) [49].

(3) Thermal tolerance of the reference layer by high-temperature annealing

As mentioned in the previous section, we have demonstrated the thermal tolerance against 400 °C annealing in CoFeB–MgO-based p-MTJs with the Co/Pt multilayer-based SyF reference layer [17].

However, we simultaneously observed a variation of shift field H_s caused by an uncompensated stray magnetic field from the reference layer as annealing temperature T_a increased from 350 °C to 400 °C [18], resulting in asymmetry of thermal stability factor Δ between parallel (P) and antiparallel (AP) states, as shown in Figure 7 [18].

To clarify the origin of the variation of H_s, we investigated T_a dependence of spontaneous magnetic moment per unit area m_s of each layer in reference layer (Figure 8) and a variation of composition depth profile after annealing at 400 °C.

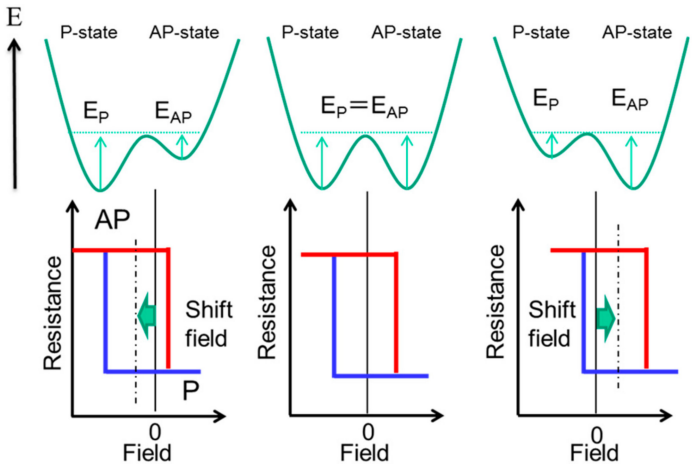


Figure 7. Schematic for potential curve at parallel (P) and antiparallel (AP) state (a) and resistance versus magnetic field curve. Shift field H_s is defined as center of hysteresis curve.

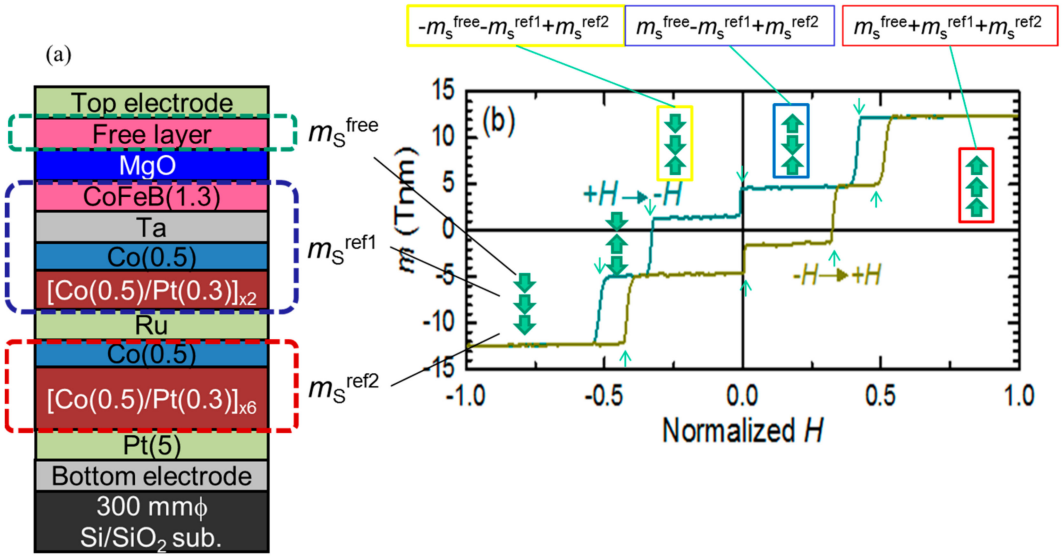


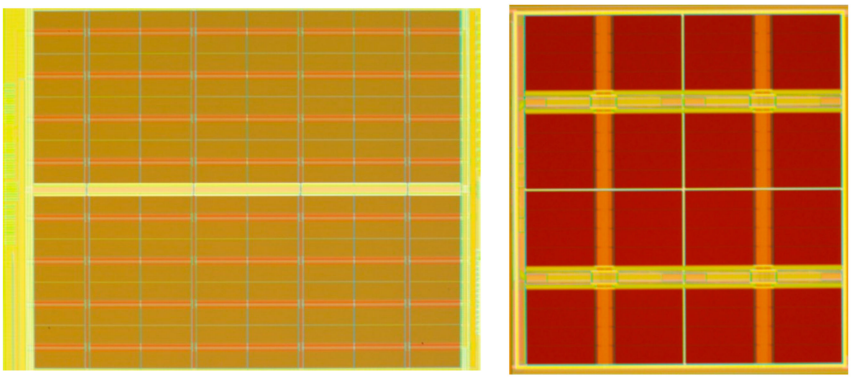
Figure 8. (**a**) Stack structure of a stack for magnetic tunnel junction (MTJ). (**b**) Magnetic moment per unit area versus magnetic field curve of the stack MTJ. Arrows show a direction of magnetic moment for free layer m_s^{free}, top part of reference layer m_s^{ref1}, and bottom part of reference layer m_s^{ref2}.

We investigated properties of the p-MTJ at elevated annealing temperature T_a from 350 °C to 400 °C. The MTJs annealed at 400 °C show larger H_s (AP state becomes more stable) compared to those annealed at 350 °C. The variation of H_s resulted because the m_s of top Co/Pt multilayer with CoFeB insertion layer decreased and the m_s of bottom Co/Pt multilayer decreased as T_a increased from 350 °C to 400 °C. EDX line analysis revealed that Fe in the CoFeB layer underneath the MgO layer (in the reference layer) diffuses into Co/Pt multilayers in the SyF reference layer via annealing at T_a = 400 °C, which could cause the variation of m_s in the SyF reference layer. The results indicate that suppression of Fe diffusion in the CoFeB layer in the reference layer is important to achieve more robust MTJs against annealing.

In order to overcome this issue, we have developed surface modification process (SMT) on the Pt buffer layer by ion irradiation [20]. SMT improves crystallinity of the Co/Pt multilayer even after 400 °C annealing, resulting in high perpendicular anisotropy of Co/Pt and suppression of Fe diffusion in the CoFeB reference layer [20].

3.1.2. Recent Progress of STT-MRAMs

As mentioned earlier, STT-MRAMs are attracting much attention owing to their high potential to offer electronics with both low-power consumption and high performance for IoT and AI applications. Recently, many researchers and fab companies have focused on STT-MRAM using CoFeB/MgO-based p-MTJ because STT-MRAM with p-MTJ is the most promising emerging memory in terms of scalability, high write endurances, high operation speed, and CMOS back-end-of-line process compatibility. We have successfully developed prototype high-speed operation 6T-2MTJ STT-MRAM, 1T-1MTJ STT-MRAM with on-via MTJ (see Figure 9), and so on [51,52]. A Gbit-class, large-capacity MRAM was also published by SK Hynix & Toshiba [53]. Three megafab companies have announced that the risk of mass production of the STT-MRAM will be started in 2018, where the STT-MRAM will be in place of either eFlash or SRAM [54–56]. For the scalability, the patterning method of MTJ has to change from ion beam etching (IBE) to reactive ion etching (RIE). However, IBE is still used because RIE of magnetic material is not easy. In order to apply RIE to MTJ etching, new etching chemistry and methods are needed. We have developed low-damage and short-failure-free RIE technologies for STT-MRAM [57]. By replacing MTJ etching technology from IBE to RIE, it can be expected to realize high density STT-MRAM for DRAM substitution.



(**a**) (**b**)

Figure 9. Microphotograph of 1Mb 6T2MTJ STT-MRAM (**a**) and 2Mb 1T1MTJ STT-MRAM (**b**).

3.2. Progress of SOT-MRAM and Future Issues for NV Memory Applications

As shown in Figure 1b, in the memory cell of SOT-MRAM, the MTJ is fabricated on the channel layer, which is made of heavy metal, such as Ta, W, Hf, and so on, in order to have higher spin-orbit torque [6,7,58–65]. There are three types of SOT devices (called type x, type y, and type z) where the relationship between magnetization easy axis direction and channel current direction differs [66]. Figure 10 shows a schematic diagram of the three types of SOT devices. In each figure,

the magnetization trajectory during switching is also shown. Among the three types of devices, magnetic-field-free switching can be achieved in only the y-type, while in the other two devices, one needs to apply either in-plane or out-of-plane field for z-type and x-type devices, respectively. However, the y-type device shows similar switching trajectory to that in the conventional STT device, resulting in a steep increase in switching current as the write pulse width reduces down to ns regime. Therefore, from the viewpoint of high-speed writing operation, the x-type and z-type devices are much preferable. In order to eliminate external magnetic field for z-type, exchange bias field is employed by putting antiferromagnetic material underneath the free layer, which can play a role as a channel layer generating SOT [62]. The field-free switching has been demonstrated in Hall-bar devices with z-type devices, but not in the actual SOT device for NV memory. Toward the NV memory applications, the field-free switching needs to be demonstrated with thermal tolerance against annealing at 400 °C in the actual SOT device for NV memory, which is a standard requirement for CMOS BEOL, as mentioned in the former section. For the x-type device, the field-free switching has also been demonstrated by tilting easy axis angle from x-axis in the actual SOT device for memory applications [67], thus we focus on how it can be done in this review paper.

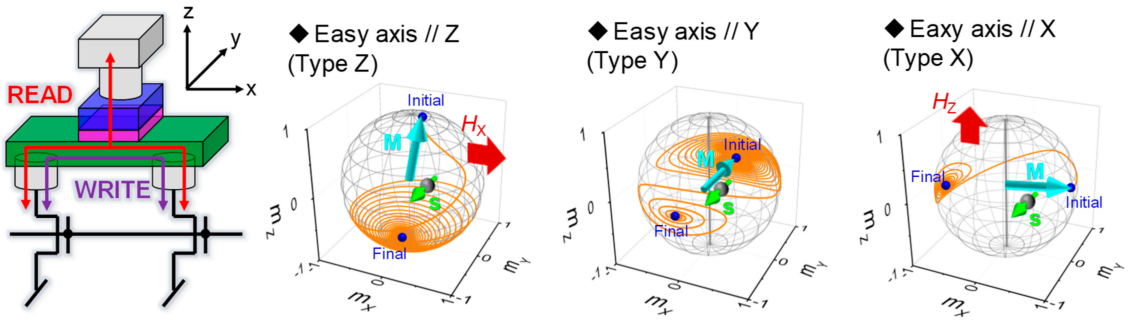


Figure 10. Schematic diagrams of three types of SOT devices in which magnetization trajectory during switching is also shown as inset.

Figure 11a shows the SOT device structure demonstrating field-free switching. In the x-type device, the direction of spin generated by the channel layer is orthogonal to the easy axis of magnetization in the free layer, therefore, in order to switch it, one needs to break the symmetry. One way to break the symmetry is applying the out-of-plane field, which is not suitable for LSIs. The other way is canting the easy axis of magnetization from the x-axis, by which the direction of spin generated by the channel layer is not orthogonal to the easy axis of magnetization, resulting in the symmetry breaking. Figure 11b shows resistance versus current density curve of the SOT device.

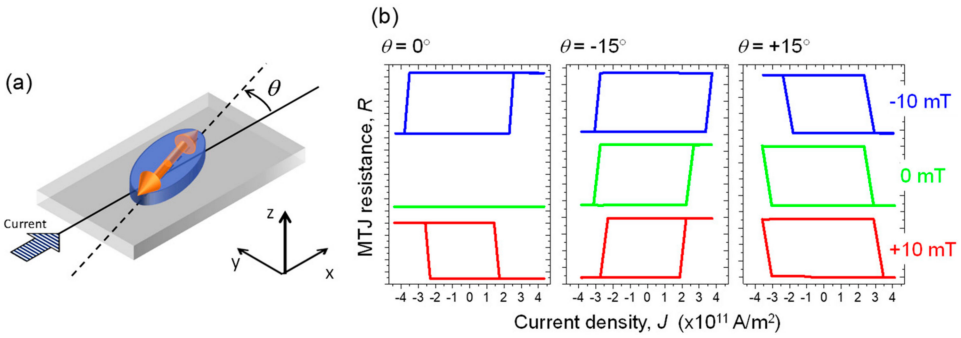


Figure 11. (**a**) SOT device structure for field-free switching where the easy axis of magnetization, parallel to the major axis of ellipse, θ is canted from the x-axis. (**b**) Resistance versus current density curve for the SOT device with $\theta = 0°$ (x-type) and 15°.

Where the easy axis of magnetization is parallel to the major axis of ellipse, θ is varied from 0 (x-type) to $\pm 15°$ with respect to the x-axis. To switch the magnetization in the x-type device with

$\theta = 0°$, a small out-of-plane field is necessary, whereas the switching can be observed in the device with $\theta = \pm 15°$ in an absence of the out-of-plane field. The results demonstrate that the field-free switching can be achieved in the SOT device.

Hereafter we focus on a few issues in SOT devices to be addressed for NV memory applications. As shown in Table 1, one of the advantages of SOT devices is high potential in realizing high-speed writing operation comparable to SRAM. In order to make it clear whether the SOT device can be used in place of SRAM at low-level cache, it is necessary to confirm its high-speed operation capability at LSI level. So far, at the device level, high-speed switching down to 500 ps has been demonstrated. However, at LSI level, one needs to consider operation speed of CMOS circuits, which is necessary for driving the SOT-MRAM, including addressing and write driver, and so on. In addition to that, the read operation needs to be confirmed at LSI level. Another issue is high writing current, which is one order of magnitude larger than that of the STT-MRAM. To reduce the writing current in the SOT-MRAM, the material of the channel layer needs to be developed such that higher SOT can be obtained. So far, high resistivity W channel is preferable for it as the high spin Hall angle can be achieved. The spin Hall angle θ_{SH} is defined as $\theta_{SH} = J_S/J_e$ where J_e and J_S are applied charge current density flowing through the channel layer and a resultant transverse-flowing spin current density, respectively. A quantitative measurement method of θ_{SH} is summarized in [68].

However, high-resistivity channel layer material deteriorates the drivability of the selective transistor, resulting in an enlargement of cell size. For lowering writing current without sacrificing drivability of the selective transistor, it is required to develop the channel layer material with low resistivity while high spin Hall angle is maintained. The last issue is scaling of the SOT device. In this review, we have mainly introduced the SOT device with in-plane-type MTJs. In the in-plane MTJs, the magnetic anisotropy originates from shape anisotropy, which will become smaller as the device dimensions reduce when the free layer thickness is fixed. One option to address this issue is the introduction of perpendicular anisotropy material (z-type device). Thus, it is very important to develop perpendicular-anisotropy MTJs with the thermal tolerance against annealing at 400 °C at least using a top reference layer fabricated on the channel layer with high spin Hall angle, while some engineering needs to be introduced such that the field-free switching can be achieved. By addressing those issues, the SOT device will be very attractive for replacement of SRAM in a lower-level cache memory.

3.3. Progress of VC-MRAM

As mentioned in the introduction, the writing scheme for VC-MRAM is electric-field effect on (or voltage-controlled) magnetic anisotropy. An electric-field effect on magnetic properties have been first demonstrated in magnetic semiconductors such as (In,Mn)As and (Ga,Mn)As. In the magnetic semiconductors, the modulation of the Curie temperature, coercivity, magnetic anisotropy, and anomalous Hall coefficient has been observed [69–72]. Those studies have triggered the following intensive studies on the modulation of the magnetic properties in metals [73–86]. From memory application viewpoint, one significant breakthrough for *E*-field effect on metal is found in the demonstration of switching in the MTJ device [77–79]. In particular, Kanai et al. demonstrated the *E*-field-induced magnetization switching in perpendicular-anisotropy CoFeB/MgO system [79], which is de facto standard material system for the STT-MRAM.

Figure 12 illustrates the writing operation principle of voltage-controlled MRAM VC-MRAM. In VC-MRAM, a magnetic anisotropy modulation by electric field (voltage) is utilized. By applying the external voltage V_b, the interfacial perpendicular magnetic anisotropy of the p-MTJ is modulated [87], resulting in the change of energy barrier depth between P and AP state. When V_b is negative (positive), interfacial perpendicular anisotropy increases (decreases). At above threshold voltage, precessional switching can be achieved under magnetic field.

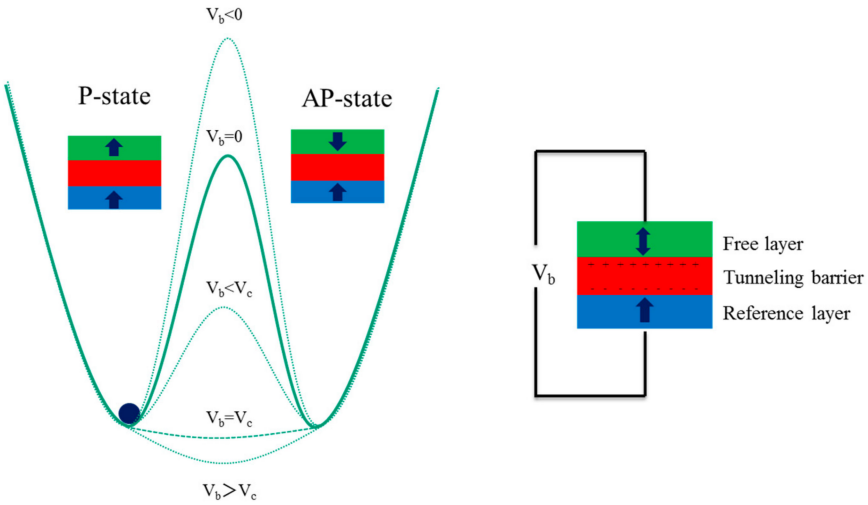


Figure 12. Schematic diagrams of writing operation principle of voltage-controlled MRAM (VC-MRAM).

Although significant developments have been done in VC-MRAM, there are still some issues for practical use in NV memory. One issue is that the required voltage to switch the magnetization is large compared with standard CMOS power-supply voltage. For example, Noguchi et al. reported VC-MRAM circuits for ultralarge last level cache memory, in which the voltage to switch the magnetization is as high as 2.2 V [10], which is larger than the standard CMOS power-supply voltage of less than 1.2 V. The necessity of such a large voltage originates from limited amounts of anisotropy modulation coefficients by *E*-field. To overcome this issue, the material development of the free-layer material is now underway [88–92]. Another issue to be addressed is the small time window for the writing. Since the precessional motion of magnetization is utilized in the VC-MRAM, the switching probability oscillates with respect to the write pulse width, resulting in the small writing-time window. One possible solution for this issue is combining *E*-field-induced switching with STT [93]. In addition to the issued raised above, it is necessary to engineer elimination of external magnetic field for precessional switching. In the papers reported so far, the external magnetic field along in-plane or out-of-plane direction is applied to induce the precessional switching. Because it is difficult to equip the external magnetic field in the LSIs, one needs to consider other schemes to induce the precessional switching without the external magnetic field.

Although there are a few issues in VC-MRAM to be addressed for practical NV memory applications, the *E*-field effect on magnetic anisotropy itself becomes useful for spintronics-based NV memory. Yoda et al. reported the possibility in reducing the memory cell size of SOT-MRAM by fabricating multiple MTJs on one channel layer, in which each MTJ can be independently switched by making use of *E*-field modulation of the magnetic anisotropy [94].

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Glossary

BEOL	back-end-of-line
MTJ	magnetic tunneling junctions
MRAM	magnetic random access memory
SOT	spin-orbit torque
STT	spin-transfer torque
VC	voltage controlled

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