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A Survey of Low Voltage and Low Power Amplifier Topologies

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Abstract: Reducing voltage supply is one of the most effective way to reduce the power consumption, but, on the other hand it is a challenging choice for the analog designers. In this paper, different topologies, well-suited for low voltage and ultra-low voltage supply, are depicted, investigated, designed in the same standard 180 nm technology and compared, highlighting the benefits and the possible applications.

Keywords: amplifiers; CMOS integrated circuits; ultra low voltage; bulk-driven amplifers; inverter-based amplifiers; rail-to-rail amplifiers

1. Introduction

One of the most effective ways to save the power is to reduce the voltage supply. On the other hand, low voltage and ultra low voltage design is challenging, especially for analog circuits. Among them, the operational trasconductance amplifier (OTA) represents the most common and used block and thus a lot of work has been and is currently devoted to fullfil the requirements of DC gain, bandwidth and slew rate, which are limited by the low voltage condition. For example, indeed, cascoding is not allowed because of the voltage headroom. Therefore, analog designers are using novel architectures, such as, for example, inverter-based amplifiers [1–5], bulk-driven and self-cascode topology [6,7], hybrid-mode input stage [8] and rail-to-rail amplifier with cross-coupled output stage [9]. In this paper, these novel topologies are analyzed, and compared, using the same standard 180 nm CMOS technology. Moreover, a nMOS-only amplifier architecture [10] has been verified in the context of low voltage supply. The paper is organized as follows: in the second section the amplifier architectures will be depicted; in the third section they will be simulated and compared, highlighting the advantages and the possible applications; in the fourth section conclusions will be drawn.

2. Amplifier Topologies

In this section, recent architectures of CMOS amplifiers are depicted. The schematics are also sized and simulated using the Design Kit of the CMOS technology UMC (United Microelectronics Corporation) 180 nm.

2.1. Inverter Based Amplifier

The technology scaling favors digital circuits, by improving speed and reducing dynamic power dissipation. Moreover, the voltage supply is constantly reduced, making the analog design challenging.

In this context, is rising the trend of implementing low-voltage, inverter-based analog circuits. Among them, examples of inverter-based OTAs can be found recently [1–5]. In this subsection, we consider three different designs: the first one is a single stage inverter-based fully differential amplifer [1], while the second one is a three stage inverter-based amplifier with a feed-forward compensation technique [2] and the last one is a current-starved amplifier [5].

2.1.1. Tunable Inverter-Based Amplifier

The inverter-based amplifier has the same topology of the CMOS digital inverter, but operates at a common-mode (CM) voltage keeping both the nMOS and pMOS transistors in the saturation region. This results in high transconductance and output resistance, and consequently high dc gain and gain bandwidth (GBW). The gain of the inverter stage can be indeed written as:

$$A_v = \frac{gmn + gmp}{gdsn + gdsp} \tag{1}$$

where gm is the transconductance and gds is the inverse of the small signal output resistance. However, a main disadvantage of operating the inverter as an amplifier is the high variation of the inverter dc gain and gain bandwidth (GBW), with temperature and process corners. To overcome this problem, a simple circuit technique can be used to tune inverter-based amplifiers across the process and temperature variations. The conceptual schematic of the inverter-based amplifier is shown in Figure 1, while the detailed description is given in [1].

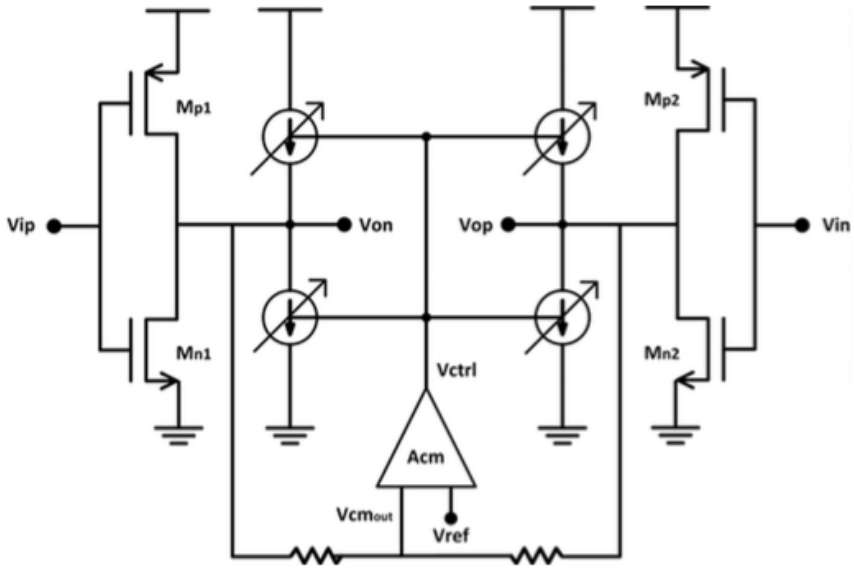

Figure 1. Tunable inverter-based amplifier.

The tuning technique is basically a CM feedback (CMFB) circuit that senses the output CM voltage and controls the current flow through the inverter using four controlled current sources. Indeed, the small signal parameter gm and gds are highly dependent on the voltage drop between the drain and source Vds which, in the inverter topology, is also the common mode (CM) output voltage. Therefore, for a simple inverter-based OTA, fixing the output CM helps, also, to fix the dc gain, and the dc-gain variation becomes limited to the variation in the threshold voltage. The tuning circuit maintains a robust operation with small dc-gain variations across the temperature and process corners, by fixing Vds of both the nMOS and pMOS transistors, for the OTA. Figure 2 shows the implementation of the tuning circuit. Stacking a tunable current source within the main OTA would consume voltage headroom, therefore the current sources that receive the control signal from the

CMFB amplifier (Acm) are added in parallel to the OTA output transistors. The CM of the OTA is extracted using two resistors and compared with a reference voltage (Vref), set at the half the supply voltage, using the amplifier Acm, shown in Figure 3. The output of the amplifier controls the nMOS and pMOS current sources (MI1–MI4). The CMFB current sources can source or sink current into the main OTA. The Acm amplifier is a simple pseudodifferential amplifier. At a certain temperature and process corner, if the output CM voltage (Vcmout) is lower than Vref, then Vctrl becomes low. This forces MI3 and MI4 transistors to source more current into the main OTA until Vcmout nearly equals Vref. The opposite operation happens when Vcmout is higher than Vref.

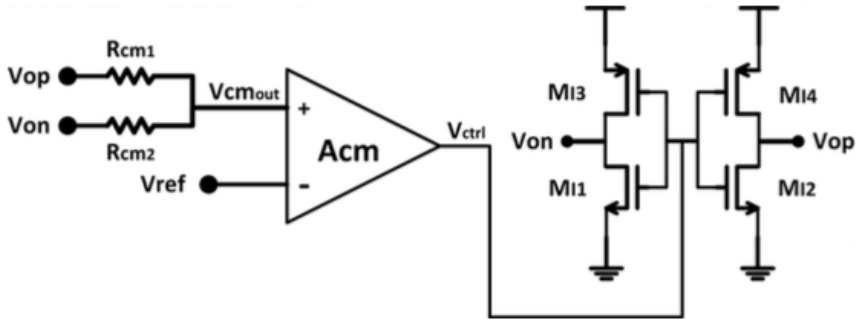

Figure 2. Schematic of the CMFB.

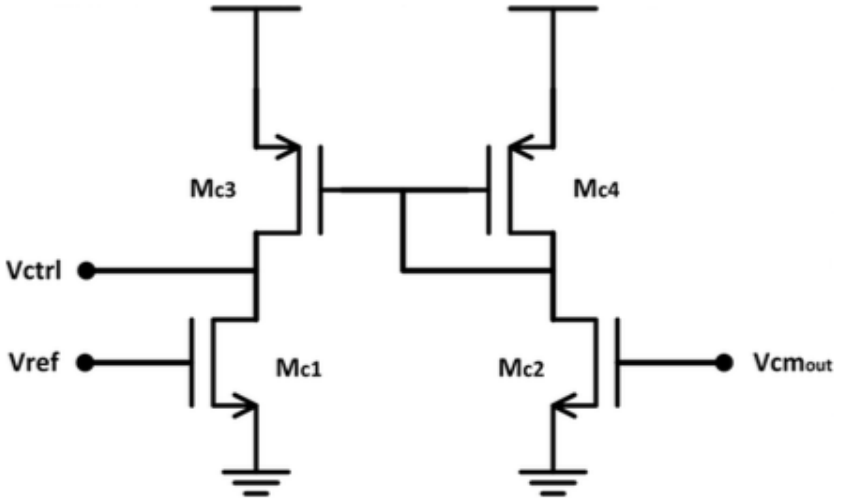

Figure 3. Acm amplifier.

The proposed circuit maintains the output CM of the inverter-based amplifier, without requiring any additional voltage headroom to the simple inverter structure. Therefore, the low-voltage operation is achieved.

2.1.2. Inverter-Based Amplifier with Feed-Forward Compensation

In [2] a different inverter-based amplifier is proposed and widely discussed. It is based on the cascade of three stages with feed-forward compensation, to achieve a reasonable gain without sacrificing the bandwidth. The conceptual schematic is shown in Figure 4 and the detailed schematic is drawn in Figure 5: at low frequency, the three stage amplifier provides a gain of approximately $-(A_O)^3$, while at high frequencies, since path B is faster, the amplifier shown only the gain of the

single stage in the feedback loop $-(A_F)$. For the sake of completeness, the low frequency gain is given by:

$$A_O^3 = -(gm \cdot rds) \cdot \frac{\alpha + gm^2 rds^2}{1 + \alpha} \quad (2)$$

where gm is the sum of the transconductances of the nMOS and pMOS devices, rds is the parallel combination of the output resistances of the nMOS and pMOS devices, and α is the ratio between the geometry of the transistors in the path B and the corresponding in the path A. As already stated, the main drawback of the inverter used as an amplifier is the high variation of its AC characteristics (dc gain and gain bandwidth (GBW)), with temperature and process corners. Therefore, a biasing circuit is added (and shown in Figure 6) which bias the n-well of the pMOS transistors, so to allow high gain at a fixed middle supply CM voltage, independently of process, temperature and power supply variations. The ratio between the transistors of path A and path B is chosen to achieve the desired phase margin.

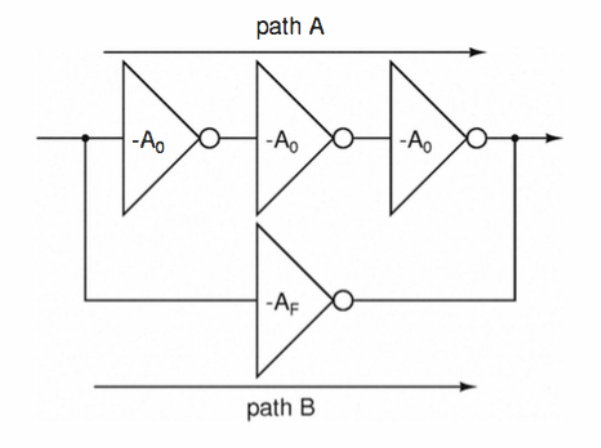

Figure 4. Conceptual schematic of the inverter-based amplifier with feed-forward compensation.

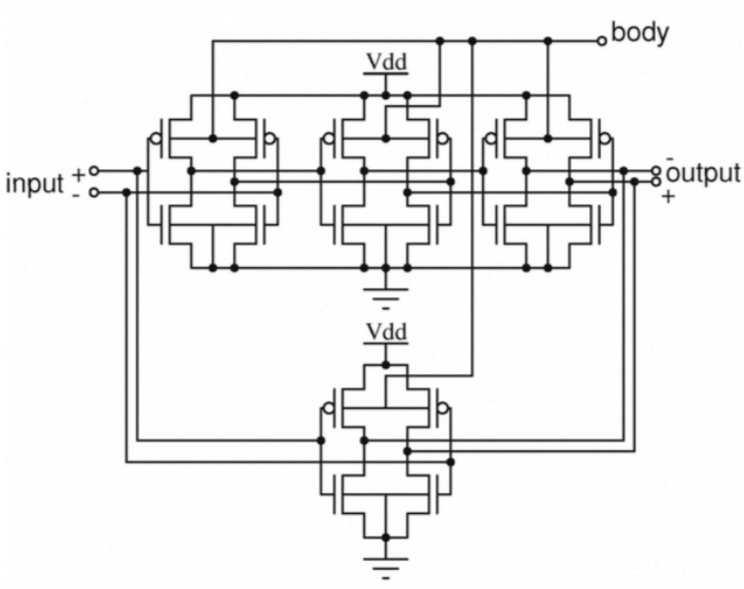

Figure 5. Frequency compensated three stage amplifier.

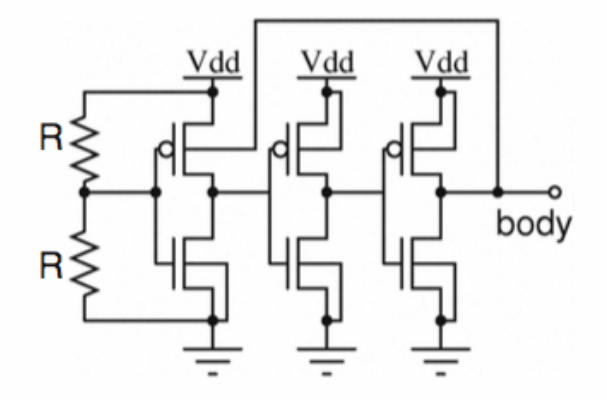

Figure 6. N-well biasing circuit.

2.1.3. Current-Starved Inverter-Based Amplifier

As already stated, an interesting solution in designing amplifier working with very low voltage supply is the inverter-based topology. When the inverter-based amplifier is implemented at a low supply voltage, the transistors will operate in the sub-threshold region, with a consequent reduction of bias currents and power consumption and, at the same time, of bandwidth and amplifier driving capability. A modification of the standard inverter-based amplifier is proposed in [5]: the novel input stage includes a couple of tail current sources (both N and P type) to better control the current through the inverters, pushing the transistors further into the sub-threshold region, and further reducing power consumption. The tail sources can also improve the amplifier's CMRR (Common-mode rejection ratio) and provide an additional input that can be used for common-mode feedback, overcoming the problems of the original inverter-based design. In addition, the use of tail separates the need for low power consumption and low input offset voltage: the inverters can be sized, indeed, appropriately to control offset voltage while the tail controls the overall power consumption.

The proposed topology shown in Figure 7 employs an active load consisting of four additional load inverters (M2, M3). M2 is connected in a cross-coupled configuration, while the outer pair of inverters (M3) is diode-connected as shown in Figure 7. The cross-coupled pair provides positive feedback and therefore a negative resistance of $-2/gm3$. The diode connected pair provides a positive resistance of $2/gm2$. This positive resistance helps stabilize the unstable negative impedance of the cross-coupling, as well as providing DC bias stability for both the input and cross-coupled inverter pairs. This combination of positive and negative impedances gives the active load circuit a large output impedance equal to the inverse of ($gm2$–$gm3$). The overall voltage gain of the amplifier's half-circuit can then be defined as:

$$A_v = \frac{gm1}{gm2 - gm3} \tag{3}$$

When sizing the transistors in this design, it is desirable for the input and tail transistors to have reasonably large lengths (typically more than 1 μm) and large W/L ratios (typically more than 16) to improve output impedance, and to have an increased transconductance.

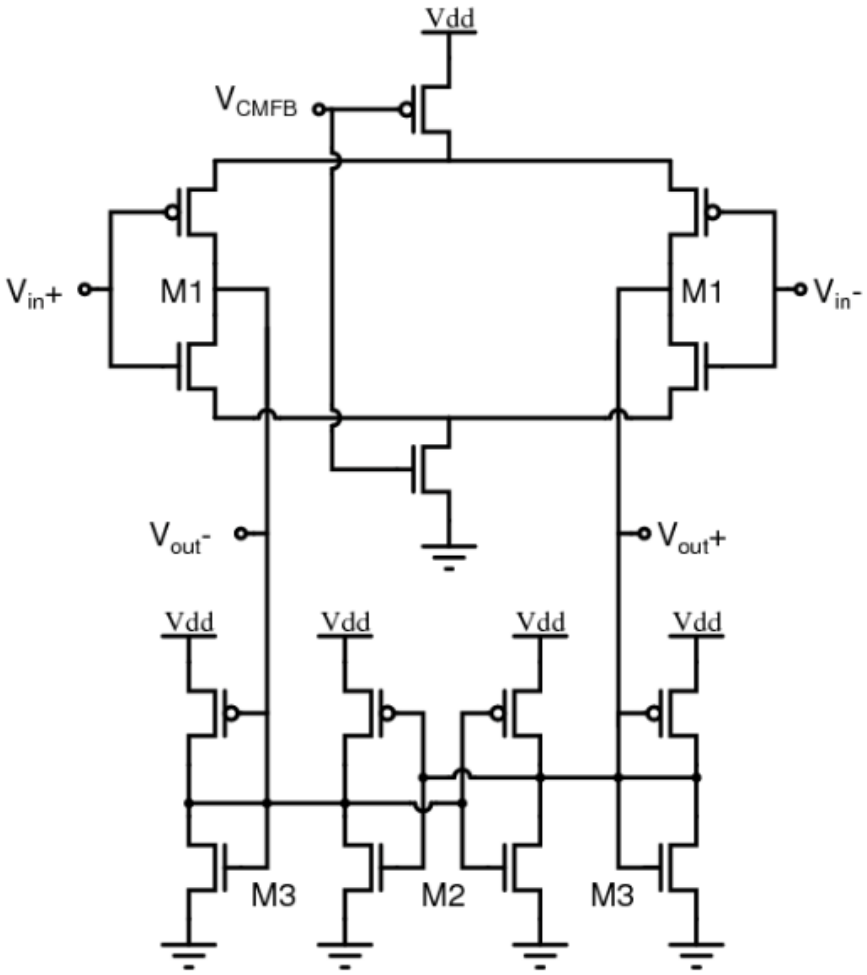

Figure 7. Current-Starved Inverter-Based Amplifier.

2.2. Bulk-driven Ampliifer

A bulk-driven Miller amplifier is composed of an input differential pair, a current source, an active load and a common source stage. The gain of the input stage is given by the small signal parameter gmb (bulk transconductance), which is of course much lower than gm (gate transconductance), multiplied by the output resistance; this results in a smaller gain and gain-bandwidth product of the bulk-driven topology respect to the classical gate-driven. However, compared to the standard gate-driven Miller OpAmp, in the bulk-driven one the input signals arise from the bulk of the differential pair, while the gate, the source and the drain voltages provide the bias of the transistors. This technique is especially appealing in the field of ultra low voltage applications, in particular biomedical, because the latter need a low power consumption and very low voltage supply, without requiring mostly a large gain-bandwidth product. Moreover, thanks to the bulk-driven technique, the input stage exhibits a better common mode input range, compared to the gate-driven topology. The bulk-driven amplifier exhibits also a lower susceptibility to the Electromagnetic Interferences, as depicted in [11]. Nevertheless, considering a P-type bulk-driven input stage, one can say that the circuit shows a poor linearity if the common-mode voltage is close to the negative rail. The differential pair causes, indeed, distortion to the signal, since the active load starts switching off. The analog happens for the N-type input stage if the common-mode voltage is close to the positive rail. To solve this problem, two batteries should be placed in series with the active load, to provide a dc shifting on the signal; in this way, the active load remains operational with constant voltage for lower values of the input signal, thus avoiding non linearity conditions. The battery can be replaced by a common-gate

amplifier. In terms of dc analysis, indeed, the transistor in diode configuration can be modeled by a resistance whose value is given by the inverse its transconductance, emulating a battery. Nevertheless, in terms of ac analysis, the composite transistor Q3–Q4 is an active load, and it presents a gain. A modified bulk-driven Miller amplifier, based on composite folded active load, is therefore presented in [6]. The composite transistor is an important configuration for MOS transistor in weak inversion, and generally for low voltage applications, because it presents a better gain respect to the single transistor without consuming voltage headroom.

The overall gain of the amplifier in Figure 8 is that of a two stage amplifier. The second stage provides the typical gain of a common source stage with active load and it can be written as:

$$A_vII = \frac{gm6}{gds6 + gds7} \tag{4}$$

The first stage has a gain similar to that of a folded cascode amplifier with a bulk driven input stage:

$$A_vI = \frac{gmb2}{gds9 + gdsEQ} \tag{5}$$

where $gdsEQ$ is the output resistance of the cascode load (Q4a, Q4b, Q2), approximately given by:

$$gdsEQ = \frac{gm4 + gmb4}{gds4} \cdot \frac{1}{gds4a + gds2} \tag{6}$$

The frequency behaviour is very similar to that of a standard two-stage amplifier and therefore the Miller compensation is added to assure the stability. Moreover, to increase the DC-gain, the schematic proposed in [6] can be improved by adding a cross-coupled pair to the bulk-driven input OTAs, which provides the positive feedback, as depicted in [7]. The transconductance with the positive feedback becomes indeed much larger than the transconductance gmb in the conventional bulk-driven input. Moreover, the frequency response of the classical two-stage schematic is improved in [7] by using an indirect feedback compensation method which expands the bandwidth and reduces the compensation-capacitor at a sub-threshold voltage.

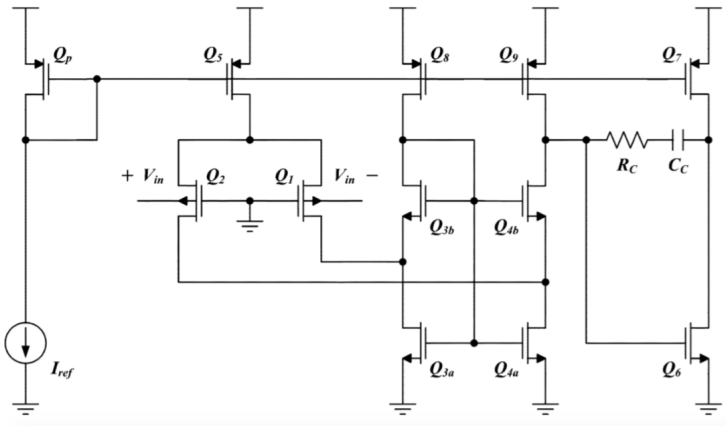

Figure 8. Bulk-driven Miller amplifier.

2.3. Hybrid Mode Amplifier

Voltage regulator is another fundamental analog building block, based on an error amplifier and a power transistor which drives the loads. In low voltage and low power applications, it presents the major challenge of achieving a good dynamic response with a low quiescent current. Therefore, the adaptive biasing scheme is used, because its the quiescent current is very small at low-load condition and gradually increases to a high value at high-load condition. Hence, when the

load current switches from the high-to-low load condition, the higher quiescent current at high-load condition initially provides a fast charging of the gate node of the power transistor connected to the error amplifier, resulting in a small overshoot at the output. However, for the low-to-high load transient edge, the low quiescent current provides a larger undershoot due to the slow discharging of the gate node of the power transistor. For this purpose, a hybrid-mode operational transconductance amplifier (HM-OTA) has been proposed, that does not occupy extra space in silicon or consume additional power to realize, while presenting a fast discharging slew-rate and achieving a good dynamic response. The hydbrid-mode amplifier is depicted in [8] and it is shown in Figure 9c, where its topology is compared to the common-mode amplifier (CM-OTA) in (a) and to the differential-mode (DM-OTA) in (b).

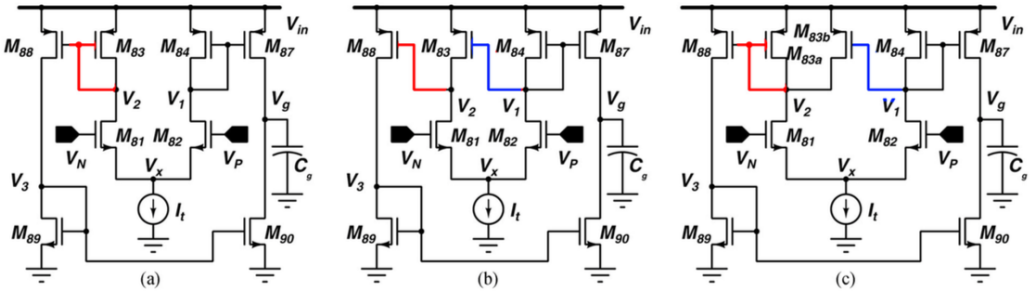

Figure 9. Schematics of CM-OTA (**a**), DM-OTA (**b**), HM-OTA (**c**).

The first one (Figure 9a) is the common-mode amplifer: it is a possible solution for implementing the error amplifier in the voltage regulator due to its single pole behavior, which eases frequency compensation. However, it has very limited dc gain as all the internal nodes have low impedance. Moreover, under large signal operation, the charging/discharging slew rate is also symmetric and quite limited. For the sake of completeness, the gain A_v of the CM-OTA is approximately given by:

$$A_v = \frac{gm82}{gm84} \cdot \frac{gm87}{gds87 + gds90} + \frac{gm81}{gm83} \cdot \frac{gm88}{gds87 + gds90} \tag{7}$$

and it is similar to a one-stage amplifier. A conventional differential-mode OTA (DM-OTA) (Figure 9b) is a more preferred option, as it provides a high dc gain as well as asymmetric slewing operation in large signal. The gain A_v is indeed:

$$A_v = \frac{gm82}{gm84} \cdot \frac{gm87}{gds87 + gds90} + \left(\frac{gm81}{gds81 + gds83} + \frac{gm82}{gm84} \cdot \frac{gm83}{gds81 + gds83}\right) \cdot \frac{gm88}{gds87 + gds90} \tag{8}$$

and it is the two-stage amplifier gain. However, the high impedance from the internal node creates a stability issue in the regulator with a small value of output compensation capacitor and a low quiescent current. Essentially, the value of the output capacitor has to be increased to restore the stability. The HM-OTA is constructed by combining both the CM-OTA and the DM-OTA as shown in Figure 9c and exploits the advantages of both the structures. Unlike the CM-OTA, the transistor M_{83} is segmented into two parts namely, M_{83a} and M_{83b}. Also, the gate of M_{83b} is connected to V1 instead of the node V2 in the proposed HM-OTA. This modification forms a localized differential stage, which forces the delta/difference current of I_{81} and I_{83b} through I_{83a} . The ratios of $M_{84} : M_{83b}$ and $M_{83a} : M_{83b}$ are chosen as 1:α and (1-α):α, respectively, for maintaining dc current balancing in the HM-OTA. So, the HM-OTA becomes a combination of αxCM-OTA and $(1-\alpha)$xDM-OTA for $0 \leq \alpha \leq 1$. The differential gain is in this case:

$$A_v = \frac{gm82}{gm84} \cdot \frac{gm87}{gds87 + gds90} + \left(\frac{gm82}{gm84} \cdot \frac{gm83b}{gm83a} + \frac{gm81}{gm83a}\right) \cdot \frac{gm88}{gds87 + gds90} \tag{9}$$

and it is the gain of an improved one-stage amplifier. The slew-rate performance of the proposed HM-OTA is discussed now. During large signal operation, the charging slew rate SR+ is similar to the conventional CM-OTA/DM-OTA. During discharging operation, the transistors M_{82},M_{84}, M_{83b} completely shut off and the whole tail current flows through M_{81} and M_{83a}. Due to the width ratio of M_{83a} and M_{88} the negative SR is higher than the conventional CM-OTA by a factor of $1/(1-\alpha)$. Of course, the value of SR- of HM-OTA is still less than the conventional DM-OTA; however the latter causes a stability issue in the regulator as mentioned before. The main advantage of the HM-OTA over the CM-OTA and the DM-OTA is that the dc gain, loop bandwidth, slew rates, and loop stability can be easily controlled with the value of α. Also, this modification does not require any additional space and quiescent current.

2.4. Rail-to-Rail Amplifier with Cross-Coupled Output Stage

In Figure 10 rail-to-rail operational amplifier with ultra-low-power operation is shown. The amplifer has a two-stage architecture based on a complementary input stage and a novel cross-coupled output stage. The cross-coupled output stage increases the transconductances of the MOSFETs of the output stage without requiring additional chip area. Hence, it increases the gain of the amplifier and drivability for a capacitive load.

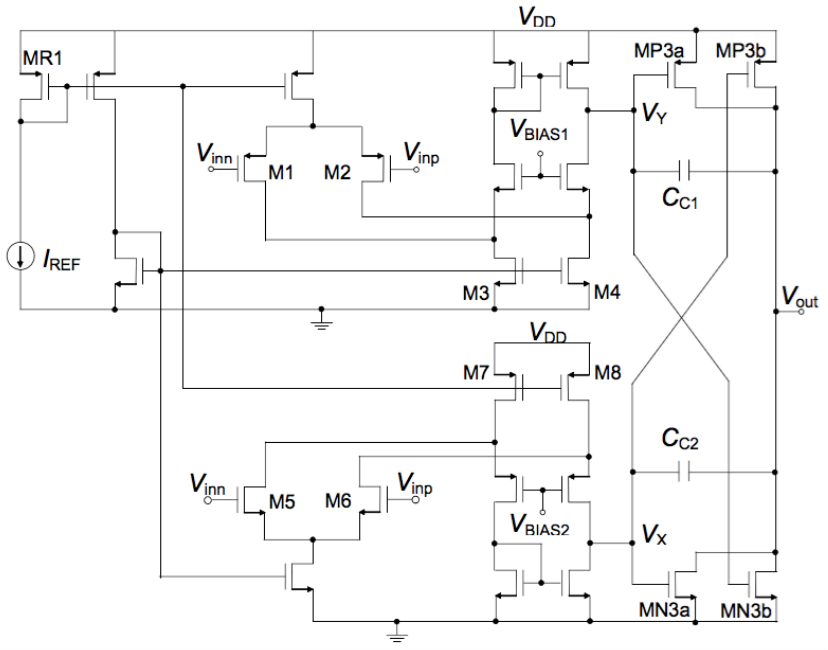

Figure 10. Schematic of the rail-to-rail amplifier with cross-coupled output stage.

The voltage gain of the amplifier is given by A_{VI} multiplied by A_{VII}, which are approximately:

$$A_vI = \frac{gm2}{gds_{CascodeN} + gds_P} + \frac{gm6}{gds_{CascodeP} + gds_N} \tag{10}$$

$$A_vII = \frac{gm_{P3a} + gm_{N3b}}{gds_{out}} + \frac{gm_{N3a} + gm_{P3b}}{gds_{out}} \tag{11}$$

where gds_{out} is given by the conductance of the cross-coupled output stage and therefore, it is:

$$gds_{out} = gds_{P3a} + gds_{P3b} + gds_{N3a} + gds_{N3b} \tag{12}$$

The architecture is well explained in [9] but the output stage is also reported in Figure 11 for the sake of clarity. In brief, the output stage proposed in [9] is divided in two branches, one cross-coupled and the other one in standard common-source topology. This exploits in increased transconductance and therefore enhanced gain and drivability for a capacitive load, respect to the standard common-source stage, with moderate current consumption, respect to the fully cross-coupled topology. The frequency behaviour is similar to that of a standard two-stage amplifier and therefore a Miller compensation capacitance is added between the output of the first and the second stages.

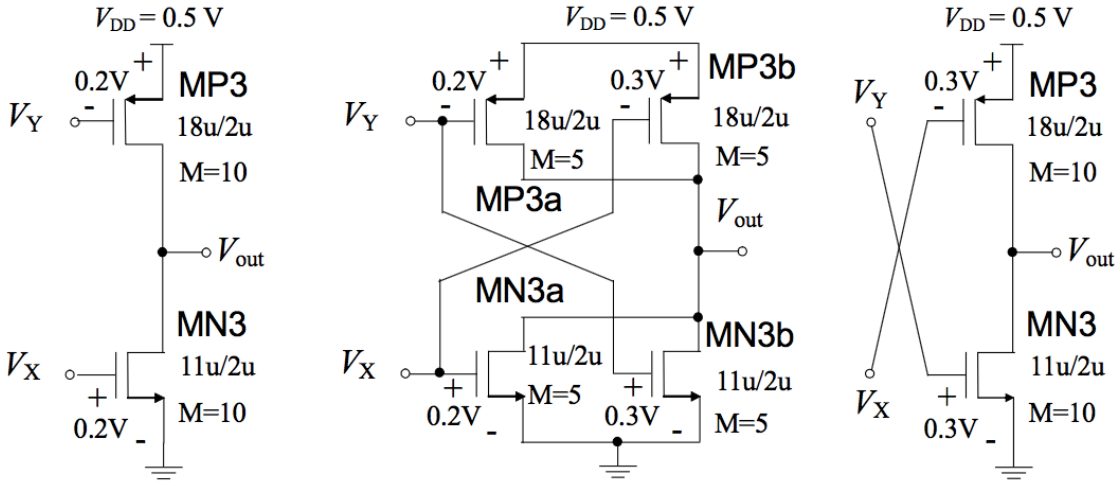

Figure 11. Conventional common-source output stage; cross-coupled output stage proposed in [9]; fully cross-coupled output stage.

2.5. NMOS-Only Amplifier

Another interesting architecture for low voltage and ultra low voltage applications is the one proposed in 1979 in the paper [10]. This amplifier is only based on nMOS devices, as shown in Figure 12; neverthless it provides the gain required in most of low voltage applications (such as, for example, biomedical and sensors). The nMOS-only amplifier is attractive because in recent technologies nMOS native transistors (i.e., with extremely low threshold voltage) are available and therefore an architecture based only on nMOS transistors allows for a very low voltage supply. Moreover, no cascode devices are needed and therefore the architecture can be strongly recommended to low voltage supply. Also, this amplifier topology can be interesting in the organic technologies where avoiding the use of complementary devices can be paramount [12]. The amplifier is based on a source coupled differential pair as input stage (M_5, M_6, M_8) with diode-connected nMOS as active load (M_4, M_7); on two source follower level shifts (M_9, M_{11}), a second gain stage (M_{12}, M_{11}) and an output stage (M_{13}, M_{14}, M_{15}, M_{16}). The overall voltage gain can be approximately given by the product of the ratios between the transistors transconductances gm and can be written as:

$$A_v = \frac{gm5}{gm4} \cdot \frac{gm12}{gm11} \cdot \frac{gm14}{gm13} \cdot \frac{gm16}{gm15} \tag{13}$$

it is worth noting that a compensation capacitance must be added C_C between the main gain stages to assure the stability when the amplifier is in closed loop configuration.

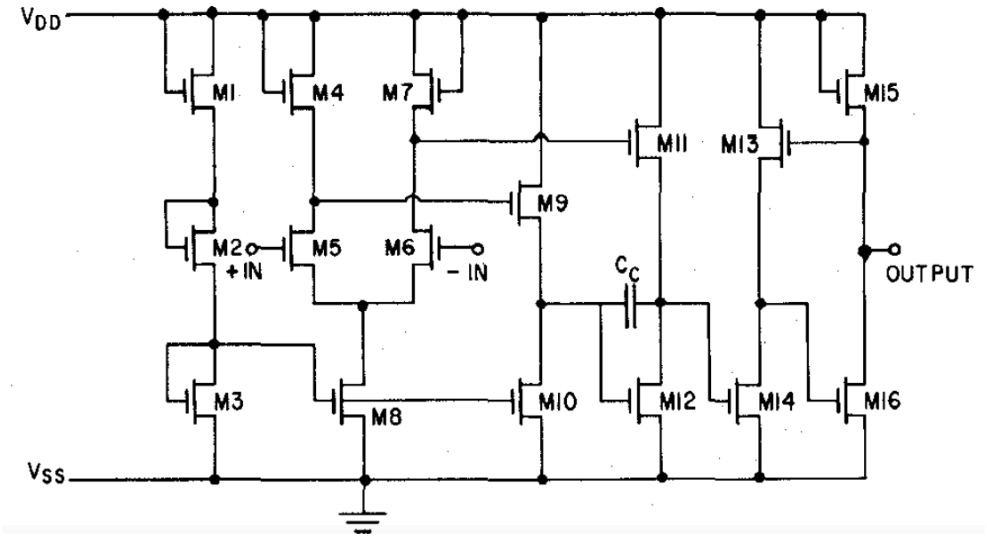

Figure 12. Schematics of the nMOS-only amplifier.

3. Results and Comparison

All the above architectures have been sized and designed in the standard UMC 180 nm CMOS technology. The layout has been carefully designed and schematic equivalent to its extracted view has been simulated. The UMC 180 nm technology is widely used in analog design because it is a ripe technology with good design kit. It provides devices for medium and low voltage supply (namely 3.3 V and 1.8 V respectively), with regular and low threshold, triple-well nMOS (along with the bulk devices) and it also provides a zero threshold nMOS transistor. Six metal levels, high resistive poly and metal-metal capacitors are available in this technology. Along with the main AC characteristics, the classical amplifier FOM (Figure Of Merit) has been also evaluated. For the sake of clarity, FOM is defined as:

$$FOM = \frac{GBW \cdot C_L}{I_{Vdd}} \tag{14}$$

where the GBW is the 0 dB frequency, C_L is the load and I_{Vdd} is the overall biasing current.

3.1. Tunable Inverter-Based Amplifier

The tunable inverter-based amplifier is designed using the standard transistors of the UMC 180 nm technology, having a nominal threshold voltage of about 340 mV (for the N-type transistors) and 500 mV (for the P-type). The circuit is therefore supplied by a voltage Vdd of 1 V. For the sake of completeness, the proposed amplifier inlcuding the CMFB circuit is compared to a simple inverter-based fully-differential stage. In the latter, the pMOS transistors are sized of 350 µm for the width and 2 µm for the lenght, while the nMOS are of W = 100 µm and L = 2 µm.The transistors sizing of the inverter-based amplifier with CMFB is, instead, listed in Table 1.

Table 1. Transistors' sizing of the Tunable Inverter-based Amplifier in Figure 1.

	Width [µm]	Lenght [µm]	Finger Number
Mn1, Mn2	100	2	10
Mp1, Mp2	350	2	24
Mi1, Mi2	4	2	2
Mi3, Mi4	16	2	2
Mc1, Mc2	1	4	2
Mc3, Mc4	4	4	2

The simple inverter-based amplifier and the amplifier with CMFB are both simulated and compared, showing very similar nominal AC characteristics which are here listed: gain of 45 dB, cut-off frequency of about 1.5 MHz, GBW of 200 MHz, phase margin of 80°. Both the amplifiers have a similar power consumption: 129 µW for the simple amplifier and 134.5 µW for the amplifier with CMFB. The amplifier with CMFB circuit exhibits a larger common mode range (about 100 mV instead of the very narrow range—9 mV—of the simple inverter-based amplifier) and a better behavior when considering the process and temperature variation. For example, by considering the corner analysis, the gain of the amplifier wth CMFB is always above 40 dB, while the simple amplifier does not work in one corner condition, and a similar result occurs also if the temperature is varied in the range between −40 °C and +80 °C. Therefore we can say that the tunable inverter-based amplifier is a more robust circuit compared to the simple one. The final layout of the inverter-based amplifier with CMFB occupies an area of about 120 µm × 40 µm and the calculated FOM is of 1.6.

3.2. Inverter-Based Amplifier with Feed-Forward Compensation

To investigate the feasibility of the inverter-based amplifier with feed-forward compensation, it has been first designed for 1.2 V voltage supply, but its performances have been also evaluated for lower and lower Vdd (down to 0.4 V). For the three inverter stage of the path A, the length has been chosen of 240 nm, the pMOS width of 18 µm and the nMOS width of 6 µm. For the inverter stage of the path B, the length is 240 nm, the pMOS width is 270 µm and the nMOS width is 90 µm. For the bulk voltage reference circuit, R is 10 kΩ, the length of all the transistors is again 240 nm, the pMOS width is 24 µm, the nMOS width is 6 µm.

The layout of the overall circuit occupies an area of about 60 µm × 40 µm.

The simulations have been performed on the circuit equivalent to the extracted layout, at different Vdd conditions, ranging from 0.4 V up to 1.2 V; the common mode has been kept at Vdd/2. Gain, gain-bandwidth product and phase margin (PM) have been listed in Table 2. For a better readability the gain and the gain-bandwidth are also plotted versus the voltage supply in Figure 13.

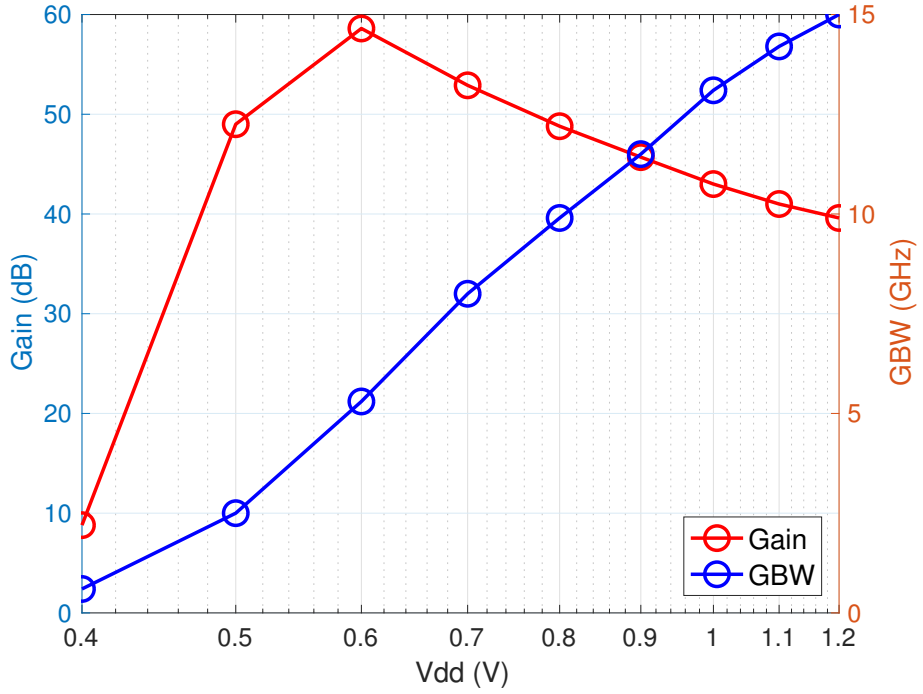

Figure 13. Voltage gain and gainbandwidth product versus Vdd for the inverter-based amplifier with feed-forward compensation.

As highlighted by the table, the amplifier is well suited also for ultra low voltage supply; moreover, it is worth noting that these simulations at different voltage supplies have been performed on the original amplifier design (i.e., the one optimized for 1.2 V) without any sizing arrangement or changes. FOM has been evaluated on 1.2 V of Vdd and it is of 4.24. Finally, corner analysis was performed in the nominal Vdd condition: the gain changes only of 4 dB and the GBW is always above 10 GHz with a good phase margin. Due to the medium gain and the very large bandwidth, this amplifier can be used for high data-rate applications which require low voltage (for example in biomedical image recording and processing).

Table 2. Main AC characteristics.

Vdd	Gain	GBW	PM
0.4 V	8.8 dB	0.6 GHz	120°
0.5 V	49 dB	2.5 GHz	46°
0.6 V	58.6 dB	5.3 GHz	18°
0.7 V	52.9 dB	8 GHz	30°
0.8 V	48.8 dB	9.9 GHz	39°
0.9 V	45.7 dB	11.5 GHz	48°
1 V	43 dB	13.1 GHz	55°
1.1 V	41 dB	14.2 GHz	60°
1.2 V	39.6 dB	15 GHz	65°

3.3. Current-Starved Inverter-Based Amplifier

The current-starved inverter-based amplifier has been designed in the UMC 180 nm technology. The nominal voltage supply has been chosen of 1.1 V and the required driving capability at 1.1 V Vdd is refered to a capacitive load of 15 pF. Good voltage gain, bandwidth, stability and rejection of common-mode signals are required as well. In addition, the power consumption must be kept below a few tens of μW. The transistors' sizing are listed in Table 3.

The layout of the circuit occupies an area of about 40 μm × 40 μm. It was extracted and the resulting amplifier was simulated: it presents a gain of 53 dB, a GBW of 3.6 MHz with a phase margin of 90°, a CMRR of 233 dB and a power consumption of 21 μW.

Table 3. Transistors' sizing of the Current-Starved Amplifier in Figure 7.

	Width [μm]	Lenght [μm]	Finger Number
nMOS1	2	1	2
pMOS1	4	1	8
nMOS2	2	4	4
pMOS2	1	2	2
nMOS3	3	3	6
pMOS3	1	2	2
N-CMFB	5.5	7.5	1
P-CMFB	3	1	1

The same amplifier (with the same transistors' sizing) was also simulated at different biasing conditions, and in particular with a voltage supply of 0.9 V and 0.7 V, in order to investigate its behavior in the case of ultra-low voltage applications. The main characteristics of the amplifier at different voltage supply are, therefore, reported in Table 4. The behavior of this amplifier is satisfactory also at very low voltage supply, as shown in the table. Moreover, the figure of merit (FOM) depends on the value of Vdd and it is of 1.93 for 0.7 V Vdd, of 3.45 for 0.9 V Vdd, of 2.87 for 1.1 V Vdd.

Table 4. Transistors' sizing of the Current-Starved Amplifier in Figure 7.

Vdd	1.1 V	0.9 V	0.7 V
A_v	53 dB	65 dB	74 dB
GBW	3.6 MHz	2 MHz	208 kHz
Load	15 pF	6 pF	1.8 pF
Phase margin	90°	90°	90°
CMRR	233 dB	180 dB	211 dB
Power consumption	21 µW	3 µW	137 nW

3.4. Bulk-Driven Amplifier

The bulk-driven amplifier proposed in [6], has been sized for the UMC 180 nm CMOS technology, with these requirements: a voltage supply of 0.5 V, gain of 30 dB at least, GBW of 100 kHz with 10 pF capacitive load. The amplifier dimensions are listed in Table 5 and refer to Figure 6.

Table 5. Transistors' sizing of the Bulk-driven Amplifier in Figure 6.

	Width [µm]	**Lenght [µm]**	**Finger Number**
Q1, Q2	2.4	0.6	2
Q3a, Q4a	1.5	0.6	2
Q3b, Q4b	4.5	0.6	2
QP, Q5	2.4	0.6	2
Q6	6	0.6	2
Q7	12	0.6	2
Q8, Q9	1.8	0.6	2

Moreover, the biasing current has been chosen of 140 nA; C_C is 1pF and R_C is not mandatory for the phase margin. The final layout occupies an area of 50 µm × 20 µm, it has been extracted and the equivalent circuit was simulated. The main characteristics of the amplifier are here summarized. The gain is of 36 dB; the GBW and the phase margin for a load of 10 pF are, respectively, 277 kHz and 70°. The amplifier has a power consumption of 554 nW and a good rejection of both common-mode and power-supply noise: the common-mode rejection ratio (CMRR) is indeed 75 dB and the positive and negative power supply rejection ratio (PSRR) are around 80 dB. Moreover, the FOM is of 1.03. Therefore, this amplifier is well suited for biomedical applications where the physiological signals can be processed at low-medium frequency and where the power consumption must be reduced while keeping a high rejection of common mode signals and noise.

3.5. Hybrid-Mode Amplifier

The hybrid-mode amplifier proposed in [8] has been sized for the UMC 180 nm CMOS technology with a nominal voltage supply of 1.8 V. The layout was designed considering matching issues and it has been extracted and simulated. The extracted equivalent circuit presents a gain of 45 dB, a GBW of 20 MHz and a phase margin of 50° when it drives a capacitive load of 5 pF. The parameter α has been chosen of 0.5. Therefore the slew rate is almost doubled respect to the CM amplifier and the frequency behavior is better than the DM one. Moreover, thanks to the traditional input stage, which is a classical differential pair, the common mode input range is nearly rail-to-rail. The amplifier dimensions are listed in Table 6 and refer to Figure 9.

Table 6. Transistors' sizing of the Hybrid-mode Amplifier in Figure 9.

	Width [µm]	Lenght [µm]	Finger Number
M81, M82	10	1	2
M84,M87, M88	90	1	4
M83a, M83b	45	1	2
M89, M90	30	1	8

The final layout occupies an area of 60 µm × 40 µm and the FOM is 1.21.

3.6. Rail-To-Rail Amplifier with Cross-Coupled Output Stage

The rail-to-rail amplifier with the cross-coupled output stage has been sized for the technology UMC 180 nm. The design constraints are the voltage supply of 0.5 V and the capacitive load of 40 pF. The voltage gain must be higher than 70 dB and a gainbandwidth product of 10 kHz is required; at the same time, the power consumption must be reduced below the µW. All the transistors work in the weak inversion region with an overdrive voltage of about 100 mV; their dimensions are listed in Table 7 and refer to Figure 10.

Table 7. Transistors' sizing of the Rail-to-Rail Amplifier in Figure 10.

	Width [µm]	Lenght [µm]	Finger Number
M1, M2	18	2	4
M3,M4	11	2	4
M5, M6	11	2	4
M7, M8	18	2	4
MN3a, MN3b	44	2	4
MP3a, MP3b	72	2	4
MB1a, MB1b	11	2	4
MB2a, MB2b	18	2	4
NM1, NM2	11	2	1
PM1, PM2, PM3	18	2	1

The layout, carefully designed considering the matching issues, occupies an area of 160 µm × 40 µm; it has been extracted and the equivalent circuit was simulated. Corner analysis was also performed because the Montecarlo models are not available in the standard design kit. The amplifier fullfils the requirements always, as highlighted in Table 8, where the main AC and DC characteristics are listed.

Table 8. Corner analysis of the Rail-to-Rail Amplifier in Figure 10.

	Gain	GBW	PM	Power Consumption
TT	96 dB	11.4 kHz	61°	240 nW
FF	95 dB	13 kHz	68°	920 nW
SS	94 dB	8.5 kHz	48°	68 nW
SNFP	98 dB	12 kHz	60°	260 nW
FNSP	93 dB	11 kHz	63°	244 nW

For a better readability, these characteristics are also shown in Figures 14 and 15, where the gain along with the phase margin and the bandwidth along with the power consumption are plotted, respectively.

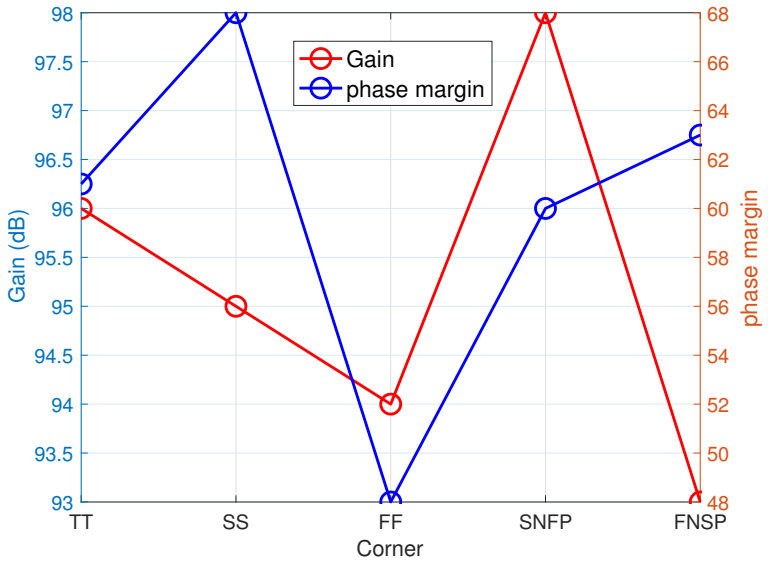

Figure 14. Gain and phase margin of the Rail-to-Rail Amplifier, simulated in the corner analysis.

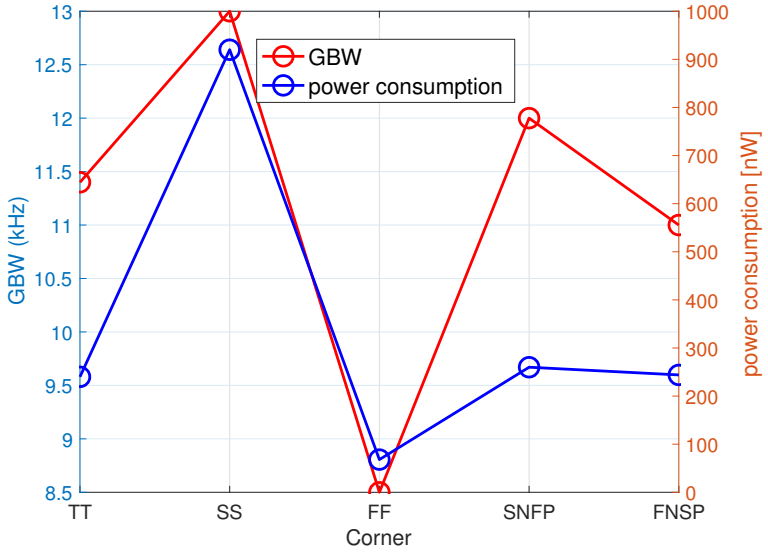

Figure 15. GBW and power consumption of the Rail-to-Rail Amplifier, simulated in the corner analysis.

Moreover, FOM has been evaluated and it is of 1.34. This amplifier can be therefore used for ultra low voltage and low power applications, where high gain and wide common mode input range are paramount.

3.7. NMOS-only Amplifier

The nMOS-only amplifier was designed in UMC180 nm technology using the regular threshold transistors and a voltage supply of 1.8 V. A gain larger than 30 dB is required. As already stated the gain is approximately given by the ratios of the transconductances, therefore the transistors must be properly sized. Two different designs are considered, simulated and compared. In the first, all the transistors work in the saturation region, while in the second one, the transistors M9, M11, M13 and M15 operate in subthreshold. The second sizing, listed in Table 9, is the most effective and shows the largest voltage gain.

Table 9. Transistors' sizing of the nMOS-only Amplifier in Figure 10.

	Width [µm]	Lenght [µm]	Finger Number
M1	42	0.5	6
M2	24	0.5	6
M3, M8, M10, M15	2	0.5	1
M4, M7	0.5	0.5	2
M5, M6	28	0.5	4
M9, M11	4	0.5	1
M12	1260	0.5	56
M13	6	0.5	2
M14	816	0.5	34
M16	1316	0.5	56

Matching issues are considering for the transistors M5, M6 and M4, M7 which are, respectively, the input pair and its active load. The internal capacitor for the frequency compensation C_C is implemented by using the metal5-metal6 capacitor provided by the UMC 180 nm process. It occupies a large area, about the half of the final layout, which is of about 200 µm × 80 µm. The equivalent circuit extracted from the layout view has been simulated and the corner analyis was also performed. The main results are summarized in Table 10. It is worth noting that the corners are two (slow and fast) because the amplifier is made by only nMOS.

Table 10. Corner analysis of the Rail-to-Rail Amplifier in Figure 10.

	Gain	GBW	PM
TT	35 dB	29 MHz	88°
FF	38 dB	34 MHz	34°
SS	29 dB	10 MHz	95°

Generally, the amplifier exhibits good GBW and stability and a medium-low voltage gain compared to the topologies based on complementary devices. Neverthless, its FOM is rather low: its value is 0.2.

4. Discussion

The amplifiers presented, designed and simulated in the above sections are discussed and compared. They can be divided in four main categories: inverter-based, bulk-driven, rail-to-rail and classical topologies with non-standard improvements. In the first category, one can consider the (1) simple inverter-based digital amplifier [3], the (2) tunable amplifier [1], the (3) amplifier with feed-forward compensation [2], and the one with current-starved devices [5]. In the second category, there are several topologies: for example, classical Miller amplifier with bulk-driven input pair can be considered, as in [11], as long as folded with self-cascode bulk-driven [6] and bulk-driven with cross coupled input pair and improved frequency compensation [7]. In the third category, a rail-to-rail amplifier with transistors operating in subthreshold and cross-coupled output stage is considered [9] instead of the standard rail-to-rail because the latter has a much larger power consumption. Finally, in the four category, a standard Miller amplifier with improvement in driving capacitive load without any penalty in the frequency response is considered [8] as long as a two stage, common source amplifier with nMOS-only transistors [10].

The inverter-based amplifiers are well-suited for ultra low voltage supply because they only need a couple of complementary transistors; therefore, the minimum voltage supply is equal to a double $V_{overdrive}$. If current-starved devices are added, these amplifiers are also well suited for low power applications. Generally speaking, they exhibit good voltage gain and gain bandwidth product (GBW), which make them very appealing for wireless applications as suggested in [13]. Moreover, if they are

designed to have a low power consumption, as in the circuit with current-starved devices [5], they are also well-suited to energy harvesting applications [14]. The main drawback of the inverter-based topology is the extremely narrow common mode input range; moreover, the AC characteristics are strongly dependent on the Vdd, the temperature and the process. For this reason, an auxiliary circuit is added to limit the effect of the variations. . The bulk-driven amplifier are well-suited for low voltage and low power, too, although they require a voltage supply larger than the inverter-based topology. The voltage gain and the GBW are medium because they are based on the bulk transconductance gmb which is smaller than the gate transconductance gm. On the other hand they can amplify signals with a very wide common mode input range. They can be used in implantable circuits for the processing of biomedical signals and also in low voltage CMOS active filter, as in [15].

The rail-to-rail topologies can reach a high voltage gain and presents a very wide common mode input range, too. Moreover they can reach a tradeoff between bandwidth and power consumption, depending on the application they are used in. They can be successfully used in energy harvesting and in low power applications, like IoT sensor nodes, [16]. The main drawback of this architecture is the increased circuital complexity and silicon area.

Among several improvements of traditional common source topology which can be found in the literature, the hybrid-mode amplifier exhibits a very good driving capability (very appealing for voltage regulator and active filter design) and the nMOS-only amplifier can be of great interest, not only for the goal of designing an extremely low voltage amplifier with nMOS native transistors, but also in advanced electronic materials, like in the organic, flexible, printed technologies [17]. These considerations are summarized in Table 11 where the amplifier topologies are compared highlighting the pro and contra. In the table also area, FOM and main applications are listed for the different architectures. It is worth adding that in the case of the current-starved inverter-based amplifier, three different values of FOM are listed: it is because they are dependent on the power supply, changing from 1.1 V down to 0.7 V, as written in Section 3.3.

Table 11. Comparison between the main topologies.

	Inverter-Based	**Bulk-Driven**	**Rail-To-Rail**	**Hybrid Mode**	**nMOS-Only**
Pro	Ultra low Vdd compatibility Good GBW Low complexity	Low Vdd compatibility Wide CM	Low Vdd compatibility Wide CM High gain	Good driving capability Good PM	Ultra low Vdd compatibility
Contra	Narrow CM range Dependence on Vdd of AC characteristics	Low GBW	Complexity	Medium-low gain	Poor AC chracteristics Complexity
Area	(1)120 µm × 40 µm (2) 60 µm × 40 µm (3) 40 µm × 40 µm	50 µm × 20 µm	160 µm × 40 µm	60 µm × 40 µm	200 µm × 80 µm
FOM	(1) 1.6 (2) 4.24 (3) 1.93–3.45	1.03	1.34	1.2	0.2
Applications	Wireless apps Energy harv.	Energy harv. Biomed. apps	Energy harv. IoT sensor	Voltage regul. Active filter	Flexible organic tech.

For the sake of clarity, complexity means the number of transistors and of course it also refers to the resulting larger area consumption and noise; good PM means that the amplifier does not require frequency compensation.

5. Conclusions

Low voltage and ultra low voltage design is challenging for analog circuits and, among them, especially for amplifiers. Advanced amplifier topologies have been therefore investigated and

compared in this paper, highlighting the benefits and the weaknesses, to help the analog designers in finding the best application-dependent solutions.

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Abbreviations

The following abbreviations are used in this manuscript:

CMOS	Complementary Metal Oxide Semiconductor
UMC	United Microelectronics Corporation
OTA	Operational Transconductance Amplifier
CM	Common Mode
GBW	Gain Bandwidth
PM	Phase Margin
CMFB	Common Mode Feedback
CMRR	Common Mode Rejection Ratio
PSRR	Power Supply Rejection Ratio
FOM	Figure Of Merit

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