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A Low-Power Voltage Reference Cell with a 1.5 V Output

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Abstract: A low-power voltage reference cell for system-on-a-chip applications is presented in this paper. The proposed cell uses a combination of standard transistors and thick-oxide transistors to generate a voltage above 1 V. A design procedure is also presented for minimizing the temperature coefficient (TC) of the reference voltage. This circuit was fabricated in a standard 0.35 µm complementary metal-oxide-semiconductor (CMOS) process. It generates a 1.52 V output with a TC of 42 ppm/°C from −70 °C to 85 °C while consuming only 1.11 µW.

Keywords: voltage reference; low power; temperature dependence; CMOS integrated circuits; analog integrated circuits

1. Introduction

Voltage reference circuits are critical building blocks that are used to generate a stable voltage across a wide range of temperatures. As newer CMOS technology nodes are providing lower threshold voltages and reduced supply voltages, the main emphasis of recent designs has been to generate a low reference voltage (especially less than 1 V) using a low supply voltage. Many good designs have been developed that provide these sub-1V reference voltages using very low power (e.g., [1–6]).

However, many applications still exist that require reference voltages greater than 1 V but also consume very little power. For example, our intended application of a low-power voltage reference cell is within a reconfigurable analog/mixed-signal platform that is capable of synthesizing a wide variety of extremely low-power circuits and systems [7]. Most applications developed on our custom Reconfigurable Analog/Mixed-Signal Processor (RAMP) consume approximately 10–20 µW and are capable of sophisticated processing (e.g., voice-activity detection, speech processing, infrared proximity detection, etc.). Therefore, the biasing circuitry should consume significantly less power than the signal-processing circuitry in order to reap the benefits of the low-power operation of the RAMP. As part of the biasing structure, this RAMP system requires a reference voltage between 1–2 V. While the low-voltage output of a sub-1 V reference could be scaled to the necessary above-1 V value for our application, the additional circuitry necessary to amplify/scale the voltage would add to the overall complexity and power consumption.

While a number of good above-1 V designs have been presented, there has been a severe trade-off between having a low temperature coefficient (TC) and low power consumption. Most above-1 V reference circuits that achieve good TCs consume too much power for many ultra-low-power applications. For example, Refs. [8–11] are all able to achieve a TC < 100 ppm/°C but consume from 35 µW to 0.648 mW, which is far too much power for our RAMP system. Other above-1 V voltage reference circuits have been able to simultaneously maintain a low TC and power consumption less than 10 µW by using devices that are not available in standard CMOS processes, such as anti-doped NMOS devices [12], native NMOS devices [13], and NPN transistors [14–16].

In this paper, we present a voltage reference cell that is able to simultaneously achieve a low TC and low power consumption over a large range of temperatures. Our voltage reference cell has been fabricated in a standard 0.35 µm CMOS process and is capable of generating a reference voltage greater than 1 V with a TC < 110 ppm/°C and single µW power consumption over a wide range of temperatures. To minimize power consumption, we operate the transistors in the subthreshold regime. We also selectively use I/O thick-oxide transistors due to their higher threshold voltage and temperature dependence than standard thin-oxide devices. Specifically, the larger threshold voltage of thick-oxide devices, and a corresponding larger V_{gs} for a given current level, allows us to raise the output voltage to a higher value than can be achieved using similar techniques employing only thin-oxide devices [2], while also using a low number of transistors. In addition, the higher temperature dependence of the thick-oxide devices' threshold voltages are used to counter-balance the positive temperature-dependent terms from the rest of the circuit to achieve a low TC. Furthermore, we have created an output voltage that is a function of the ratio of resistors, and thus the temperature-dependent terms due to the resistors largely cancel out. Additionally, this resistive ratio, along with the circuit topology, permits an easy design procedure to minimize the TC.

The remainder of this paper is organized as follows. Section 2 describes the operation of the proposed circuit. Section 3 provides details on how to minimize the TC. Section 4 presents the experimental results of the proposed circuit. Finally, Section 5 presents the conclusion of this work.

2. Principle of Operation

In this section, we present a voltage reference circuit that uses both standard transistors and 5 V I/O transistors to generate a low-TC output voltage while consuming low power. The complete voltage reference circuit is shown in Figure 1. All the transistors used in this circuit are standard (thin-oxide) transistors except for M_{t1} and M_{t2} that are thick-oxide transistors (5 V I/O devices). Two resistors are used in this circuit—one to generate the reference current (R_C) and the other to generate the final reference voltage (R_{out}).

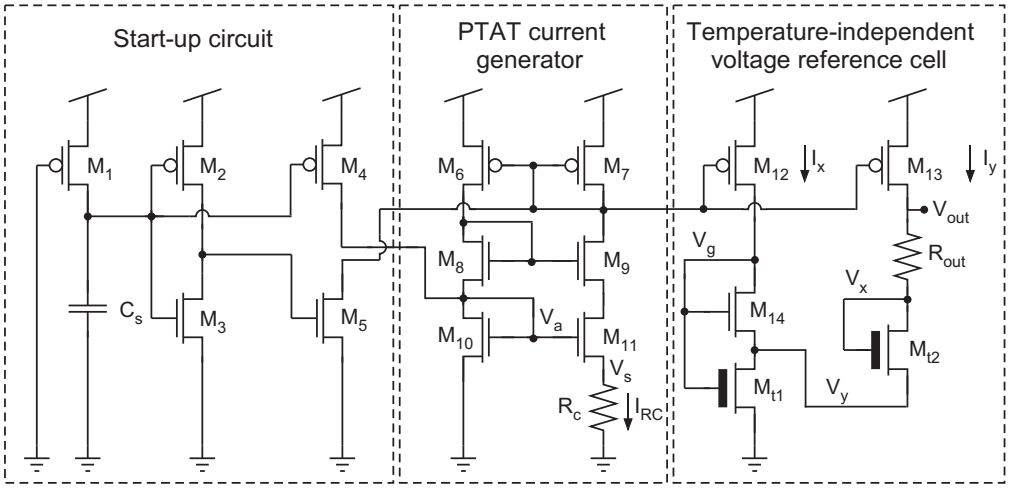

Figure 1. Schematic diagram of the proposed voltage reference cell. M_{t1} and M_{t2} are thick-oxide transistors (5 V I/O devices).

This circuit has three main blocks, as shown in Figure 1. A current reference cell is used to generate a current that is proportional to absolute temperature (PTAT). A start-up circuit is used to initialize the current reference cell and stabilize its current at a nonzero value. Finally, the third block generates the temperature-independent voltage by first creating a voltage at node V_x that is complementary to absolute temperature (CTAT). Resistor R_{out} then combines the PTAT and CTAT signals into an overall output voltage that has very low temperature dependence.

To achieve low power consumption, our circuit was designed to operate in the subthreshold region with very low bias currents. The drain current of a transistor biased in subthreshold can be expressed as [17]:

$$I_d = I_0' S e^{\frac{\kappa(V_g - V_T)}{U_T}} \left(e^{\frac{-V_s}{U_T}} - e^{\frac{-V_d}{U_T}} \right), \quad (1)$$

where $I_0' = \frac{2}{\kappa}\mu C_{ox} U_T^2$, S is the aspect ratio (W/L) of the transistor, $U_T = kT/q$ is the thermal voltage, k is the Boltzmann constant, q is the elementary charge, T is the absolute temperature in kelvins, V_T is the MOSFET threshold voltage, and κ is the subthreshold slope coefficient representing the capacitive coupling from the gate to the surface potential ($\kappa = C_{ox}/(C_{ox} + C_D)$). Voltages V_g, V_s, and V_d are the gate, source, and drain voltages, respectively, referenced to the substrate. When the transistor operates in the saturation region, $exp(\frac{-V_d}{U_T})$ approaches zero and is, therefore, negligible. We also assume that the transistors have been designed with large-enough channel lengths that the channel-length modulation effect can be safely neglected.

The detailed operation of each block will be explained in the remainder of this section.

2.1. Reference Current Generator

We use a standard PTAT current generation block that includes a current source and a current mirror. The difference between the V_{gs} values of M_{10} and M_{11} establishes a voltage across R_C. By proper sizing of R_C, M_{10}, and M_{11} ($S_{11} > S_{10}$), all the transistors in the PTAT current generator can be biased to be in the subthreshold region. By setting $S_6 = S_7$, the PMOS current mirror provides unity gain. Using Equation (1) to define expressions for the currents in M_{10} and M_{11}, the current generated by R_C is

$$I_{R_C} = \frac{V_s}{R_C} = U_T \left(\frac{1}{R_C} \right) \ln \left(\frac{S_{11}}{S_{10}} \right), \quad (2)$$

which linearly increases with temperature. I_{R_C} is mirrored to M_{12} and M_{13} with ratios of x and y. Thus, we have

$$I_x = I_{12} = I_{14} = x I_{R_C}, \quad (3)$$

$$I_y = I_{13} = I_{t2} = y I_{R_C}. \quad (4)$$

Accordingly, the voltage drop across R_{out} caused by the PTAT current source can be expressed as

$$V_{PTAT} = y \left(\frac{kT}{q} \right) \left(\frac{R_{out}}{R_C} \right) \ln \left(\frac{S_{11}}{S_{10}} \right). \quad (5)$$

This voltage is PTAT and can be set by R_{out}/R_C and the aspect ratios for M_{10} and M_{11}

2.2. Start-Up Circuit

A start-up circuit is used to initialize the current reference cell and stabilize its current at a nonzero value ($I_{R_C} \neq 0$). We use the start-up circuit presented by [18]. This start-up circuit turns on M_6, M_7, M_{10}, and M_{11} at power-up to initialize a nonzero I_{R_C}. After a very short delay, C_s is charged up to V_{dd} through M_1, thereby turning off M_4 and M_5 so that they no longer inject current to the current generator. After the brief initialization period, the start-up circuit consumes no appreciable current and, therefore, does not add to the overall power consumption of the voltage reference cell.

2.3. Temperature-Independent Voltage Reference Cell

The temperature-independent voltage reference cell is based upon a modified version of the building block shown in Figure 2a that is commonly used as a PTAT voltage generator (e.g., [19]).

The currents through M_b and M_a are I_x and $I_x + I_y$, respectively. These two currents can be expressed using Equation (1) as

$$M_b : I_x = I'_0 S_b e^{\frac{\kappa(V_g - V_T)}{U_T}} e^{-\frac{V_y}{U_T}}, \tag{6}$$

$$M_a : I_x + I_y = I'_0 S_a e^{\frac{\kappa(V_g - V_T)}{U_T}} \left(1 - e^{-\frac{V_y}{U_T}}\right). \tag{7}$$

By dividing Equation (7) by Equation (6) and solving for V_y, we find that

$$V_y = U_T \ln\left(1 + \left(\frac{S_b}{S_a}\right)\left(\frac{I_x + I_y}{I_x}\right)\right). \tag{8}$$

The resulting voltage is PTAT and can be set by proper sizing of M_a and M_b and the bias currents (I_x and I_y). However, the value of V_y cannot be made large because of the log compression working on the ratio of the transistor sizes and currents. Some designs stack this circuit repeatedly to generate a higher reference voltage, as shown in Figure 2b, but they still struggle to achieve a high voltage [20].

Figure 2c shows a modification to Figure 2a that replaces the bottom transistor with a thick-oxide device. This configuration has been used previously to provide a low voltage at V_y that is CTAT [18,21,22]. We, instead, use this configuration to help us achieve a much higher voltage at another node that is also CTAT.

The currents through M_b and M_{at} follow the forms of Equations (6) and (7), with the only differences being the various process-dependent parameters for the thick-oxide device, M_{at},

$$M_{at} : I_x + I_y = I'_{0t} S_{at} e^{\frac{\kappa_t(V_g - V_{Tt})}{U_T}} \left(1 - e^{-\frac{V_y}{U_T}}\right), \tag{9}$$

where the extra 't' in the subscript represents the value for the thick-oxide device. By dividing Equation (9) by Equation (6) and solving for V_y, we obtain

$$V_y = U_T \ln\left(1 + \frac{I_x + I_y}{I_x}\frac{I'_0 S_b}{I'_{0t} S_{at}} e^{\frac{\kappa_T V_{Tt} - \kappa V_T}{U_T}} e^{\frac{\kappa V_g - \kappa_t V_g}{U_T}}\right). \tag{10}$$

Noting that $V_{Tt} > V_T$ and that $\kappa V_g - \kappa_t V_g \approx 0$, Equation (10) can be approximated as

$$V_y \approx \kappa_t V_{Tt} - \kappa V_T + U_T \ln\left[\left(\frac{I_x + I_y}{I_x}\right)\left(\frac{I'_0 S_b}{I'_{0t} S_{at}}\right)\right] \tag{11}$$

with proper sizing of the transistors. V_{Tt} is typically several hundred mV greater than V_T, which means that using a thick-oxide transistor for M_{at} can produce a voltage at V_y that is much larger than can be produced by Figure 2a. Additionally, V_y is dominated by the first two terms of Equation (11), and since threshold voltages are widely known to be CTAT [23], V_y is also a CTAT voltage.

Next, we show that we can use Figure 2c to create a CTAT voltage at the bottom of R_{out} (V_x) in Figure 1. The current through M_{t1} can be expressed as

$$I_{t1} = \left(1 + \frac{y}{x}\right) I_{14}. \tag{12}$$

Using Equations (11) and (12), the following equation can be achieved:

$$V_y \approx \kappa_t V_{Tt} - \kappa V_T + U_T \ln\left[\left(1 + \frac{y}{x}\right)\left(\frac{I'_0 S_{14}}{I'_{0t} S_{t1}}\right)\right]. \tag{13}$$

Using Equation (13) and the equation for the current through M_{t2}, the voltage at node V_x can be expressed as

$$V_x = 2V_{Tt} - \frac{\kappa}{\kappa_t} V_T + \frac{U_T}{\kappa_t} \ln\left[\frac{\xi}{R_c T}\right], \tag{14}$$

where

$$\xi = \left(y + \frac{y^2}{x}\right) \frac{S_{14}}{S_{t1}S_{t2}} \ln\left(\frac{S_{11}}{S_{10}}\right) \frac{q}{k} \frac{\kappa_t^2 C_{ox}}{2\mu\kappa C_{oxt}^2}. \tag{15}$$

V_x is dominated by the first two terms of Equation (14), and, since threshold voltages are widely known to be CTAT [23], V_x is a CTAT voltage.

Finally, V_{out} is the summation of the PTAT voltage given by Equation (5) and the CTAT voltage given by Equation (14):

$$V_{out} = yR_{out}I_{R_C} + V_x, \tag{16}$$

$$V_{out} = y\frac{R_{out}}{R_C}U_T \ln\left(\frac{S_{11}}{S_{10}}\right) + 2V_{Tt} - \frac{\kappa}{\kappa_t}V_T + \frac{U_T}{\kappa_t} \ln\left[\frac{\xi}{R_c T}\right]. \tag{17}$$

The goal of this voltage reference cell is to generate an above-1 V output using thick-oxide transistors. The execution of this idea is visible in Equation (17), where $2V_{Tt}$ is a considerable portion of the output voltage. Additionally, the voltage drop across R_{out} further increases V_{out}. Thus, using the proposed structure, a higher voltage can be achieved by using a small number of transistors and taking advantage of the thick-oxide transistor's larger threshold voltage.

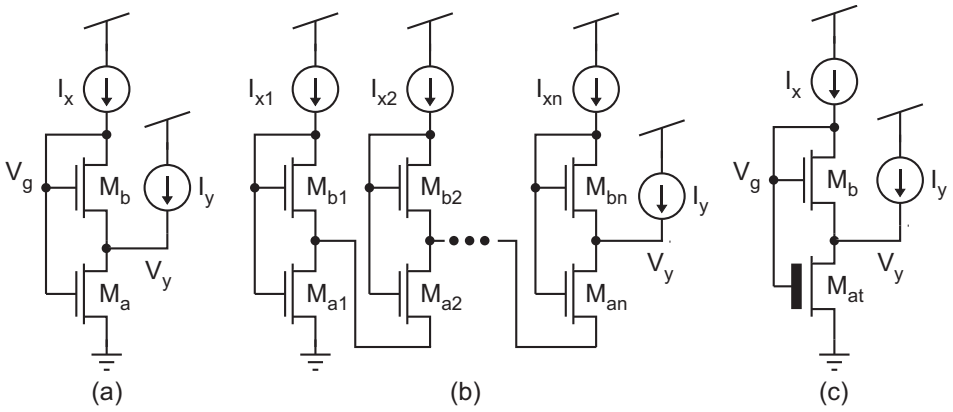

Figure 2. (**a**) A PTAT voltage generator; (**b**) generating a higher voltage through stacking PTAT voltage generators; (**c**) a CTAT voltage generator.

3. Design Procedure for Low TC V_{out}

In this section, we discuss how to design this voltage reference circuit to have a low temperature coefficient. By taking the derivative of Equation (17) with respect to T, we arrive at an equation for the TC at V_{out}:

$$TC = \frac{\partial V_{out}}{\partial T} = y\frac{k}{q}\frac{R_{out}}{R_C} \ln\left(\frac{S_{11}}{S_{10}}\right) + 2\alpha_t - \frac{\kappa}{\kappa_t}\alpha + \frac{k}{\kappa_t q}\left[\ln\left(\frac{\xi}{R_c T}\right) - 1\right]. \tag{18}$$

The α terms, which have a negative value, come from the commonly used expression for the temperature effects on the threshold voltage [23] given by

$$V_T(T) = V_T(T_0) + \alpha(T - T_0), \tag{19}$$

where T_0 is a reference temperature, and T is the temperature of interest. The α terms are generally in the mV/K range, with I/O thick-oxide devices typically having larger values than thin-oxide devices.

Analyzing Equation (18), we can see that the temperature dependence of the resistors and their exact values have little impact on the TC; assuming both resistors are made from the same material, their temperature dependencies cancel in the first term. R_C is also contained within the ln term, but its temperature effects have little impact since they are compressed by the logarithmic function; hence,

the temperature effects of R_C are neglected in this analysis (and they are far less significant than the T term in the same ln function). The ξ term also contains the temperature-dependent items μ, κ, and κ_t; again, since they are logarithmically compressed, they have little impact on the overall TC, and their temperature effects can be safely neglected. The only other remaining temperature-dependent term in Equation (18) is T within $\ln(\xi/R_C T)$. Since T is within an ln function, its effect on the TC is significantly compressed, meaning that it is possible to achieve a low overall TC. To achieve a low TC over a temperature range of interest, a reference temperature in the middle of the range should be chosen; then, the TC can be minimized by setting Equation (18) equal to zero at that reference temperature, T_0. By then solving for $\ln(\xi/R_C T)$ and plugging that expression into Equation (17), we find the optimal value for V_{out}:

$$V_{out,optimal} = 2V_{Tt} - \frac{\kappa}{\kappa_t}V_T - 2\alpha_t(T_0) + \frac{\kappa}{\kappa_t}\alpha(T_0) + \frac{U_T}{\kappa_t}, \tag{20}$$

$$V_{out,optimal} \approx 2V_{Tt} - V_T - 2\alpha_t(T_0) + \alpha(T_0) + \frac{U_T}{\kappa_t}. \tag{21}$$

Noting that the α terms have negative values (i.e., V_T is CTAT) and are typically in the mV/K range [23], the optimal V_{out} at room temperature will be greater than 1 V, particularly because of the reasonably high V_T of 5 V I/O devices. An estimate for $V_{out,optimal}$ can be calculated from Equations (20) and (21) by obtaining values for V_T, V_{Tt}, κ, κ_t, α, and α_t from the simulation models. Accordingly, for our design, $V_{out,optimal} \approx 1.6$ V.

To minimize the TC, the output voltage of this circuit as given by Equation (17) should be designed to equal $V_{out,optimal}$. The use of the resistive ratio R_{out}/R_C greatly simplifies this design consideration. Once again, we note that the transistor aspect ratios in Equation (17) are primarily within ln functions, so the ratio of R_{out}/R_C plays an important factor in establishing the correct V_{out}. To determine the best ratio for R_{out}/R_C to minimize the TC, Equations (17) and (20) can be equated, and the best resistor ratio can be found to be

$$y\frac{R_{out}}{R_C} = \frac{\frac{1}{\kappa_t}\left[1 - \ln\left(\frac{\xi}{R_C T_0}\right)\right] - \frac{q}{k}(2\alpha_t - \alpha)}{\ln\left(\frac{S_{11}}{S_{10}}\right)}. \tag{22}$$

In our design, a ratio of $R_{out}/R_C \approx 6$ is needed to achieve a good TC and, accordingly, cause $V_{out} \approx V_{out,optimal}$. Additionally, by changing the resistive ratio slightly, the temperature at which the TC is minimized can be shifted to a higher or lower value while still maintaining a good TC. Of note, our implementation utilized discrete off-chip resistors, limiting our ability to exactly achieve $V_{out,optimal}$, and the resulting TC was still low. Varying the resistor ratio is explored further in Section 4.

Next, we present a design procedure to obtain a low-TC, above-1 V voltage reference cell using the circuit of Figure 1.

1. Set $\frac{S_{11}}{S_{10}} \gg 1$, and choose a proper size for R_C to bias the current reference cell in subthreshold. Note that increasing $\frac{S_{11}}{S_{10}}$ will necessitate a larger R_C in order to bias the circuit in subthreshold, so area limitation requirements for the circuit can be used to set a maximum value of $\frac{S_{11}}{S_{10}}$.
2. Choose appropriate transistor aspect ratios such that $\frac{S_{14}}{S_{t1}S_{t2}} \geq 1$ and also that x and y keep all transistors in the subthreshold. These design choices make it possible to approximate Equation (10) with Equation (11).
3. Ensure that all transistor lengths are large enough to neglect the effects of channel-length modulation.
4. Choose the midpoint, T_0, of the desired temperature range, and use Equation (22) to solve for $y\frac{R_{out}}{R_C}$.
5. If the midpoint of the V_{out} vs. T curve is not at the desired location, then, according to Equation (22), we can adjust R_C to move T_0 to higher or lower temperatures. In addition,

R_{out} must be adjusted, accordingly, to keep the resistive ratio at a reasonable value, based on Equation (22).

4. Experimental Results

The voltage reference circuit of Figure 1 was fabricated using a standard 0.35 µm CMOS technology and operates on a 3.3 V supply. Table 1 provides details of the transistor sizes. A die photograph of this circuit is shown in Figure 3. The die area of this circuit, excluding the resistors, was 0.033 mm^2. The resistors (R_C and R_{out}) used in this circuit were off-chip resistors to allow for variety of R_{out}/R_C combinations. Using the design procedure of Section 3, we found that $R_{out}/R_C \approx 6$ for a low TC output. R_{out} and R_C were set to 3 MΩ and 500 kΩ, respectively, to achieve this ratio and to ensure subthreshold operation. These values were also chosen to minimize the TC around room temperature. If the resistors that we used in our experiments were integrated on chip, the die area would increase to 0.06 mm^2. Future implementations of this circuit would include on-chip resistors; basic trimming capabilities can be used to modify both the resistor values and resistor ratio to meet the required V_{out} and TC. One simple and conventional approach for trimming in a standard CMOS process is to create a series combination of smaller resistor values, each of which can be shorted out through digital selection to achieve the desired resistance.

Table 1. Device sizes used in our design.

Device (s)	Size
$M_1 - M_5$	5 µm × 1 µm
$M_6 - M_7$	20 µm × 20 µm
$M_8 - M_{10}$	4 µm × 2 µm
M_{11}	40 µm × 2 µm
M_{12}	20 µm × 20 µm
M_{13}	40 µm × 20 µm
M_{14}	4 µm × 20 µm
$M_{t1} - M_{t2}$	200 µm × 10 µm
C_S	3.1 pF

A Tenney TUJR environmental chamber was used to measure the performance of this circuit under varying temperatures; this environmental chamber has a temperature range of −75 °C to 200 °C. Figure 4a,b shows the measured V_{out} over temperature for multiple values of V_{DD}. Figure 4b shows that this circuit is able to achieve a low TC of 42 ppm/°C over the temperature range of interest (−70 to +85 °C). Even extending this temperature range significantly to cover from −70 to +125 °C, this circuit can still achieve a TC of 110 ppm/°C at the nominal V_{DD} = 3.3 V (see Figure 4a). By reducing V_{DD} to 1.7 V, the TC is 48 ppm/°C over this extended temperature range.

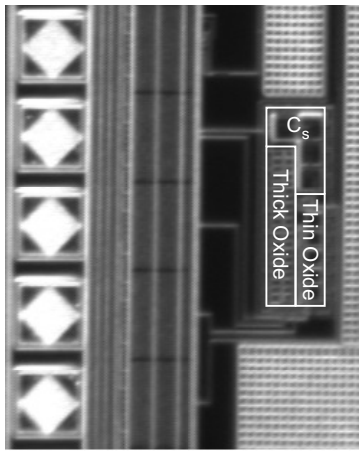

Figure 3. Die photograph of the proposed circuit. The single capacitor (C_s), the thick-oxide transistors, and the thin-oxide transistors are all delineated in this die photograph. The two resistors were included as off-chip components. The size of this voltage reference cell (excluding the resistors) was 300 µm × 110 µm.

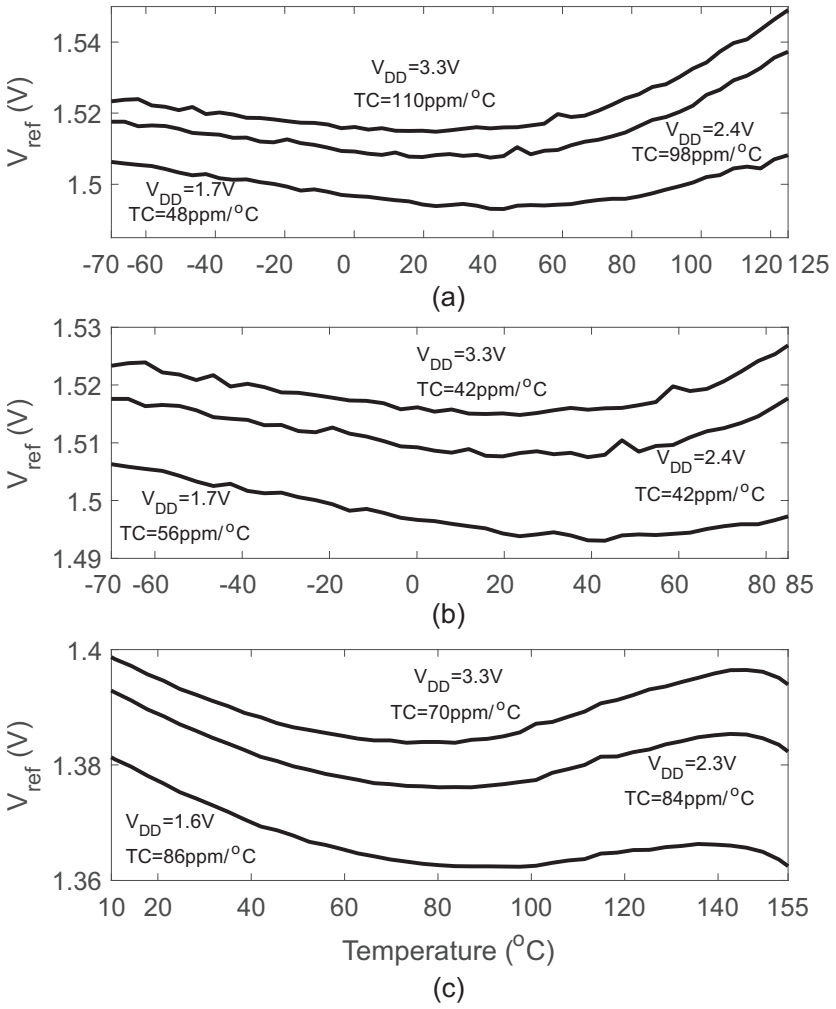

Figure 4. Measured TC of the proposed circuit under three different supply values for multiple conditions. (**a**) R_{out}/R_C = 3 MΩ/500 kΩ from −70 to +125 °C; (**b**) R_{out}/R_C = 3 MΩ/500 kΩ from −70 to +85 °C; (**c**) R_{out}/R_C = 2 MΩ/400 kΩ from +10 to +155 °C.

As discussed in the previous section, this circuit can be optimized to achieve a good TC for different temperature ranges. Figure 4c shows an example of shifting the midpoint of the temperature range to a higher value. This midpoint reference temperature can be increased by setting R_{out}/R_C to a smaller value and by also reducing the value of R_C, as is evidenced by Equation (18). In this example, R_C was reduced to 400 kΩ, which increases the temperature midpoint, T_0, due to the $\ln(\xi/R_C T)$ term. R_{out} was also decreased to 2 MΩ to keep the resistor ratio similar (but slightly smaller). The result is that the same circuit, with different resistor values, can be used to provide a low TC (70 ppm/°C at V_{DD} = 3.3 V) at higher temperatures (+10 to +155 °C). Under this condition, the output voltage was V_{out} = 1.395 V, and, if the resistors were integrated on-chip, then the area would be 0.044 mm^2.

The measured supply current versus temperature for these two reference voltages (V_{out} = 1.52 V, 1.395 V) under a 3.3 V supply is shown in Figure 5. The power consumption of this circuit at room temperature for the two R_{out}/R_C conditions were 1.11 µW (V_{out} = 1.52 V) and 1.34 µW (V_{out} = 1.395 V). Thus, this circuit is an appropriate choice for low-power applications.

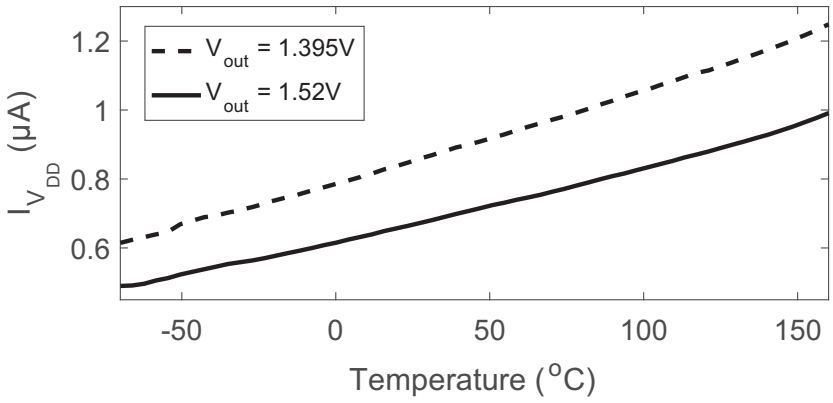

Figure 5. Measured supply current.

The line regulation of the circuit was measured at room temperature by sweeping the supply voltage from 0 V to 3.3 V, as shown in Figure 6. The line regulation for the two R_{out}/R_C conditions of Figure 4 were 10 mV/V (V_{out} = 1.52 V) and 9.3 mV/V (V_{out} = 1.395 V). The line regulation can be significantly improved by cascoding the PMOS transistors M_6, M_7, M_{12}, and M_{13} at the expense of a higher minimum supply voltage. Simulation results show that using a cascode structure would improve the line regulation to 2.88 mV/V and would only degrade the supply range by approximately 100 mV. The limited $V_{DD,min}$ of this circuit was due to the high output voltage of the circuit. In both R_{out}/R_C cases, $V_{DD,min}$ was approximately $V_{DD,min} \approx V_{out} + 200$ mV (and would be approximately $V_{out} + 300$ mV if cascoded PMOS devices were used to improve the line regulation).

The measured power supply rejection ratios (PSRR) at 100 Hz were −35 dB (V_{out} = 1.52 V) and −37.9 dB (V_{out} = 1.395 V). The PSRR values at 1 MHz were −44 dB (V_{out} = 1.52 V) and −44.8 dB (V_{out} = 1.395 V).

The die-to-die distribution of the DC output voltage was found at room temperature by measuring the average reference voltage (μ) and the standard deviation (σ) for 17 available chips. The coefficient of variation (σ/μ) for the 1.52 V and 1.395 V outputs were 2% and 1.76%, respectively.

Table 2 compares the three cases of our voltage reference circuit shown in Figure 4 to other similar circuits. Specifically, we compared our work to other circuits that (1) were fabricated; (2) were in a CMOS process; (3) have $V_{out} \geq 1$ V; and (4) have power consumption $\leq$50 µW. As can be seen from this table, our voltage reference circuit is able to provide a good balance of a low TC, low power consumption, and a large range of temperatures. Additionally, our circuit only uses devices available in standard CMOS processes (thicker-oxide I/O devices are now widely available), whereas some of the listed designs require non-standard devices [13,15].

Table 2. Comparison of the proposed work with other works.

	Process	Temperature Coefficient (ppm/°C)	Temperature Range	V_{REF}	Line Regulation (mV/V)	PSRR (dB)	V_{DD}	Power	Area (mm^2)	Comments
[8]	0.6 µm	14.36	[0 100]	1.2525 V	5.5	−42 dB @ 10 MHz	1.5∼2	40 µW	0.11	-
[9]	0.35 µm	12.85	[5 95]	1.2 V	28	−26.2 dB @ 100 Hz	1.75∼3.5	35.7 µW	0.0206	-
[13]	0.18 µm	8–73	[0 100]	1.25 V	0.31	−41 dB @ 100 Hz	1.4∼3.6	35 pW	0.0025	Native NFETs
[15]	0.18 µm	4.1	[−55 125]	1.1402 V	0.3	−54 dB @ 100 Hz	1.3∼2.6	11.18 µW	0.05	NPN BJTs
[19]	0.35 µm	215–394	[−20 80]	1.18V	4.5	-	1.3∼3.3	0.108 µW	0.21	-
[24]	0.25 µm	627	[20 50]	0.71–1.03 V	0.2	−51 dB @ 100 Hz	1.5∼3.5	0.12 µW	0.011	-
[25]	0.18 µm	147	[−40 120]	1.09 V	-	−62 dB @ 100 Hz	1.2∼1.8	0.1 µW	0.0294	-
[26]	0.18 µm	4	[0 100]	1.012 V	0.5	−66 dB @ 1 kHz	1.1∼1.8	21 µW	-	-
This work #1	0.35 µm	110 @ 3.3 V	[−70 125]	1.52 V	10	−44 dB @ 1 MHz	1.7∼3.3	1.11 µW	0.06	-
This work #1	0.35 µm	42 @ 3.3V	[−70 85]	1.52 V	10	−44 dB @ 1 MHz	1.7∼3.3	1.11 µW	0.06	-
This work #2	0.35 µm	70 @ 3.3 V	[10 160]	1.395 V	9.33	−44.8 dB @ 1 MHz	1.6∼3.3	1.34 µW	0.044	-

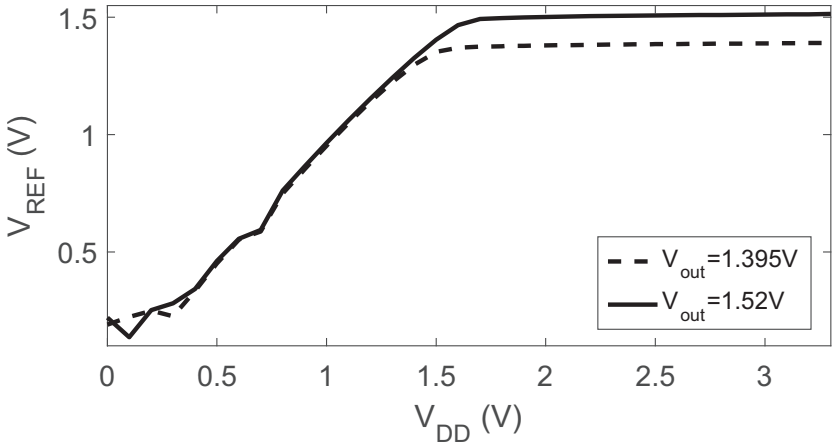

Figure 6. Measured line regulation.

5. Conclusions

A low power voltage reference cell for system-on-a-chip applications has been presented in this paper. This proposed cell uses a combination of thin-oxide and thick-oxide transistors to generate a reference voltage greater than 1 V with a low TC. We also presented a design methodology for how to translate this circuit to other processes and to provide a low-power and low-TC reference voltage.

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