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A Bond Graph Approach for the Modeling and Simulation of a Buck Converter

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Abstract: This paper deals with the modeling of bond graph buck converter systems. The bond graph formalism, which represents a heterogeneous formalism for physical modeling, is used to design a sub-model of a power MOSFET and PiN diode switchers. These bond graph models are based on the device's electrical elements. The application of these models to a bond graph buck converter permit us to obtain an invariant causal structure when the switch devices change state. This paper shows the usefulness of the bond graph device's modeling to simulate an implicit bond graph buck converter.

Keywords: Bond graph modeling; PiN diode; power MOSFET; buck converter

1. Introduction

A bond graph is a physics-based modeling tool that provides an energy-based topological framework for the modeling of physical systems [1]. It enhances the visual understanding of these systems through the visual indication of the cause and effect relationships of the energy transfer between the subsystem variables. A bond graph, as a powerful modeling tool, has known great development and enjoyed a well-deserved popularity in many engineering disciplines.

Regarding the power converter modeling discipline, recent research has begun to overcome the problem of switching and state discontinuities. In [2], a new bond graph element to represent an ideal switch was proposed. In this method, the switching operation is handled by sending, on a junction, zero flow when the switch is ON and zero effort when the switch is OFF. This method needs a reconfiguration of the causality whenever the position of the switchers changes. An extension of this method is the causality resistor technique [3] that suggests the addition of a resistor to the switch port. The adaptation of the causality of this resistor according to the ideal switch state leads to unchanged causality for the rest of the bond graph diagram. Other models use the modulated transformer (MTF) [4,5], where a modulation parameter m is set to 1 for the closed switch state and to 0 for the open switch state, but the causality must be reassigned. An extension of this technique [3], taking account of the resistance of the switcher during the ON mode, consists in combining a Ron resistor to the MTF to represent the non-linear characteristics of the switcher. This method allows for the definition of a single bond graph model that holds for all switch positions. Another method that implies invariant causalities during the different switch modes is the switched power junction [5]. Here, more than one bond can decide the effort at a 0-junction and the flow at a 1-junction at mutual time instants. These techniques, however, do not show the dynamic internal comportment of the switch devices during their switching mode. In this respect, there are some works [6–8] where the authors developed new switcher component models based on the bond graph formalism for a better modeling of the internal physical behavior of these devices. In this paper, we present the dynamic models, by a bond graph formalism, of the power MOSFET transistor and the PiN diode and their

application in a buck converter circuit. The use of these switcher models leads to unchanged causality during the different transition states, and to a better simulation of the dynamic comportment of the buck converter and the switcher devices.

To analyze the transfer of energy and the performance in a converter system against input or load changes, a PWM regulator block is always used. Therefore, the bond graph package was developed in the VHDL-AMS language. This is to design bond graph schema mixed with digital control blocks. This package was integrated into the graphical modeling tool SystemVision in order to explore rapid prototyping and the visual design facilities.

VHDL-AMS is a new mixed-signal modelling language based on the VHDL language. It is designed to support mixed-signal systems that contain digital elements and analog elements and to allow the interaction between them. It allows for hierarchy description and the simulation of continuous and discrete events [9,10].

This article is organized as follows. Section 2 introduces the bond graph theory. Section 3 describes the buck bond graph design methodology using a power MOSFET and a PiN diode bond graph sub-model. Section 4 presents the simulation results. Finally, the last section provides some conclusions and suggestions for future work.

2. The Bond Graph Theory

A bond graph is an engineering tool based on the description of physical systems by analyzing the exchange of energy within [1]. This exchange determines the dynamic behavior of the systems. Bond graph modeling involves devices, their connections, directed power transfers, and causality strokes. The power or the energy flow is represented by a half arrow called a power bond. Each bond is associated with two variables: effort and flow. The direction of the flow variable is given by the causality information. Graphically, the causality is indicated by putting a stroke near the element which controls the flow as shown in Figure 1.

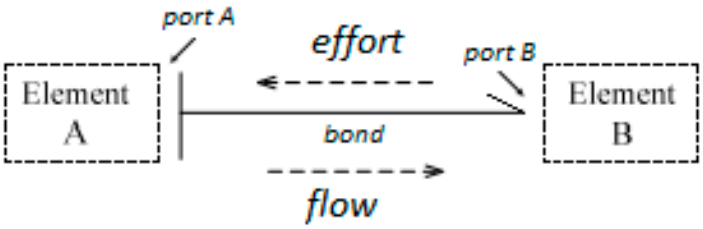

Figure 1. The general conventions of bond causality.

The energy flow in a system is described at any time by the value of the power, which is the product of the effort variable by the flow variable. Therefore, a bond graph can represent systems from different domains in a unified way. Table 1 shows the effort and the flow variables of the main physical domains.

Table 1. Effort and flow variables of the main physical domains.

Physical Domain	Flow Variable	Effort Variable
Electrical	Current	Voltage
Mechanical	Velocity	Force
Hydraulic	Volume flow	Pressure
Thermal	Entropy flow	Temperature

3. The Buck Bond Graph Model

The buck converter to simulate is pictured in Figure 2. It consists of a switch-regulated buck converter, where the values of its components have been chosen as: voltage E = 9 Volts, L = 50 µH, C = 50 µF, and R = 4 Ohms. The switcher Sw1 represents the power MOSFET IRF740 and Sw2 represents the PiN diode STTA81200. In this example, the buck converter is chosen to operate in continuous conduction mode.

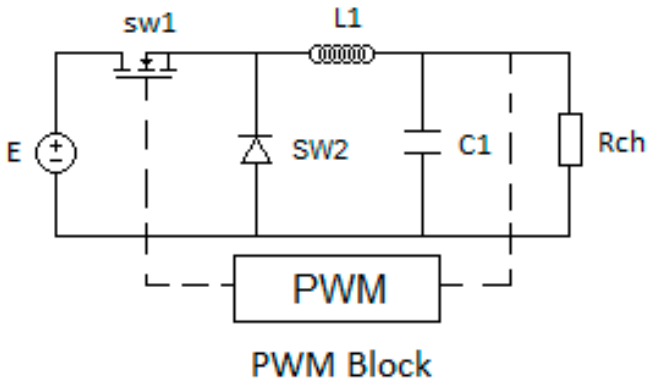

Figure 2. Circuit diagram of the regulated buck converter.

To derive the buck bond graph schema, we designed the switchers' bond graph sub-model and added them to the buck bond graph model with respect to the sequential causality assignment procedure.

3.1. Power MOSFET Bond Graph Sub-Model Description

Figure 3 shows the cross-section of the power MOSFET (VDMOS). The basic electrical components to satisfy its dynamic behavior are [11]:

- The capacitances C_{ds}, C_{gd} and C_{gs} that simulate the drain-source, gate-source, and gate-drain capacitances, respectively;
- The resistances R_d, R_g and R_s that represent the equivalent resistance of the drain, gate, and source, respectively;
- The resistance R_{ds} that represents the total resistance between the drain and the source (the body-drain diode); and
- The controlled current source Ids, whose associated equations are:

$$I_{ds} = 0 if\ V_{gs} < v_t \tag{1}$$

$$I_{ds} = k_{psat} \frac{(V_{gs} - v_t)V_{ds} - \frac{k_{plin}{V_{ds}}^2}{2k_{psat}}}{1 + \theta(V_{gs} - v_t)} if\ V_{ds} \leq (V_{gs} - v_t)\frac{k_{psat}}{k_{plin}} \tag{2}$$

$$I_{ds} = k_{psat} \frac{(V_{gs} - v_t)^2}{2(1 + \theta(V_{gs} - v_t))} if\ V_{ds} > (V_{gs} - v_t)\frac{k_{psat}}{k_{plin}}. \tag{3}$$

Therefore, an equivalent bond graph model for the power MOSFET can be derived from these basic components.

To derive the bond graph model of the power MOSFET, we used the 0-junction to represent the Kirchoff's current law (the 0-junction is inserted at each node and between elements that have the same potential) and the 1-junction to represent Kirchoff's voltage law (the 1-junction is inserted between the 0-junctions). For the assignment of the causality (Figure 4), we applied the sequential causality assignment procedure [1] in order to transfer the effort value (that is the voltage) from the drain and

the source to the flow source element Ids. The value of the effort V_{gs} used on the flow source Ids is obtained from a voltage-to-quantity converter, placed at the gate bond, via an information link. Table 2 shows the values of the Power MOSFET IRF740 parameters.

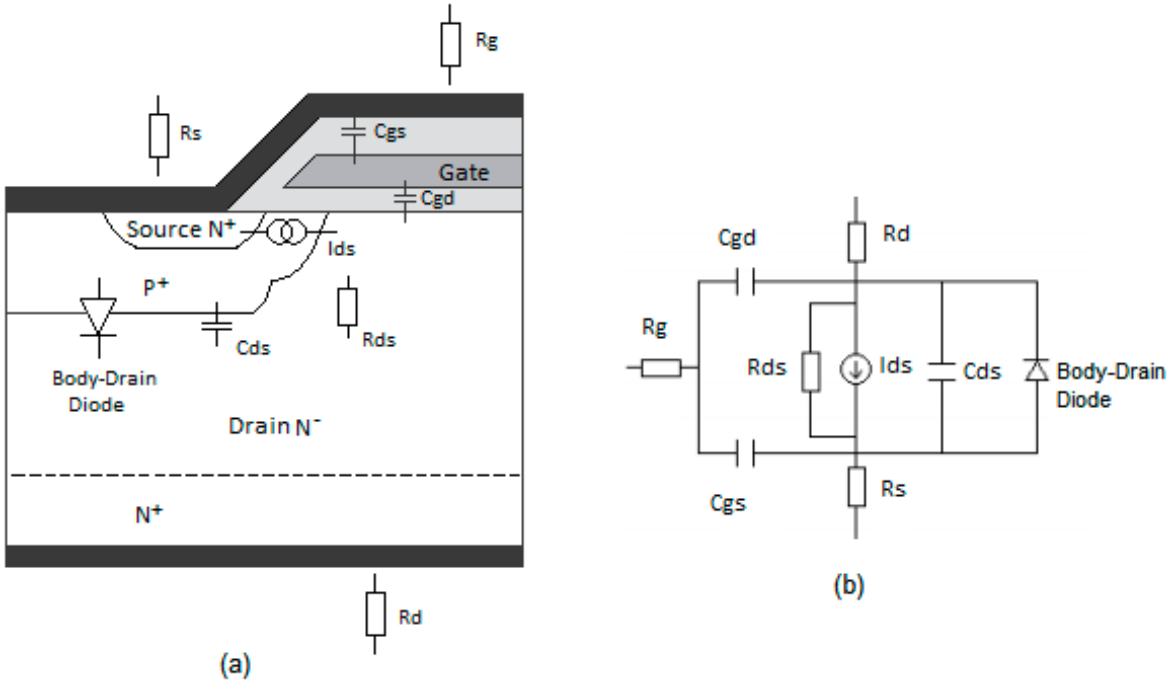

Figure 3. (**a**) Cross-Section of Power MOSFET showing the principal electrical elements; (**b**) equivalent electrical schema of the Power MOSFET.

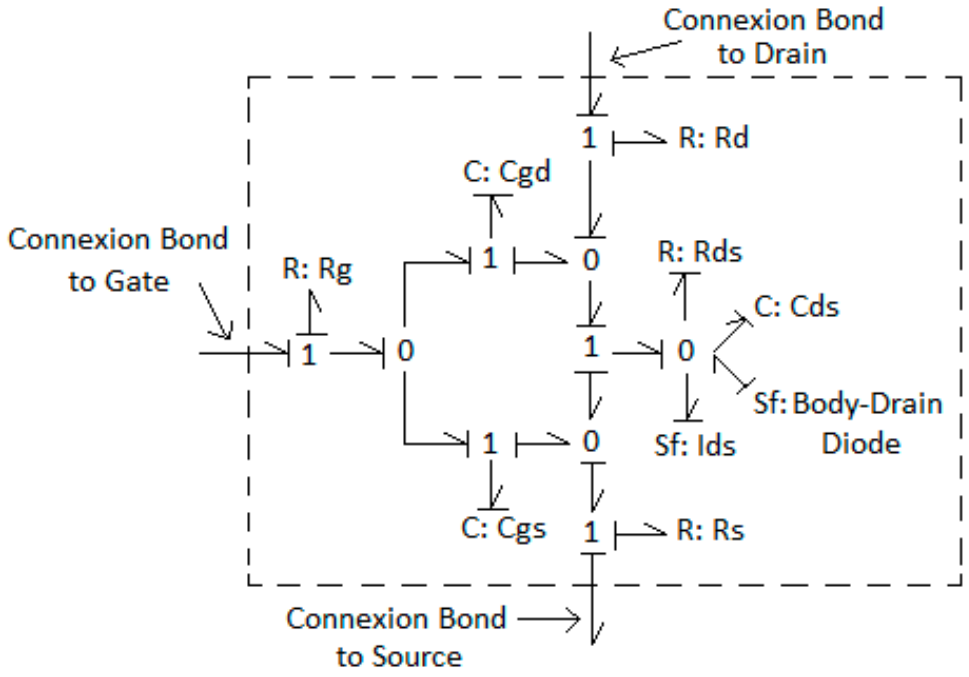

Figure 4. Bond graph sub-model of the power MOSFET.

Table 2. The Power MOSFET IRF740 Parameters.

Parameters	Description	Values	Unity
T_{eta}	Transverse electric field factor of the MOSFET	3.5	V^{-1}
K_{plin}	Linear transconductance	9.0	A/V^2
K_{psat}	Saturation transconductance	15.0	A/V^2
v_t	Threshold voltage	3.5	V
R_d	Equivalent resistance of the drain	0.02	Ω
R_s	Equivalent resistance of the source	0.038	Ω
R_g	Equivalent resistance of the gate	0.09	Ω
R_{ds}	Resistance between the drain and the source	1.5×10^6	Ω
C_{ds0}	Drain-source capacity at zero level polarization	5.2×10^{-9}	F
I_{s0}	Saturation current of the body-drain diode	4.0×10^{-9}	A
P_B	Potential of the MOSFET base	0.8	V
M_J	Gradient coefficient	1.0	–
N_B	Concentration in the MOSFET base	5.4×10^{21}	m^{-3}
C_{oxd}	Gate oxide capacity	0.045×10^{-9}	F
A_{gd}	Equivalent surface of the gate-drain area	4.0×10^{-6}	m^2
C_{gs}	Grid-source equivalent capacity	0.4×10^{-9}	F

3.2. PiN Diode Bond Graph Model Description

The Pin diode consists of a wide and lightly doped central region delimited by two generally much thinner and more highly doped lateral regions P^+ and N^+ (Figure 5). To model the dynamic comportment of the PiN diode, we use the following electrical components [12]:

- The current junction source I_j defined by the following equation:

$$I_j = I_{se}\left[exp\left(\frac{2V_e}{U_t}\right) - 1\right] \tag{4}$$

  where V_e is the junction voltage and U_t is the thermal voltage.
- The current base source I_b, whose relations are as follows:

$$I_b = \frac{q_e - q_b}{T_M} \tag{5}$$

  where q_e is the injected charge level at the junction and q_b is the total charge in the central region, where:

$$q_e = I_s tau\left[exp\left(\frac{V_e}{U_t}\right) - 1\right] \tag{6}$$

  and

$$\frac{dq_b}{dt} = I_b - \frac{q_b}{tau}. \tag{7}$$

- The voltage base source V_b, equal to:

$$V_b = \frac{U_t\ T_M\ R_{M0}\ I}{q_b\ R_{M0} + \ U_t\ T_M}. \tag{8}$$

- The junction capacitance C_j
- The equivalent resistance R_s

Based on the same procedure used in the case of the power MOSFET, we can derive the bond graph PiN diode sub-model as represented below in Figure 6. The parameters of the PiN diode STTA81200 are reported in Table 3.

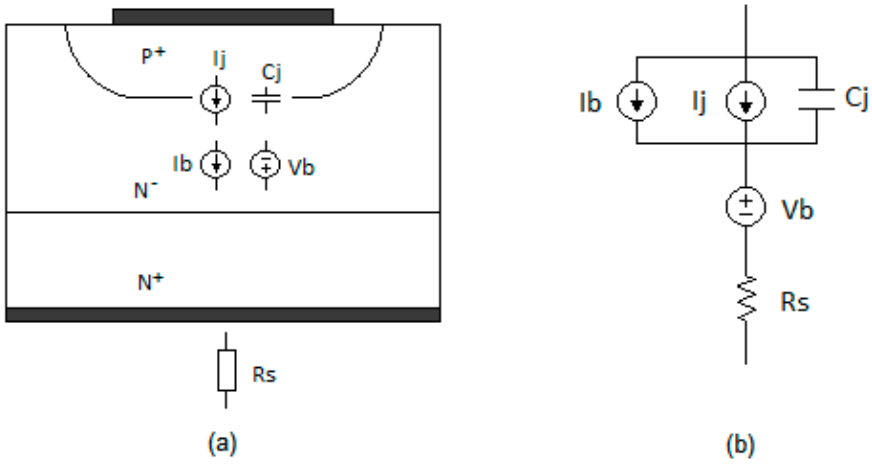

Figure 5. (**a**) Cross-Section of PiN diode showing the principal electrical elements; (**b**) equivalent electrical schema of the PiN diode.

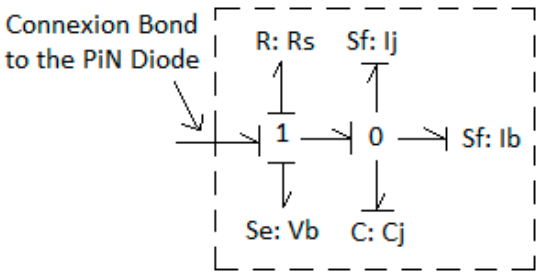

Figure 6. Bond graph sub-model of the PiN diode.

Table 3. The PiN diode STTA81200 Parameters.

Parameters	Description	Values	Unity
R_s	Serial resistance	30.0×10^{-3}	Ω
I_{se}	Recombination current	1.0×10^{-23}	A
T_M	Carriers transit time	8.2×10^{-9}	ns
T_{AU}	Carriers lifetime	1.3×10^{-7}	ns
R_{M0}	Initial resistance	0.1	Ω
M	Gradient coefficient	0.55	–
C_{j0}	Junction capacitance	3.0×10^{-9}	F
I_s	Saturation current	1.0×10^{-12}	A

3.3. Derivation of the Buck Bond Graph Model

By applying the bond graph sub-model of the power MOSFET transistor and the PiN diode, and with respect to the sequential causality assignment procedure, the resulting buck bond graph model is as shown in Figure 7.

The implementation of the power-MOSFET, PiN diode, and the buck bond-graph model in SystemVision is achieved via the graphical and user-friendly interface (Figures 8–10). In SystemVision, the designer can draw the bond graph model on the screen by using the basic bond graph library written in the VHDL-AMS language. For more information about the combination of bond graph theory and mixed language programming, the reader can refer to [13–15], and [15–17] for more detail about the implementation of the basic bond graph elements in VHDL-AMS.

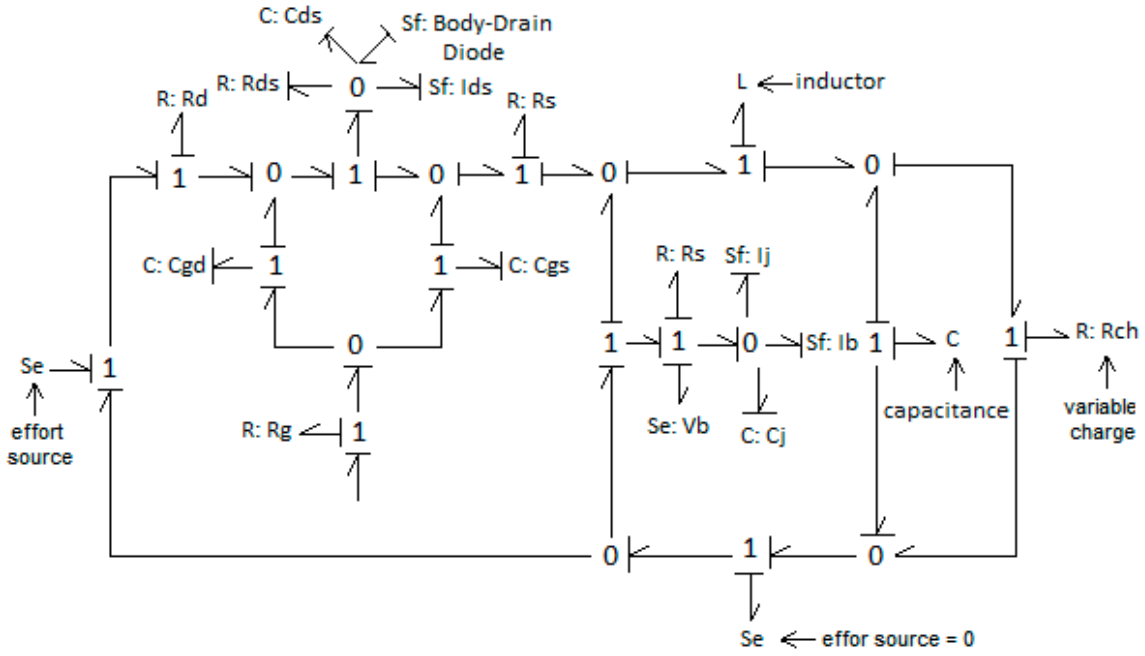

Figure 7. Bond graph buck converter schema.

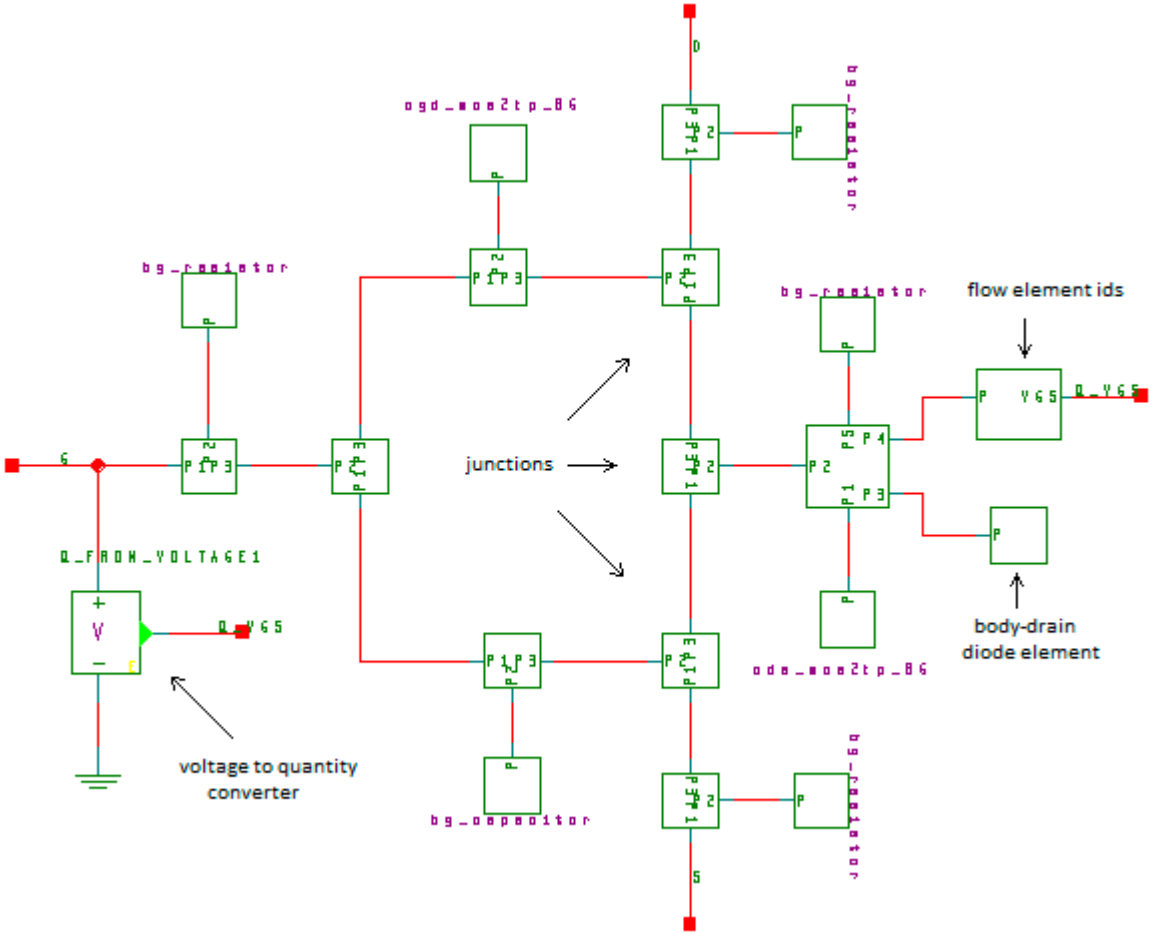

Figure 8. Implementation of the power MOSFET bond graph sub-model in SystemVision.

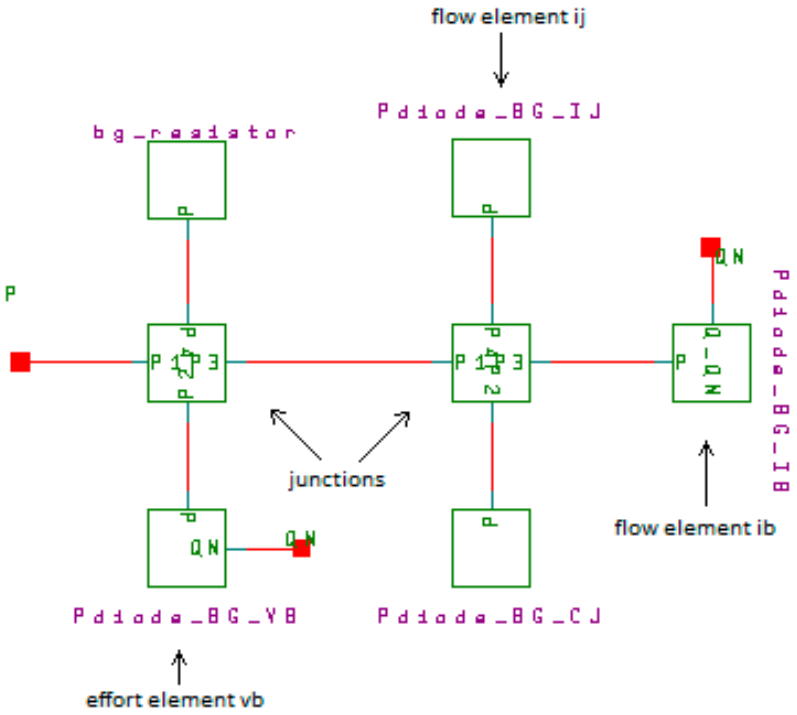

Figure 9. Implementation of the PiN diode bond graph sub-model in SystemVision.

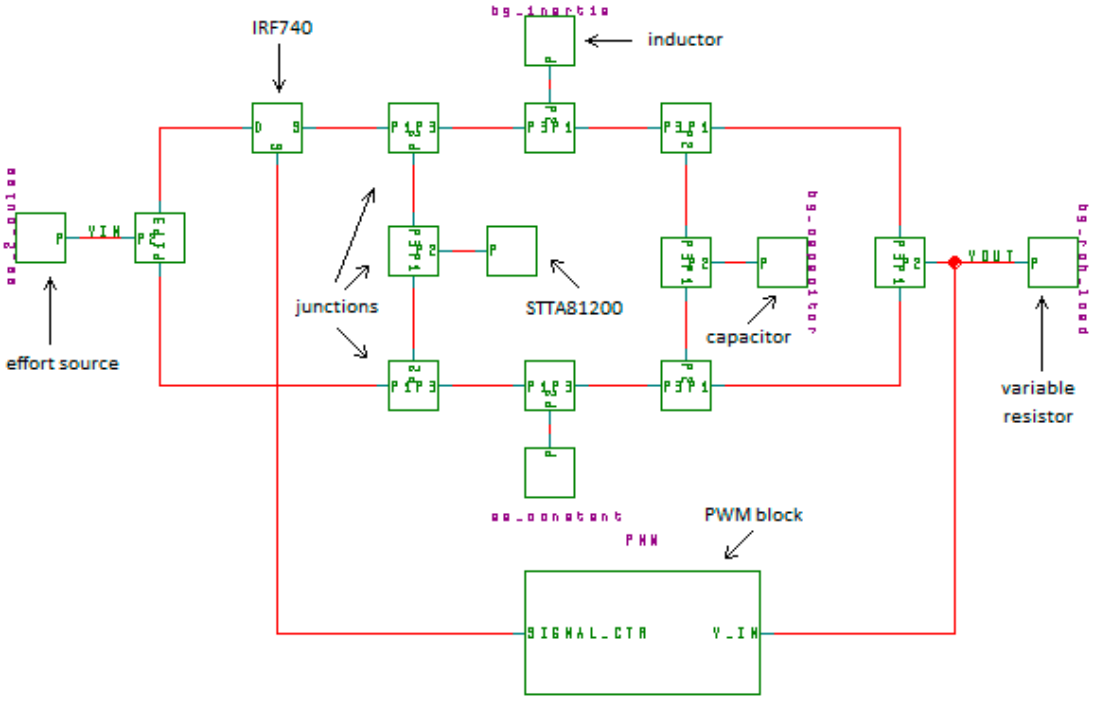

Figure 10. Screen of SystemVision showing the buck bond graph model.

4. Simulation Results

The simulation results of the bond graph buck model are displayed in Figures 11–13. To show the output voltage regulation, we perturbed the input voltage (Figure 11) and the resistive charge (Figure 12) at various times during the simulation. As a result of these perturbations, we can see that the output voltage is regulated to the reference voltage (4.5 V). In Figure 13, we can see the inverse

current of the PiN diode during its reverse recovery. Therefore, the simulation results of the bond graph buck model present satisfactory switching operation results.

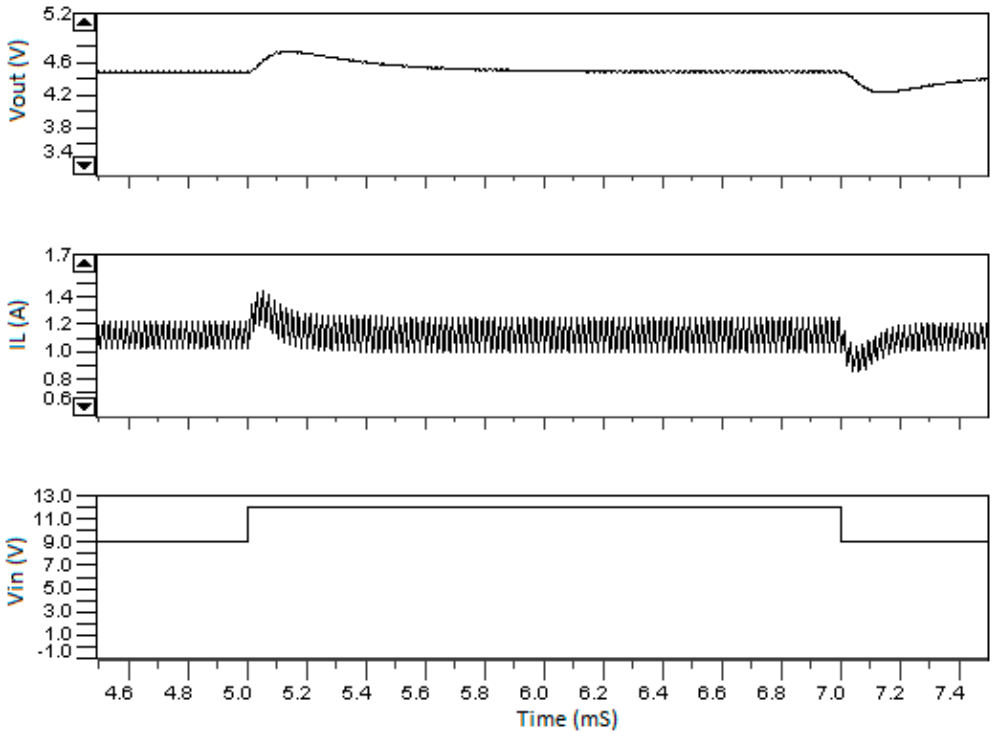

Figure 11. Time evolution of the output voltage Vout(t) and the inductor current IL(t) during the Vin(t) jump and drop with an amplitude of 3 V at t = 5 ms and t = 7 ms.

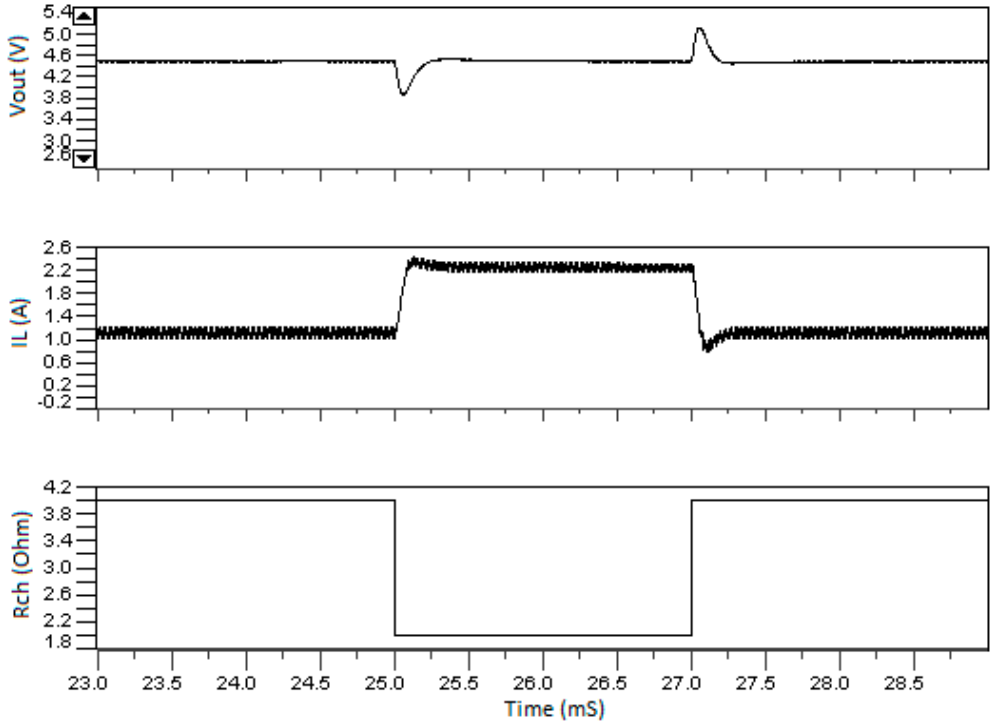

Figure 12. Time evolution of the output voltage Vout(t) and the inductor current IL(t) during the R load drop and jump from 4 ohm to 2 ohm at t = 25 ms and back to 4 ohm at t = 27 ms.

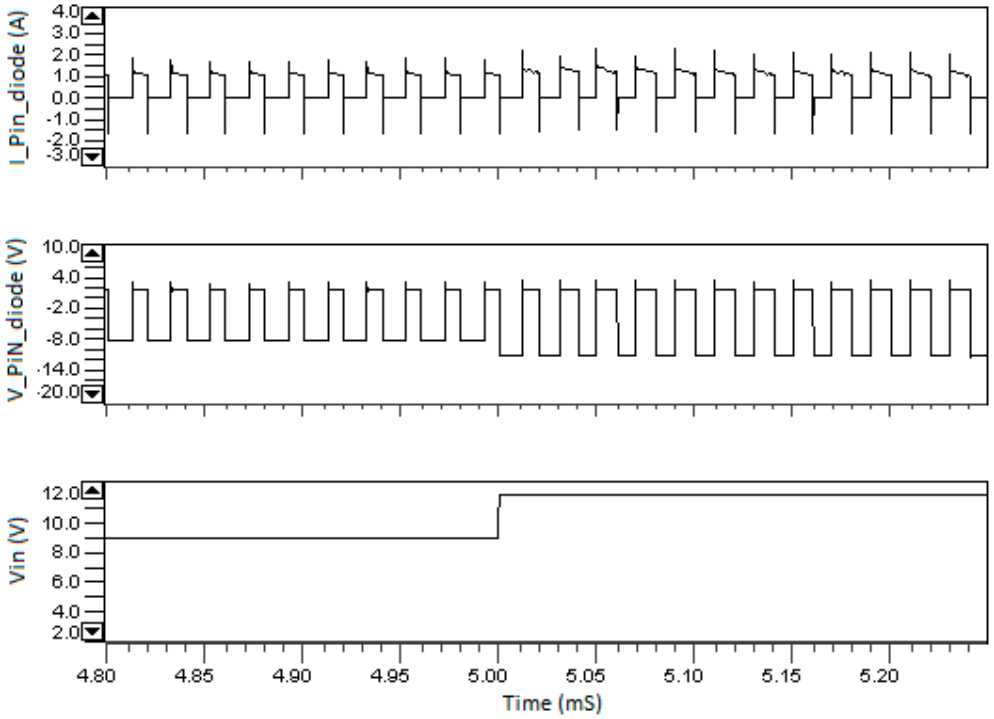

Figure 13. Time evolution of the STTA81200 voltage and current during the Vin(t) jump with an amplitude of 3 V at t = 5 ms.

In addition, the bond graph buck model operates at the different switching modes without any modification on the model schema. Therefore, the use of a bond graph sub-model, based on the electrical components for the switcher devices, provides an unchanged causality of the buck bond graph schema for the different switching states. The commutation of the switcher devices is ensured mainly through the controlled flow element Ids for the power MOSFET IRF740 and the controlled flow elements I_j and I_b for the simple diode STTA81200.

5. Conclusions

In this paper, we present a methodology using the unified formalism of a bond graph to model a buck converter circuit. This approach allows us to model a bond graph buck converter very well at all switching modes. Thus, the use of a bond graph sub-model, based on the electrical elements for the switcher devices, allows for the maintenance of a causality invariant.

The design of the buck converter is realised using a bond graph package developed in the VHDL-AMS language and under the SystemVision environment. This is to achieve a rapid prototyping of the target design and to explore the graphics facility.

In future work, we will add the thermal effect within the switcher devices.

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Author Contributions: Rached Zrafi is the main author of the paper. Sami Ghedira and Kamel Besbes was responsible for the supervising of the paper.

Conflicts of Interest: The authors declare no conflict of interest.

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