Journal of
Low Power Electronics and Applications

MDPI

Article

The Design and Implementation of a Low-Power Gating Scan Element in 32/28 nm CMOS Technology

Mahshid Mojtabavi Naeini [1], Sreedharan Baskara Dass [2] and Chia Yee Ooi [1,*]

[1] Department of Electronic Systems Engineering, Malaysia-Japan International Institute of Technology Universiti Teknologi Malaysia, Jalan Sultan Yahya Petra, 54100 Kuala Lumpur, Malaysia; ma.mojtabavi@gmail.com

[2] Integrated Circuit Engineering, 14387, Taman Paik Siong, Batu 71/2, Jalan Puchong, 47180 Puchong, Selangor Darul Ehsan, Malaysia; sree@icesb.com

* Correspondence: ooichiayee@utm.my; Tel.: +60-127823819

Academic Editor: Tony Tae-Hyoung Kim
Received: 22 November 2016; Accepted: 27 March 2017; Published: 28 April 2017

Abstract: Excessive power consumption during test application time has severely negative effects on chip reliability since it has an inevitable role in hot spots that appear, degradation of performance, circuit premature destruction, and functional failures. In scan-based designs, rippling transitions caused by test patterns shifting along the scan chain not only elevate power consumption in the scan chain but also introduce spurious switching activities in the combinational logic. In this work, a new low power gating scan cell for scan based designs has been proposed in order to reduce power consumption in the scan chain as well as the combinational part during shifting. We have modified the conventional scan cell and augmented it with state preserving and gating logic that enables an average power reduction in combinational logic during shift mode. The new scan cell mitigates the number of transitions during shift and capture cycles. Thus, it reduces the average power consumption inside the scan cell and as a result the scan chain during scan shifting with a low impact on peak power during the capture cycle. Furthermore, due to introducing a new shorter shift path, improvements are observed in terms of propagation delay and power consumption in the scan chain during shifting. This leads to higher feasible shift frequency whereby the shift frequency is limited by the maximum power budget and hence results in reducing the test application time. The post-layout spice simulation results show a 7.21% reduction in total power consumption, an average 12.25% reduction of shift power consumption, and a 50.7% improvement in the clock (CLK)-to-shift propagation delay over the conventional scan cell in Synopsys 32/28 nm standard CMOS technology.

Keywords: switching activity; scan cell; gating logic; shift power; peak power; design for testability

1. Introduction

The most major concerns regarding challenges to test current high integration density circuits are the test cost and test power. On one hand, product quality requires the execution of high quality manufacturing tests and diagnostics. Such a high quality test procedure can elevate the test application time that results in high test cost. The standard scan is one of the most widely employed design-for-testability (DFT) approaches that offers a high quality test procedure by providing controllability and observability on every single storage element in the circuit-under-test (CUT). Unfortunately, scan-based architectures are very expensive in terms of power, as each scan test pattern contributes to a shift operation with high power consumption [1]. Power consumption during testing is significantly higher than that during the normal operation. Since there is less correlation between scan test vectors generated by an Automatic Test Pattern Generation (ATPG) tool compared to the data

during normal mode, high switching activities incurred in capture mode have increased the test power drastically over the chip power threshold. On the other hand, high test power consumption not only increases the test cost, but also may cause reliability hazards or even instant damages [1]. Reducing the switching activities at any instant of time mitigates the average power and hence the peak power of the chip [2]. Moreover, the peak power and average power reduction during testing contributes to enhanced reliability of the test and improvement of the yield [3].

In this paper, a novel low power gating scan cell for shift power reduction considering both the scan chain and combinational part with the following features is presented:

- Gating redundant transitions from the scan cell to combinational logic during shift mode.
- Reducing switching activity inside the scan cell during shift mode.

In order to achieve the above mentioned features within an integrated structure, we have modified the slave latch in the conventional master/slave scan cell with state preserving and gating abilities. The proposed gating scan architecture introduces a new short shift path that improves both shift and capture propagation delays as well as power consumption in the scan chain during shift mode. This makes shifting at higher frequency possible in those cases where the maximum shift frequency has been bounded by the maximum allowable power consumption. Therefore, the proposed gating scheme improves the test application time over existing gating solutions.

Since state preserving and gating logics have been embedded as part of the slave latch in the proposed gating scan cell, the area overhead is as low as two transistors that are sharable by several scan cells. The proposed structure contributes to the average power reduction in the scan architecture (combinational logic and scan chain) during shift mode while not causing high peak power during capture mode. In gating methods, the main source of excessive peak power during capture mode is the switching activities in the gating elements when the mode changes from shift to capture mode or vice versa. Excessive peak power can be avoided by reducing the level of switching activity during testing [4]. Therefore, the proposed structure is able to control the peak power violations by reducing the switching activities in other parts of the scan cells. The presented paper is organized as follows. Section 2 provides a background overview in the context of power definitions and the corresponding evaluation models in low power testing. Section 3 reviews the state of the art hardware-based test power reduction techniques. In Section 4, the proposed low power gating scan cell is presented and its function is elaborated. Section 5 discusses the experimental results and comparative analysis. Section 6 outlines future evaluations at the circuit level. Finally, Section 7 concludes the presented work.

2. Power Estimation in Digital VLSI Circuits

Regardless of short-circuit power which is consumed due to the short-circuit current flows between the supply voltage and ground during the slice time when all of the gate inputs are active, dynamic power is consumed during the charging and discharging of the output and internal nodes capacitance, which can be given by Equation (1):

$$P_{dyn} = P_{dyno} + P_{dynj} = \frac{1}{2} f(V_{DD}^2 \sum_i (\alpha_i \cdot C_{Li}) + V_{DD} \sum_i \sum_j (\alpha_{ij} \cdot C_{ij} \cdot V_{ij})) \quad (1)$$

where, P_{dyno} and P_{dynj} correspond to the dynamic power consumption at the output load capacitance and the internal nodes capacitance, respectively. The switching activity at gate i output and that at the *j*th internal node of the *i*th gate are represented by α_i and α_{ij}, respectively. V_{ij} corresponds to the voltage swing which is generally equal to VDD-Vth. Finally, C_{Li} and C_{ij} are used for gate i load capacitance and the *j*th internal capacitance at gate i.

The average power consumption is the total energy consumption divided by the test time. This parameter is even more important than the energy as hot spots and reliability problems may be caused by constantly high power consumption.

The average power consumed during the test session is presented by Equation (2), where T is the clock period and L is the total number of clocks during the test phase [5].

$$P_{average} = E_{total}/(L \cdot T) \quad (2)$$

The peak power consumption corresponds to the highest amount of power consumption during one clock cycle. If the peak power exceeds the circuit power threshold for several clock cycles, the correct function of the entire circuit is no longer guaranteed. Peak power can be expressed as follows [5]:

$$P_{peak} = Max\ P_{inst}(V_k) = Max_k\ (E_{vk}/t_{small}) \quad (3)$$

where, $P_{inst}(V_k)$ (instantaneous power) determines the amount of power consumed during a small instant of time t_{small} after the application of the test vector V_k. E_{vk} corresponds to the energy consumed in the circuit after application of successive input vectors (V_{k-1},V_k).

3. Overview of Hardware-Based Test Power Reduction Approaches

A significant number of techniques that attempt to reduce power in the combinational part or scan chain during the test application time fall into the category of hardware-based approaches. The hardware-based approaches require additional hardware to be added into the design, and are easy to be integrated with different embedded compression techniques [6]. Clock gating is one of the well-known power reduction techniques in the wide range of hardware-based methods [7–11]. The methods proposed in [7,8] offer an algorithm for constructing an activity-sensitive clock tree that combines nodes with the same activity pattern to disconnect the clock signal efficiently. However, Shen et al. [9] have shown that merging nodes only based on the identical activity pattern may result in more transitions of the control signal. Thus, this offsets the power savings obtained by clock gating. The approach in [10] divides the scan chain into two partitions (odd and even scan cells) and uses two separate clocks for each partition. At any time instant, only one partition is active so that the peak and average power during the scan period is reduced by a factor of two. The major disadvantage of this approach is that by increasing the scan cells derived by each clock control signal, the elevated delay may make it difficult to meet the timing closure. A partial clock gating algorithm has been proposed in [11]. Since generally only a portion of scan cells participate in response capturing, a gated clock controller selectively gates the inactive scan cells during the response capture cycle. However, the power saving has been limited only to the response capture cycle at the cost of a high complexity clock gating controller. The clock skew problem in the normal mode of operation is the main disadvantage of the clock gating technique. In addition, a high complexity clock controller circuit turns out to be another drawback for this category of hardware-based approaches.

The method that aims to minimize switching activity in the scan chain through re-ordering the scan cells in the scan chain is proposed in [12–18]. In [18], a weighted graph comprised of scan cells as the graph vertices and the number of transitions between two adjacent cells for a specific sequence of test patterns as the edges of graph was introduced. The non-deterministic polynomial-time (NP)-hard problem of finding the lowest transition cost arrangement via the lowest cost Hamilton path has been solved by a greedy algorithm. However, constructing a graph for high density circuits with a large number of test vectors is very time consuming. Generally, the scan cell re-ordering techniques are known as high computational complexity approaches that limit their applicability. Furthermore, they may raise the scan routing congestion problem and have higher silicon area.

Another approach known as scan partitioning splits the scan chain into multiple partitions and activates only one partition at any time interval [3,19–25]. The partitioning scheme in [19] limits the scan chain transitions from propagating to combinational logic during shifting by activating only one scan path at any time interval. Bhunia et al. in [20] has utilized the previous partitioning approach on the first level supply (FLS) gating approach that extends the partitioning to capture cycle as well. To mutually exclusively activate each segment, several clock cycles, both in shift and capture mode,

are required which results in a higher test application time. Both of these techniques introduce a high area penalty due to using high complexity controlling circuits. A segment regrouping algorithm has been proposed by Yamato et al. in [23] which identifies an optimal combination of scan segments to be clocked simultaneously and results in further instantaneous shift power reduction in the scan chain. Methods in [24,25] employ a scan chain grouping technique where only a single scan chain in each group is activated at any time during shift-in and shift-out cycles, and all other scan chains are disabled. Thus, repeated shift-in (shift-out) cycles are required to load the test data (or to shift-out the response data). In the operational mode, test responses are captured in all the chains during the capture cycle. These techniques, except [20], aim to reduce the amount of switching in the scan chain and cannot completely prevent redundant power loss in the combinational logic [20]. The drawbacks of the scan chain partitioning approaches are: 1. They result in test time complexity increase; 2. They may cause data dependency problems; 3. They are depending on complicated control circuits for the activation of the proper partition at the right time; thus, they are expensive in terms of area; 4. Although significant achievement in test power reduction has been gained due to scan chain reordering and partitioning techniques, none of the solutions within this category have completely eliminated spurious switching activities in the combinational logic during shift mode.

One of the most straight-forward methods for shift power reduction is to reduce switching activity in the combinational logic by isolating the stimulus path of scan cells from combinational logic during the shift cycle, since the major source of dynamic power in CUT is the propagation of ripple transitions from the scan cells to the combinational logic during scan shifting. These methods are less intrusive to the original designs compared with the aforementioned approaches, and they are independent of the test set. However, they may degrade the performance due to the inserted logic between the scan cells' stimuli paths and the combinational part. Moreover, depending on the added logic, the high area penalty is avoidable. In [26,27], the authors reported gating the stimulus paths of flip-flops by tying the path to a constant logic '1' or '0' through utilizing gating logic (NOR [26], transmission gate (TG), together with a pull-up or a pull-down transistor [27]) at the scan cells' output, and thus eliminated spurious switching in logic gates. However, depending on the logic on the scan cell output, they still may not be able to block all switching from propagating to the combinational logic in the beginning of the shift cycle if the logic on the scan cell output differs from the gating logic. Thus, the unblocked transient can still propagate to the deeper level of the combinational logic, causing many transitions at circuit internal lines before reaching the steady state.

Approaches in [28,29] exercised gating logic (multiplexer (MUX) [28], extra inverter-based latch [29]) to hold the scan output at the previous logic and completely blocks any redundant switching activity in the combinational logic during the shift mode. An enhanced scan structure has been reported in [30] for delay fault testing. In this method, each scan cell has been augmented into an AND-NOR-based hold latch at the scan cell output to ensure that the scan stimulus paths remain unchanged during the shift session. The hold latch has been implemented by a cross-coupling of NOR and two AND gates to hold the scan cells' stimulus paths. However, these approaches suffer from large overhead in terms of area and propagation delay. The first level supply (FLS) gating scheme proposed by Bhunia et al. [31] inserted a common pull-down gating transistor to the gates at the first level of logic which are typically connected to the scan chain outputs. In order to prevent the outputs of the first level gates from floating, they have added another pull-up transistor to force the output to VDD. The FLS scheme has less overhead in terms of area, propagation delay, and even switching activity in gating logic compared with the other gating schemes. However, it is unable to block all transients in the combinational logic in the first shift cycle because the output of the first level gates are forced to a fixed value, which is similar to the NOR and TG gating approaches. Bhunia et al. [32,33] gives an alternative solution for the Enhanced Scan in delay fault testing named First Level Hold (FLH), which gates the rippling transition to the combinational logic during the shift mode. All of the mentioned techniques can reduce shift power in combinational logic effectively. However, they suffer

from large overhead in terms of area and propagation delay. Another modified scan flip-flop for low power delay fault testing has been proposed in [34].

As shown in Figure 1, it bypasses the slave latch with an alternative low cost dynamic latch in the scan shifting path. Therefore, it can successfully eliminate all transitions to the combinational logic during shift mode. However, there is no improvement in the level of power consumption inside the scan cell and as a result in the scan chain.

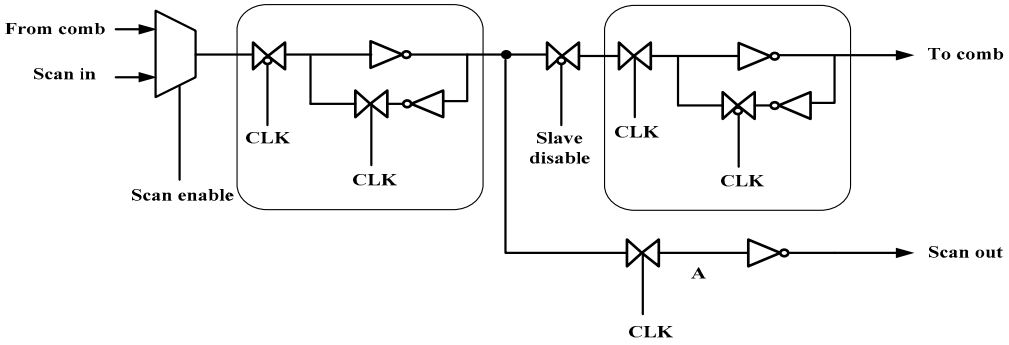


Figure 1. Modified scan flip-flop for low power delay fault testing [35].

Partial gating methods [35–39] have been proposed to reduce the full gating penalties in area overhead and performance degradation. By having the proper selection of scan cells on non-critical paths to be gated and their gating values, they try to maximize the shift power reduction with acceptable performance degradation. The most recently reported partial gating methods such as those in [6,40–42] gate a sub-set of scan cells not only during shift mode but also during capture mode in order to reduce peak power in addition to shift power reduction. However, in large industrial designs, scan cells have large fan out cones. Thus, un-gated scan cells in the partial gating method can still cause a great amount of switching activities in the combinational logic. Moreover, in both existing full gating and partial gating techniques, significant power is consumed in the gating elements themselves, which causes the peak power to increase from 5% to 60% in all the benchmark circuits when the gating overhead was considered [34]. This is due to the large switching activity occurring in the gating logic when the scan mode changes to capture mode or vice versa [43]. The missing part of both existing full gating and partial gating methods is that they have limited their approaches only to power reduction in combinational circuits during shift cycles without highlighting that shift power consumption is also related to the total amount of power consumed in the scan chain besides combinational logic.

4. Proposed Low Power Gating Scan Cell

During the shift cycle, the rippling transitions cause great switching activities in the scan chain. The propagation of this switching activity into the combinational part contributes to large redundant transitions in the circuit lines. In order to suppress the scan chain transitions from propagating during shift cycles, we have proposed a low power gating scan cell which contains a modified slave latch augmented by a gating logic. For constructing the gating logic, we have utilized a transmission gate and an inverter to gate the scan output to the combinational logic as illustrated in Figure 2a. It uses the transmission gate to cut off the connection between the inverted scan cell output $\overline{Q}$ and the output Q of the scan cells during shift mode. As a result, the switching activities on the $\overline{Q}$ during shift mode does not affect the scan cell output Q which is used for driving the combinational logic. High resistance offered by an inactive transmission gate reduces the leakage current in the transmission gate during shift mode and the response capture cycle since the transmission gate is idling in these intervals. In addition, the transmission gate is a strong driver that feeds the gating logic inverter and pseudo primary inputs during normal/capture mode. Figure 2a–c depicts the proposed low power gating scan cell and the data propagation paths during shift and normal/capture modes of operation, respectively.

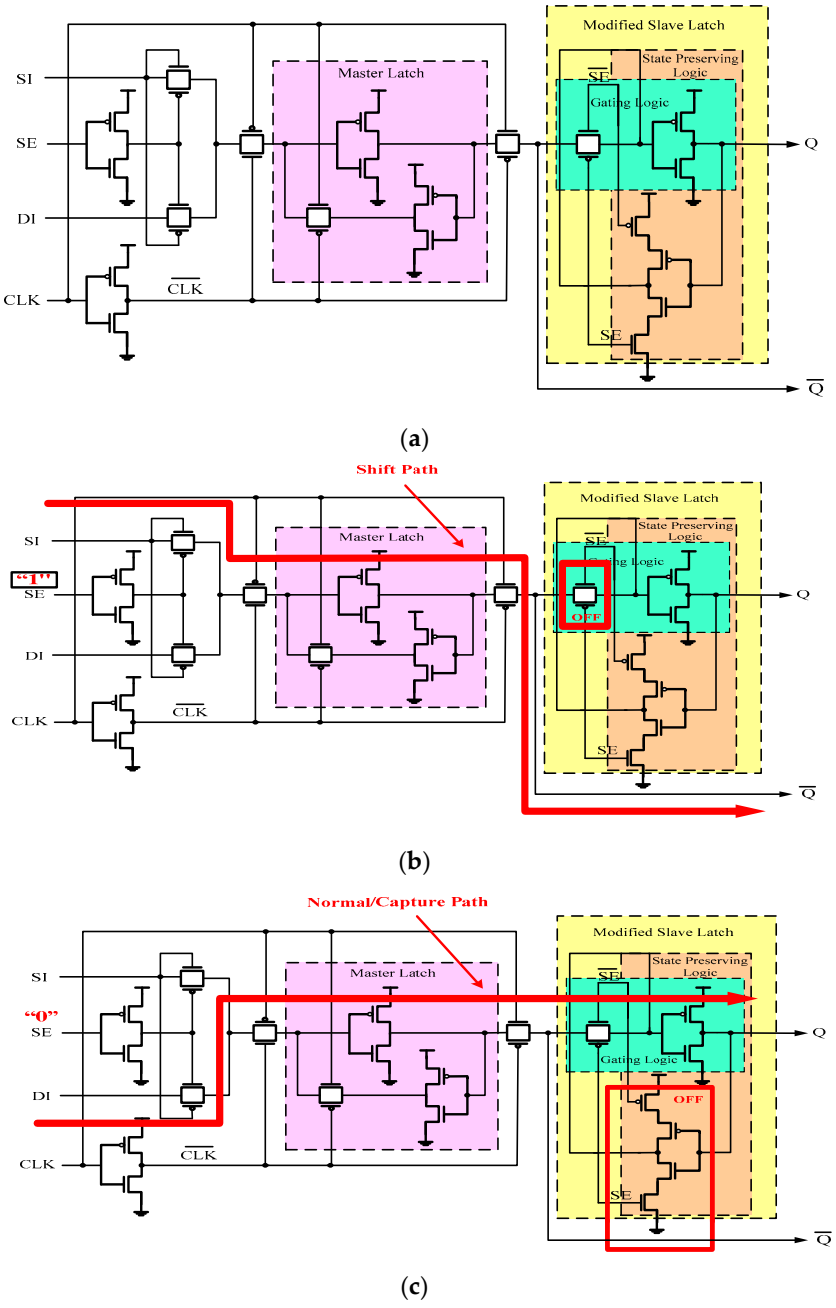


Figure 2. (**a**) Proposed low power gating scan cell with gating and state preserving logic; (**b**) Data propagation path in shift mode; (**c**) Data propagation path in normal/capture mode.

In order to totally prevent the unnecessary transitions to the combinational logic during shift mode, a state preserving logic has been proposed. It is a feedback structure that refreshes the scan output Q with the previous logic state. The two pull-up and pull-down sleep transistors are active during shift mode which cause the state preserving logic to fix the scan output logic to the same previous logic. However, unlike gating logic, this section is transparent in the normal/capture mode of operation since the sleep transistors are inactive. During this mode, the state preserving logic consumes low leakage power since the two sleep transistors cut off the power rail. The two pull-up and pull-down transistors also contribute to active leakage reduction due to the stacking effect [44,45]. These can alleviate the effect of state preserving on peak power during normal/capture mode. The transmission gate, pull-up, and pull-down sleep transistors are driven by the shift enable signal *SE* so no extra

control signal is required. Sharing the pull-up and pull-down transistors of the state preserving logic among all the scan cells can alleviate the scan chain area overhead.

It is aforementioned that one of the main concerns about gating techniques is the elevated peak power beyond the chip power budget caused by gating logic toggling between gating (shift) mode and transparent (normal/capture) mode. It is noteworthy that the proposed scheme aims to take advantage of the high potential of scan gating approaches in shift power reduction and offers a more practicable scheme by maintaining the scan gating's average and peak power consumption during capture mode (which are the general side effects of scan gating approaches) as close as possible to that of the conventional scan cell.

It is important to note that, often, capture power consumption refers to transitions that happen within scan cells when they have different values before and after capture. However, in some studies, transitions in the combinational part in launch cycles also have been considered as capture power. In this paper, we consider the whole capture clock cycle including both launch and capture clock edges for evaluating the capture power consumption.

During capture mode, peak power consumption is highly dependent on the test vectors and also test responses that are applied to the scan cell through the functional (*DI*) input of the scan cell. Moreover, in gating scan cells, the shift enable (*SE*) signal also has an important influence on the amount of switching activities during capture mode. Hence, the numbers of transitions occuring in the scan cell during capture mode is determined based on two conditions:

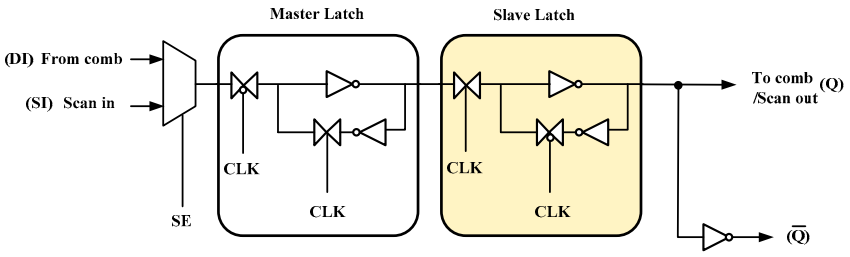
- Whether the value that is needed to be captured (the value on *DI* input) is identical to the corresponding test bit value.
- Whether the shift enable (*SE*) signal falls within the capture clock rising edge.

As highlighted earlier, the peak power corresponds to the highest amount of power consumed during a small instant of time t_{small} after the application of the test vector. This can be interpreted as the highest number of transistors that simultaneously switch during capture mode. It usually happens at the beginning of each capture cycle due to significant switching activities that occur at the signal lines and transistors due to the circuit mode changing from shift to capture.

Figure 3a,b demonstrate the gate level implementation of the conventional scan cell and the proposed low power gating scan cell. As seen, the only difference between the architecture of the conventional scan cell and the proposed gating scan cell lies in their slave latch internal structure. Consequently, the difference in the amount of transitions that happen in the modified slave latch of the proposed scan compared with the slave latch of the conventional scan cell can determine the capture power overhead in the proposed gating scan cell scheme.

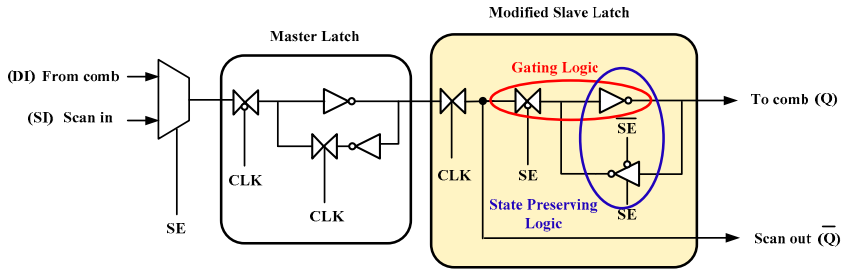
According to above discussion, in order to present a valid comparison regarding the capture peak power, it is necessary to consider every possible scenario in each scan cell at the beginning of each capture mode.

Here are the possible scenarios that can happen in each scan cell during capture mode.



(**a**)

Figure 3. *Cont.*



(**b**)

Figure 3. Gate level implementation of (**a**) Conventional scan cell; (**b**) Proposed low power gating scan cell.

4.1. Worst Case Capture Switching Activity

In the capture mode of operation, one or both of the following scenarios may happen:

- The binary logic of the test response ($DI(t+1)$) has a different value compared with the corresponding test vector bit on the Q output of the scan cell ($SI(t)$).
- Test pattern pairs ($V1$,$V2$) are applied to the circuit-under-test (CUT) through scan cells in launch-off-capture (LOC) transition fault testing. Pattern $V1$ and pattern $V2$ include non-identical corresponding pattern bits to propagate the transition and capture it at an observation point.

4.1.1. Conventional Scan Cell

It causes both feedback inverters in the conventional slave latch to switch. In addition, there are two transmission gates in the conventional slave latch controlled by the clock that contribute to capture switching as the capture clock rises. Therefore, the total numbers of switching transistors in the conventional slave latch is eight (8) transistors.

4.1.2. Proposed Low Power Scan Cell

In this case, the number of switching transistors in the modified slave latch vary depending on the time that the shift enable (SE) signal toggles from "1" to "0":

- The shift enable (SE) signal falls simultaneously with the capture rising clock, and then the total number of switching transistors in the modified slave latch will be six (6) transistors, including two transmission gates and two feedback inverters. Note that the inverter in the refresh feedback does not contribute in switching activity as the two sleep transistors disconnect it from the power supply and ground during the capture mode of operation.
- The shift enable (SE) signal falls before the capture rising clock, and then the total number of switching transistors in the modified slave latch will be four (4) transistors, including the transmission gate that is controlled by the clock and inverter in the scan cell functional path. Note that since the shift enable signal has already switched from "1" to "0" earlier, the inverter in the refresh feedback as well as the transmission gate controlled by the shift enable (SE) signal likely do not contribute in toggling in this capture scenario, as the former is disconnected from the power supply and the latter merely behaves as a connected switch.

Considering the worst case scenario for the conventional scan cell and both possible worst case scenarios for the proposed gating scan cell, it can be seen that the proposed scan cell is able to reduce the peak power compared to the conventional scan cell. This is because the proposed low power gating scan cell compared with the conventional scan cell causes less number of transistors to switch simultaneously inside the scan cell during the application of test vectors (capture mode). To the best of

our knowledge, there is no gating scan cell found in the literature that is able to reduce the capture peak power over the conventional scan cell.

The proposed low power gating scan cell works as a flip-flop because the inserted state preserving logic together with the gating logic function as a modified slave latch which has power reduction roles. Due to the shift path with less complexity, the scan cell speed has been accelerated during shifting which consequently alleviate the setup time violations. However, like other scan cells, the hold time violation concerns still exist. The reduced area and propagation delay due to the removal of two inverters and a transmission gate in the scan structure can moderate the area and delay overhead imposed by the augmented gating logic and also the state preserving logic.

Since the shift path in the proposed scan cell has been established through the $\overline{Q}$ output of scan cell, adaptive test patterns can be used instead of original ones. The adaptive scan process has been summarized in Figure 4.

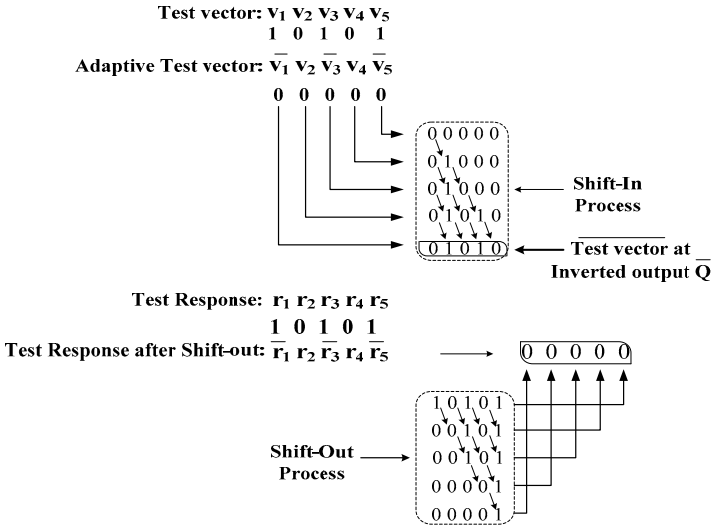


Figure 4. Adaptive scan process.

Let v_i represent a test pattern to be shifted to a scan cell. The adaptive test patterns are generated such that $\overline{v_i}$ is shifted to the destination of the inverted scan cell after the shift-in process. $\overline{v_i}$ is inverted to vi after going through gating logic during the test application. Let $v_i{}'$ be an adaptive test pattern and $1 \leq i \leq N$ where N is the number of scan cells in a scan chain. $v_i{}' = v_i$ for an even index i and $v_i{}' = \overline{v_i}$ for an odd index i whether N is an odd or even number. The adaptive test pattern formulation is as follows.

$$vi' = \begin{cases} vi \text{ for even index } i \\ \overline{v_i} \text{ for odd index } i \end{cases}$$

Modifications are necessary for test responses after the shift-out process since the responses are captured by the inverted scan cells. Let r_i represent the test response of a pseudo output. After being captured by the inverted scan cell, it becomes $\overline{r_i}$ The shifting process of $\overline{r_i}$ takes place along the inverted scan cells. Let $r_i{}'$ be the test response that reaches scan-out after shifting where $1 \leq i \leq N$ and N is the number of scan cells. $r_i{}' = \overline{r_i}$ for an odd index i and $r_i{}' = r_i$ for an even index i when N is an odd number, while $r_i{}' = r_i$ for an odd index i and $r_i{}' = \overline{r_i}$ for an even index i when N is an even number. The modifying test pattern formulation is as follows.

For N number of scan cells when N is an odd number:

$$ri' = \begin{cases} ri \text{ for even index } i \\ \overline{r_i} \text{ for odd index } i \end{cases}$$

For N number of scan cells when N is an even number:

$$ri' = \begin{cases} ri \text{ for odd index } i \\ \overline{r_i} \text{ for even index } i \end{cases}$$

Therefore, an inversion needs to be performed on r_i' when $r_i' = \overline{r_i}$ to retrieve the correct test response for the response comparison.

It is noteworthy that the mentioned adaptive scan process is fully automated and will be carried out with the automatic test pattern generation (ATPG) tool. Since the adaptive test vector and the expected test response after shift-out is generated by the ATPG tool after scan insertion of the synthesized circuit using the proposed scan structure, the proposed structure does not have any impact on the original fault coverage.

5. Experimental Results and Comparisons

The proposed low power gating scan cell has been implemented through conducting a full-custom layout design incorporating the Synopsys Custom Designer and Laker. Figure 5 shows the full-custom layout design for the proposed gating scan cell. Next, in order to verify the proposed scan cell, a set of post-layout simulations has been carried out on the parasitic included spice netlist using HSPICE in Synopsys 32/28 nm CMOS technology with the supply voltage of 1.05 Volt and clock frequency 250 MHz at room temperature. The simulation results were then compared to the conventional scan cell and the modified scan cell presented in [34] in terms of power, propagation delay, power-delay-product (PDP), and area overhead. The power consumption and propagation delay were observed by applying randomly generated waveforms.

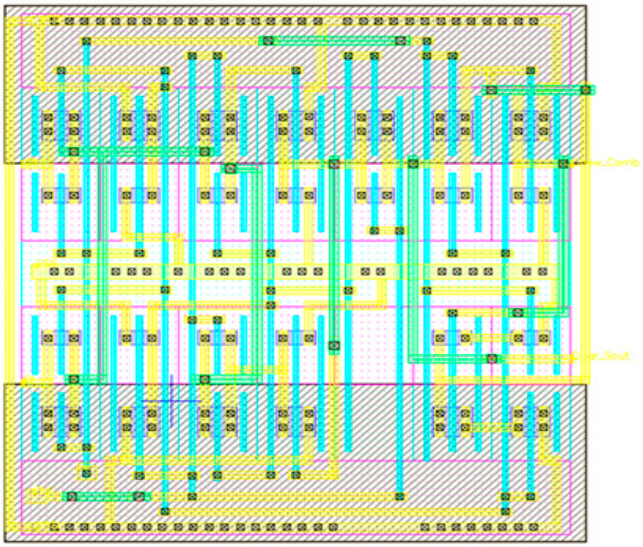


Figure 5. Full-custom layout design for the proposed low power gating scan cell in 32/28 nm CMOS technology using Laker.

The simulated output waveform of each scan cell to the combinational logic has been shown for the conventional scan cell, proposed gating scan cell, and modified scan cell in Figure 6. It is clearly seen that unlike the conventional scan cell, the proposed gating scan cell and the modified scan cell have no transitions in the combinational logic during the shift session, as the scan cell output "*Qnew_Comb*" remains the same while the shift enable (*SE*) is high. Note that, "*Qnew_Comb*" is the scan cell output connecting to the combinational part.

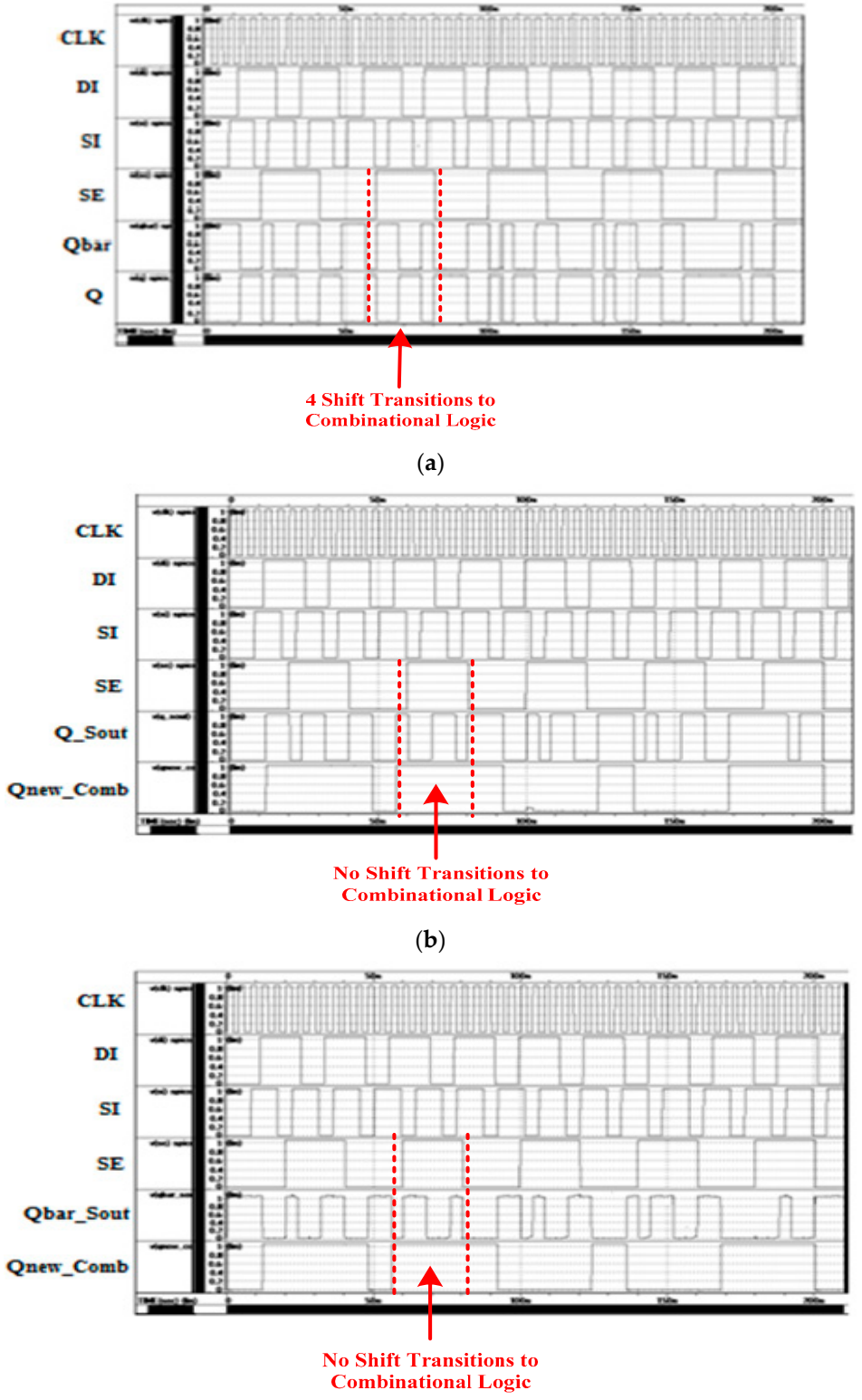


Figure 6. Post-layout simulated output waveform of (**a**) Conventional Scan Cell; (**b**) Modified Scan Cell [34]; and (**c**) Proposed Gating Scan Cell at 250 MHz clock frequency.

In order to clarify the transition reduction ratio (TRR) at the functional output of each scan cell, we have pointed out one sample shift cycle with red dotted lines in the post-layout simulated

waveforms for the conventional scan cell, proposed scan cell, and modified scan cell presented in [34] (see Figure 6). It is clearly observable that the proposed scan cell and modified scan cell are both able to totally suppress the transitions on the functional path of the scan cell and consequently combinational logic during shift mode. This means a 100% Transition Reduction Ratio (TRR) on the scan cell functional path is achievable during shift mode using the state preserving hold technique employed in the proposed gating scan cell as well as the modified scan cell. Moreover, the number of transitions on the "*Qnew_Comb*" (which is the proposed scan cell output connecting to the combinational part) during the whole test application time has been reduced from 26 transitions to 8 transitions in the proposed gating scan cell and the modified scan cell for the identical applied test patterns. This means a 69.93% Transition Reduction Ratio (TRR) during the whole test application has been achieved using the state preserving hold technique.

The main goal to be achieved by the proposed low power gating scan cell is to reduce the power consumption not only in the combinational part but also inside the scan cell structure as well. This makes the proposed low power gating scan cell more distinct compared to the modified scan cell and existing scan gating approaches. In the next part, a comparative analysis study of the power consumption for one scan cell has been reported in terms of the scan cell total average power during the whole test application time, shift power, and capture power. The latter refers to peak power since the logic values in many scan cells change simultaneously during this mode.

5.1. Post-Layout Scan Cell Simulation Results

The comparative analysis results on total power consumption for each scan cell are shown in Table 1. To evaluate the total power consumption, identical random patterns are applied to each scan cell and the total power consumption during both test and normal modes of operation is observed. As shown in Table 1, the proposed low power gating scan cell achieves a 7.21% improvement on average in terms of the total power consumption inside the scan cell over the conventional scan cell. The negative 26.97% improvement obtained for the modified scan cell implies that unlike the proposed gating scan cell, this scan cell increases power consumption over the conventional scan cell. Thus, it is only able to reduce power dissipation in the combinational part, during shifting.

Table 1. Comparison of the total power consumption during shift and normal/capture mode.

	Conventional Scan Cell	**Proposed Low Power Gating Scan Cell**		**Modified Scan Cell**	
	Power Con. (W)	**Power Con. (W)**	**% Imp.**	**Power Con. (W)**	**% Imp.**
Ave. Total Power	7.6622×10^{-7}	7.1095×10^{-7}	**7.21**	9.7289×10^{-7}	**−26.97**

Table 2 shows the improvement of power consumption for our proposed scan cell and the modified scan cell over the conventional scan cell in four successive shift cycles. The proposed scan cell outperforms both the conventional scan cell and modified scan cell in all shift cycles. This is because it exploits a shorter shift path with less complexity compared to the other mentioned scan cells.

Table 2. Comparison of the average power consumption during Shift mode.

	Conventional Scan Cell	**Proposed Low Power Gating Scan Cell**		**Modified Scan Cell**	
	Power Con. (W)	**Power Con. (W)**	**% Imp.**	**Power Con. (W)**	**% Imp.**
Shift Cycle #1	8.9381×10^{-7}	7.4193×10^{-7}	16.99	1.0064×10^{-6}	−12.59
Shift Cycle #2	7.4784×10^{-7}	6.6012×10^{-7}	11.72	8.7580×10^{-7}	−17.11
Shift Cycle #3	7.5832×10^{-7}	6.7539×10^{-7}	10.93	1.0704×10^{-6}	−41.15
Shift Cycle #4	7.6638×10^{-7}	6.6542×10^{-7}	13.17	8.9380×10^{-7}	−16.62
Average	7.9158×10^{-7}	6.8571×10^{-7}	**13.37**	9.6160×10^{-7}	**−21.48**

In order to show the impact of the proposed gating scan cell on the peak power, we have compared the percentage of peak power increase in the proposed gating scan cell and modified scan cell over the conventional scan cell through four successive normal/capture cycles (each including one clock period).

Table 3 backs up our earlier claim regarding the capture peak power reduction in the proposed scan cell over the conventional scan cell since the modified slave latch in the proposed scan cell is able to reduce simultaneous transistor transitions at the beginning of the capture cycle. It shows the peak power consumption during four capture cycles for the proposed gating scan cell and modified scan cell over the conventional scan cell. It can be seen that the proposed scan cell is able to improve peak power over the conventional scan cell during all capture/normal cycles up to 5.32%, while the modified scan cell increases peak power in all investigated normal/capture cycles (up to 19.10% in second capture cycle).

Table 3. Comparison of the peak power consumption during normal/capture mode.

	Conventional Scan Cell	**Proposed Low Power Gating Scan Cell**		**Modified Scan Cell**	
	Power Con. (W)	**Power Con. (W)**	**% Imp.**	**Power Con. (W)**	**% Imp.**
Capture Cycle #1	4.4665×10^{-5}	4.2286×10^{-5}	5.32	4.9785×10^{-5}	**−11.46**
Capture Cycle #1	4.0590×10^{-5}	3.9353×10^{-5}	3.04	4.8344×10^{-5}	**−19.10**
Capture Cycle #1	4.7428×10^{-5}	4.5979×10^{-5}	3.05	5.0032×10^{-5}	**−5.49**
Capture Cycle #1	4.7463×10^{-5}	4.6714×10^{-5}	1.57	5.0358×10^{-5}	**−6.09**

In Table 4, various delay arcs for all compared scan cells has been reported in two sub-sections. The first sub-section represents the exact amount of propagation delay for each scan cell and the achieved percentage of improvement in each (shift, capture, and launch) path over the conventional scan cell. It is observable that the proposed gating scan cell delivers improvements on shift delay and capture delay over the conventional scan cell by 3.08% and 1.12%, respectively.

Table 4. Comparison of the propagation delay overhead.

Percentage of Improvements over Conventional Scan Cell					
	Conventional Scan Cell	**Proposed Low Power Gating Scan Cell**		**Modified Scan Cell**	
	Ave. Prop. Delay(S)	**Ave. Prop. Delay(S)**	**% Imp.**	**Ave. Prop. Delay(S)**	**% Imp.**
Shift Input (SI) to shift output (Shift Delay)	1.3505×10^{-9}	1.3088×10^{-9}	3.08%	1.3397×10^{-9}	0.79%
Data Input (DI) to shift output (Capture Delay)	8.5344×10^{-10}	8.4385×10^{-10}	1.12%	8.4360×10^{-10}	1.15%
DI to Qnew (Launch Delay)	8.5344×10^{-10}	8.7755×10^{-10}	**−2.82%**	8.6798×10^{-10}	**−1.70%**
Percentage of Propagation Delay over Clock Period					
CLK to shift output	1.25%	0.61%		0.99%	
CLK to Qnew (launch) output	1.33%	**1.93%**		**1.69%**	
Power-Delay-Product (PDP)					
PDP	4.0947×10^{-17}	5.5132×10^{-17}		6.6137×10^{-17}	

It can be noticed that, the achieved improvement in shift delay is on the scan cell level. However, the improvement in shift speed in large industrial designs highly depends on the number of scan cells in the scan chain due to the serial nature of shifting. Our proposed gating scan cell causes delay overhead on the scan cell data path to combinational logic by 2.82% through the normal/capture mode of operation.

The calculated propagation delay on the clock signal in shift (CLK-to-shift output) and launch (CLK-to-launch-output) has been presented as the percentage of simulated clock period in the second

sub-section. According to this sub-section, the portion of time is needed to be taken for propagating data through the shift path after the rising edge of the clock for the proposed scan cell is 0.61% of the clock period that corresponds to 50.7% and 37.86% improvements in the CLK-to-shift output over the conventional scan cell and modified scan cell, respectively. Finally, the last row in Table 4 refers to exact amount of PDP for each related scan cell. It is interesting to note that although the modified scan cell delivers better propagation delay on the clock to launch output, the proposed scan cell still outperforms the modified scan cell in terms of PDP.

It is noteworthy that the increased complexity in the proposed scan cell regarding the delay overhead on the data launch path and also the launch clock in the proposed gating scan cell may raise the question of violating the timing closure on critical paths. Note that we implemented sleep transistors in state preserving with a minimum transistor size in 32/28 nm CMOS technology. However, a further improvement in launch delay can be achieved by up-sizing the sleep transistors referred to in [33]. This does not have any effect on the gate switching activity and it only has a penalty in terms of the area. Furthermore, partial gating techniques can be practiced by identifying those scan cells which can meet the timing closure after getting substituted by the proposed gating scan cell. This will result in power reduction in both the scan chain and combinational part at no performance degradation cost.

To evaluate the area overhead imposed by the proposed structure, we calculated the actual size of the proposed gating scan cell from the layout design. The routing overhead has not been considered in the area overhead. However, the routing overhead associated with the proposed gating structure should not be high since no additional control signal is required. In the same manner, the area overhead for the conventional scan cell and modified scan cell has been measured. The largest ITC'99 benchmark circuits were chosen in order to show the impact of the proposed scan cell on the circuit area overhead. Furthermore, the full gating architecture has been considered for all benchmark circuits as an index for the worst case of the area penalty. We have considered the actual scan chain size in each benchmark circuit as a metric for calculating the area overhead in each case. Since the compared scan cells address the area overhead only on the scan chain structure, they do not have any impact on increasing the combinational part area. Table 5 shows the characteristic of the selected benchmark circuits.

Table 5. ITC'99 Benchmark Circuits' characteristics.

Benchmark Circuit	# PI	# PO	# Gates	# Flip-Flops
b14	32	54	10,098	245
b15	36	70	8922	449
b17	37	97	32,326	1415
b18	36	23	114,621	3320
b19	21	30	231,320	6642
b21	32	22	20,571	490
b22	32	22	29,951	735

In Figure 7 the actual size of the scan chain for each compared scan cell has been shown. It is observable that the area overhead addressed by the scan chain has been reduced in the case of using the proposed scan cell compared with the modified scan cell by 20.4%. The achieved improvement for the proposed scan cell in the area overhead remains at the same level for all benchmark circuits regardless of the circuit size.

In order to alleviate the active area taken up by the proposed gating scan cell, the pull-up/down sleep transistors in state preserving logic can be shared between all scan cells in the full gating architecture. In partial gating architecture, only those scan cells that are on non-critical paths share the sleep transistors. We have considered the full gating scan in our experiment and have assumed that for random input patterns, nearly half of the scan cells do not switch and the pull-up and pull-down

transistors are exercised for almost half of the scan cells at the same time. Thereby, the channel width for shared pull-up and pull-down transistors are chosen as follows.

$$W_{Shared\_pull\text{-}up} = 0.5 \times FF \times (5 \times W_{min\ (Pmos)})$$

$$W_{Shared\_pull\text{-}down} = 0.5 \times FF \times (5 \times W_{min\ (Nmos)})$$

where FF is the number of scan cells. The active area for the shared pull-up and pull-down transistor is calculated based on the total transistor active area ($W \times L$ for a transistor) and is denoted by AreaPull-up and AreaPull-down, respectively.

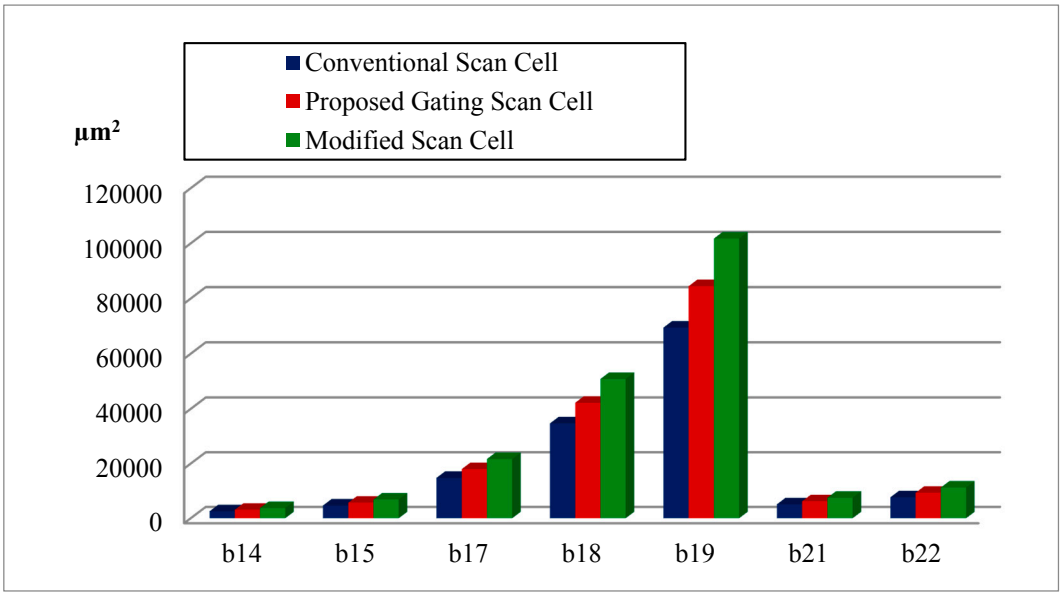


Figure 7. Comparison of the full gating area overhead in ITC'99 benchmark circuits.

Next, similar to previous experiments, the actual size of the proposed design excluding the pull-up and pull-down sleep transistors has been extracted from the layout design. Based on this discussion, the actual size of benchmark circuits fully gated by the proposed low power gating scan cell is given by

$$Area_{Benchmark\_circuit} = (Area_{PGscan\_cell} \times FF) + Area_{Pull\text{-}down} + Area_{Pull\text{-}down}$$

Figure 8 indicates the area overhead of the proposed shared low power gating scan chain for the different benchmarks compared with the conventional scan chain and modified scan chain. As can be seen, improvement in area overhead has been achieved by 12.46% for the proposed shared low power gating scan chain compared with the proposed low power gating scan chain. The observed area overhead penalty for the shared low power gating scan chain compared with the conventional scan chain is 6.45% for all benchmark circuits.

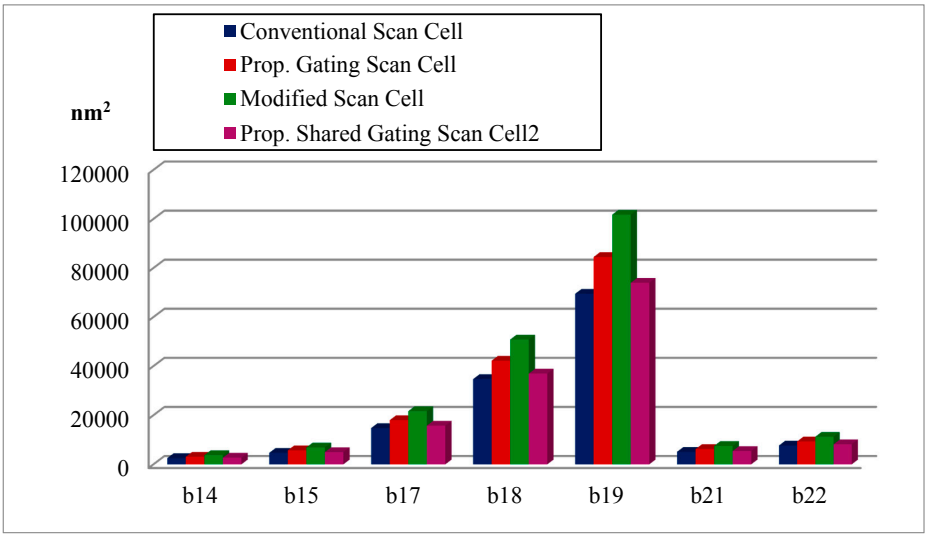


Figure 8. Comparison of the full gating area overhead in ITC'99 benchmark circuits.

5.2. Vector-Dependent Power Analysis Results

In the previous section, the simulation results and discussions were presented for each scan cell. This section provides simulation results on the shift and capture power consumption for several ITC'99 benchmark circuits. In this experiment, each benchmark circuit first was scan inserted with the conventional scan cell and next with the proposed low power gating scan cell. The results on the shift and capture power are then compared for power improvement calculations.

Power consumption evaluations for benchmark circuits were carried out by synthesizing and scan insertion of the ITC'99 benchmark circuits in the Synopsys Design Compiler. The test patterns for transition fault models were then generated for the gate-level mapped netlists using Synopsys TetraMax in 32/28 nm standard CMOS technology for all possible corners, including the worst case corner of the fast NMOS and fast PMOS transistors. Next, the Verilog test-benches generated by Synopsys TetraMax for each benchmark circuit were dumped into VCD files using Synopsys VCS. The VCD files were then used by Synopsys PrimeTime PX to create the vector-dependent power reports during the shift mode and capture mode.

Table 6 shows the percentage of shift power improvements for each benchmark circuit using the proposed low power gating scan cell over the conventional scan cell to form their scan chain.

Table 6. Percentage of shift power improvements for the proposed low power gating scan cell over the conventional scan cell.

	Scan Chain with Conventional Scan Cell		Scan Chain with Proposed Low Power Gating Scan Cell			
	Dynamic Power (W)	Peak Power (W)	Dynamic Power (W)	% Imp.	Peak Power (W)	% Imp.
b14	1.17×10^{-5}	0.4174	4.59×10^{-6}	60.7%	0.1445	65.4%
b15	1.03×10^{-5}	1.4332	5.57×10^{-6}	46.1%	0.2173	84.8%
b18	1.69×10^{-5}	1.8324	7.40×10^{-6}	56.2%	0.3287	82.1%
b21	2.10×10^{-5}	1.5403	9.81×10^{-6}	53.34%	0.2800	81.8%
b22	3.78×10^{-5}	1.4919	1.23×10^{-5}	67.45%	0.4784	67.9%

As it is stated in Table 6, all simulated benchmark circuits employing the proposed low power gating scan cell showed significant improvements up to 67.4% and 84.8% in shift dynamic and peak power, respectively.

Table 7 represents the percentage of capture (average and peak) power improvements for each benchmark circuit utilizing the proposed low power gating scan cell over the conventional scan cell in their scan chain. It is clearly observable that all simulated benchmark circuits achieve considerable capture peak power improvement up to 80.2%. As shown earlier in Table 1, one proposed scan cell is able to improve the capture peak power over one conventional scan cell in the worst case scenario. Consequently, significant peak power reductions have been observed in benchmark circuits composed of hundreds or thousands of scan cells.

Table 7. Percentage of capture power improvements for the proposed low power gating scan cell over the conventional scan cell.

	Scan Chain with Conventional Scan Cell		Scan Chain with Proposed Low Power Gating Scan Cell			
	Average Power (W)	Peak Power (W)	Average Power (W)	% Imp.	Peak Power (W)	% Imp.
b14	1.876×10^{-4}	0.3738	1.989×10^{-4}	−6.0%	0.1445	61.3%
b15	3.214×10^{-4}	0.6936	3.385×10^{-4}	−5.3%	0.2438	64.9%
b18	4.525×10^{-4}	1.6027	5.000×10^{-4}	−10.5%	0.4255	73.5%
b21	4.192×10^{-4}	1.5402	4.569×10^{-4}	−9.0%	0.3044	80.2%
b22	6.318×10^{-4}	1.7336	7.063×10^{-4}	−11.8%	0.5496	68.3%

However, all benchmark circuits using the proposed low power gating scan cell show a capture average power penalty up to 11.8%. This is because unlike peak power that is defined based on the highest instantaneous power, capture average power is determined based on the internal power, switching power, leakage power, and net switching power over a period of time. The proposed low power gating scan cell implements gating logic in the modified slave latch by an extra transmission gate (controlled by shift enable (*SE*) signal) compared with the conventional scan cell, and therefore results in higher capture average power.

It is noteworthy that, similar to the existing scan gating approaches, the proposed low power scan cell aims for shift power reduction through suppressing the redundant transitions from the scan cell to combinational logic during shift mode. As mentioned earlier, current scan gating techniques increase capture (average and peak) power as a result of the redundant switching activity occurring in gating logics. However, one of the main advantages of the proposed scan gating scheme is that contrary to the existing scan gating techniques, it is able to maintain the capture average power close to that in the conventional scan cell and even improve the capture peak power over the conventional scan cell by implementing internal gating logic in the scan cell's slave latch. In other words, the proposed scan cell does not reduce capture power compared to the conventional scan cell, however unlike current scan gating techniques, it does not cause a high elevation in capture power.

Hence, power-aware ATPG techniques can be utilized as an alternative solution in conjunction with the proposed gating scheme in order to reduce the excessive power consumption during capture mode.

6. Future Works

To evaluate and verify the impact of the proposed low power gating scan cell on the power reduction of the whole circuit during the test (shift) mode of operation in benchmark circuits, a library characterization process will be conducted in order to develop a standard power-aware scan cell based on the proposed low power gating scan cell timing and power characteristics. The exact amount of reduction in test application time therefore will be presented according to static timing analysis (STA) reports.

7. Conclusions

One of the less intrusive and effective solutions to reduce shift power significantly, independent of the test set, is scan gating techniques. However, significant delay on signal propagation paths, large area overhead, high switching activity, and finally undesired impacts on peak power all caused by gating logics, has made them less practical for large industrial circuits. Most previous works successfully reduce shift power in combinational logic only, without considering the scan chain as the main source of power consumption during the shifting phase. In this paper, we designed and implemented an area-efficient low power gating scan cell as an integrated solution for shift power reduction in both the scan chain and combinational logic. Since the gating scan cell reduces power consumption inside the scan cell compared with the conventional scan cell, the total power consumption is reduced during the shift (test) mode of operation. The proposed gating scan cell is a modified scan cell augmented by gating and state preserving logics to gate and hold the scan cells' stimulus path while maintaining peak power under a certain threshold. Choosing a new data shift path through a less complex propagation path in the proposed gating scan cell incorporates further power reduction in the scan chain in addition to improving the critical shift timing and hence, leads to test application time reduction. Compared with the lowest cost gating techniques, the proposed gating scan cell has less DFT overhead with respect to average power, shift, and capture delay. Similar to other gating methods with state hold abilities such as the modified scan cell, the proposed low power gating architecture can be effectively employed in broadside delay fault test applications. Furthermore, it can be applied effectively to both the full gating and partial gating methods. The original fault coverage is not degraded and it does not face routing problems since no additional control signal has been employed. The proposed scheme can efficiently be utilized in both built-in-self-test (BIST) and non-BIST architectures. It can also be applied together with other scan-based power optimization methods such as scan chain partitioning and reordering techniques. Low power hardware-based as well as ATPG-based methods can be applied to the proposed structure efficiently for capture average power reduction. Therefore, these advantages make the proposed approach a potential candidate for all scan-based DFT architectures.

Acknowledgments: This research is partly sponsored by Malaysia-Japan International Institute of Technology (MJIIT) Grant with vote No. 4J014.

Author Contributions: Mahshid Mojtabavi Naeini conceived and designed the experiments; performed the experiments; analyzed the data; and wrote the paper. Sreedharan Baskara Dass gave technical advice and support regarding the Synopsys analysis tools. Ooi Chia Yee contributed in developing the design idea and supervised the project.

Conflicts of Interest: The authors declare no conflict of interest. The founding sponsors had no role in the design of the study; in the collection, analyses, or interpretation of data; in the writing of the manuscript, and in the decision to publish the results.

References

1. Girard, P. Survey of low-power testing of VLSI circuits. *IEEE Des. Test Comput.* **2002**, *19*, 82–92. [CrossRef]
2. Narayanan, P.; Mittal, R.; Poddutur, S.; Singhal, V.; Sabbarwal, P. Modified Flip-Flop Architecture to Reduce Hold Buffers and Peak Power during Scan Shift Operation. In Proceedings of the IEEE VLSI Test Symposium, Dana Point, CA, USA, 1–5 May 2011; pp. 154–159.
3. Rosinger, P.; Al-Hashimi, B.M.; Nicolici, N. Scan Architecture with mutually exclusive scan segment activation for shift and Capture Power Reduction. *IEEE Trans. Comput. Aided Des. Integr. Circuits Syst.* **2004**, *23*, 1142–1153. [CrossRef]
4. Bosio, A.; Dilillo, L.; Girard, P.; Todri, A.; Virazel, A. Why and How Controlling Power Consumption during Test: A Survey. In Proceedings of the IEEE Asian Test Symposium, Niigata, Japan, 19–22 November 2012; pp. 221–226.
5. Girard, P.; Wen, X.; Touba, N.A. Low Power Testing. In *System-on-Chip Test Architectures: Nanometer Design for Testability*; Morgan Kaufmann: Burlington, MA, USA, 2006; Chapter 7.
6. Lin, X.; Huang, Y. Scan Shift Power Reduction by Freezing Power Sensitive Scan Cells. *J. Electron. Test.* **2008**, *24*, 327–334. [CrossRef]

7. Chen, C.; Kang, C.; Sarrafzadeh, M. Activity-Sensitive Clock Tree Construction for Low Power. In Proceedings of the International Symposium Low Power Electronics Design, Monterey, CA, USA, 12–14 August 2002; pp. 279–282.
8. Farrahi, A.; Chen, C.; Srivastava, A.; Tallez, G.; Sarrafzadeh, M. Activity-Driven Clock Design. *IEEE Trans. Comput. Aided Des. Integr. Circuit Syst.* **2001**, *20*, 705–714. [CrossRef]
9. Shen, W.; Cai, Y.; Hong, X.; Hu, J. An Effective Gated Clock Tree Design Based on Activity and Register Aware Placement. *IEEE Trans. Very Large Scaled Integr. (VLSI) Syst.* **2010**, *18*, 1639–1648. [CrossRef]
10. Bonhomme, Y.; Girard, P.; Guiller, L.; Landrault, C.; Pravossoudovitch, S. A Gated Clock Scheme for Low Power Scan Testing of Logic ICs or Embedded Cores. In Proceedings of the IEEE Asian Test Symposium, Kyoto, Japan, 19–21 November 2001; pp. 253–258.
11. Rau, J.C.; Wu, C.L.; Wu, P.H. An Efficient Algorithm to Selectively Gate Scan Cells for Capture Power Reduction. *Tamkang J. Sci. Eng.* **2011**, *14*, 39–48.
12. Chosh, S.; Basu, S.; Touba, N. Joint minimization of power and area in scan testing by scan cell reordering. In Proceedings of the IEEE Computer Society Annual Symposium on VLSI, Tampa, FL, USA, 20–21 February 2003; pp. 246–249.
13. Baek, C.-K.; Kim, I.; Kim, J.-T.; Kim, Y.-H.; Min, H.B.; Lee, J.-H. A dynamic scan chain reordering for low power VLSI testing. In Proceedings of the International Conference on Information Technology Convergence and Services (ITCS), Cebu, Philippines, 11–13 August 2010; pp. 1–4.
14. Sinanoglu, O.; Bayraktaroglu, I.; Orailoglu, A. Test power reduction through minimization of scan chain transitions. In Proceedings of the VLSI Test Symposium, Monterey, CA, USA, 28 April–2 May 2002; pp. 166–171.
15. Ghosh, D.; Bhunia, S.; Roy, K. A Low Complexity Scan Reordering Algorithm for Low Power Test-Per-Scan BIST. In Proceedings of the International Conference on VLSI Design, Mumbai, India, 5–9 January 2004; pp. 883–888.
16. Bellos, M.; Bakalis, D.; Nikolos, D. Scan cell ordering for low power BIST. In Proceedings of the IEEE Computer Society Annual Symposium on VLSI, Lafayette, LA, USA, 19–20 February 2004; pp. 281–284.
17. Tseng, W.D. Scan chain ordering technique for switching activity reduction during scan test. *IEE Proc. Comput. Digit. Tech.* **2005**, *152*, 609–617. [CrossRef]
18. Bonhomme, Y.; Girard, P.; Landrault, C.; Pravossoudovitch, S. Power Driven Chaining of Flip-flops in Scan Architectures. In Proceedings of the IEEE International Test Conference, Baltimore, MD, USA, 7–10 October 2002; pp. 796–803.
19. Whetsel, L. Adapting scan architectures for low power operation. In Proceedings of the IEEE International Test Conference, Atlantic City, NJ, USA, 3–5 October 2000; pp. 863–872.
20. Bhunia, S.; Mahmoodi, H.; Ghosh, D.; Roy, K. Power Reduction in Test-Per-Scan BIST with Supply Gating and Efficient Scan Partitioning. In Proceedings of the International Symposium on Quality Electronic Design (ISQED'05), San Jose, CA, USA, 21–23 March 2005; pp. 453–458.
21. Almukhaizim, S.; Sinanoglu, O. Dynamic scan chain partitioning for reducing peak shift power during test. *IEEE Trans. Comput. Aided Des. Integr. Circuits Syst.* **2009**, *28*, 298–302. [CrossRef]
22. Xiang, D.; Hu, D.; Xu, Q.; Orailoglu, A. Low power scan testing for test data compression using a routing-driven scan architecture. *IEEE Trans. Comput. Aided Des. Integr. Circuits Syst.* **2009**, *28*, 1101–1105. [CrossRef]
23. Yamato, Y.; Wen, X.; Kochte, M.A.; Miyase, K.; Kajihara, S.; Wang, L.-T. A novel scan segmentation design method for avoiding shift timing failure in scan testing. In Proceedings of the International Test Conference, Anaheim, CA, USA, 20–22 September 2011; pp. 1–8.
24. Xiang, D.; Shen, K.; Bhattacharya, B.B.; Wen, X.; Lin, X. Thermal-Aware Small-Delay Defect Testing in Integrated Circuits for Mitigating Overkill. *IEEE Trans. Comput. Aided Des. Integr. Circuits Syst.* **2016**, *35*, 499–512. [CrossRef]
25. Xiang, D.; Wen, X.; Wang, L.-T. Low-Power Scan-Based Built-In Self-Test Based on Weighted Pseudorandom Test Pattern Generation and Reseeding. *IEEE Trans. Very Large Scaled Integr. (VLSI) Syst.* **2017**, *25*, 942–953. [CrossRef]
26. Gerstendörfer, S.; Wunderlich, H.J. Minimized Power Consumption for Scan-based BIST. In Proceedings of the IEEE International Test Conference, Atlantic City, NJ, USA, 28–30 September 1999; pp. 77–84.

27. Khatri, S.P.; Ganeshan, S.K. A Modified Scan D Flip-Flop to Reduce Test Power. In Proceedings of the IEEE International Test Synthesis Workshop (ITSW), Santa Barbara, CA, USA, 7–9 April 2008; pp. 1–3.
28. Zhang, X.; Roy, K. Power Reduction in Test-per-Scan BIST. In Proceedings of the International Online Testing Workshop, Palma De Mallorca, Spain, 3–5 July 2000; pp. 133–138.
29. Parimi, N.; Sun, X. Design of A Low Power D Flip-Flop for Test-Per-Scan Circuits. In Proceedings of the IEEE Canadian Conference on Electrical and Computer Engineering, Niagara Falls, ON, Canada, 2–5 May 2004; pp. 777–780.
30. Bushnell, M.L.; Agrawal, V.D. *Essentials of Electronic Testing for Digital memory, and Mixed-Signal VLSI Circuits*; Kluwer: Boston, MA, USA, 2000.
31. Bhunia, S.; Mahmoodi, H.; Ghosh, D.; Mukhopadhyay, S.; Roy, K. Low-Power Scan Design Using First Level Supply Gating. *IEEE Trans. Very Large Scaled Integr. (VLSI) Syst.* **2005**, *13*, 384–395. [CrossRef]
32. Bhunia, S.; Mahmoodi, H.; Ghosh, D.; Mukhopadhyay, S.; Roy, K. First Level Hold: A Novel Low-Overhead Delay Fault Testing Technique. In Proceedings of the IEEE International Symposium on Defect and Fault Tolerance in VLSI Systems, Cannes, France, 10–13 October 2004; pp. 314–315.
33. Bhunia, S.; Mahmoodi, H.; Ghosh, D.; Mukhopadhyay, S.; Roy, K. Arbitrary Two-Pattern Delay Testing Using A Low-Overhead Supply Gating Technique. *J. Electron. Test.* **2008**, *24*, 577–590. [CrossRef]
34. Mishra, A.; Sinha, N.; Satdev; Singh, V.; Chakravarty, S.; Singh, A.D. Modified Scan Flip-Flop for Low Power Testing. In Proceedings of the IEEE Asian Test Symposium, Shanghai, China, 1–4 December 2010; pp. 367–370.
35. Elshoukry, M.; Tehranipour, M.; Ravikumar, C.P. A Critical-Path-Aware Partial Gating Approach for Test Power Reduction. *ACM Trans. Des. Autom. Electron. Syst.* **2007**, *12*, 1–22. [CrossRef]
36. Sharifi, S.; Jaffari, J.; Hosseinabady, M.; Kusha, A.A.; Navabi, Z. Simultaneous Reduction of Dynamic and Static Power in Scan Structures. In Proceedings of the Design Automation and Test in Europe Conference and Exhibition, Munich, Germany, 7–11 March 2005; pp. 846–851.
37. Sankaralingam, R.; Touba, N.A. Inserting Test Points to Control Peak Power during Scan Testing. In Proceedings of the IEEE International Symposium on Defect and Fault Tolerance in VLSI System, Vancouver, BC, Canada, 6–8 November 2002; pp. 138–146.
38. Kavousianos, X.; Bakalis, D.; Nikolos, D. Efficient Partial Scan Cell Gating for Low-Power Scan-Based Testing. *ACM Trans. Des. Autom. Electron. Syst.* **2009**, *14*, 1–15. [CrossRef]
39. Jayaraman, D.; Sethuram, R.; Tragoudas, S. Gating Internal Nodes to Reduce Power during Scan Shift. In Proceedings of the ACM GLSVLSI'10, Providence, RI, USA, 16–18 May 2010.
40. Lin, X.; Rajski, J. Test Power Reduction by Blocking Scan Cell Outputs. In Proceedings of the IEEE Asian Test Symposium, Hokkaido, Japan, 24–27 November 2008; pp. 329–336.
41. Zhao, W.; Tehranipour, M.; Chakarvarty, S. Power-Safe Test Application Using an Effective Gating Approach Considering Current Limits. In Proceedings of the IEEE VLSI Test Symposium, Dana Point, CA, USA, 1–5 May 2011; pp. 160–165.
42. Lin, Y.T.; Huang, J.L.; Wen, X. A Transition Isolation Scan Cell Design for Low Shift and Capture Power. In Proceedings of the IEEE Asian Test Symposium, Niigata, Japan, 19–22 November 2012; pp. 107–112.
43. Suhag, A.K.; Ahlawat, S.; Shivastava, V.; Singh, N. Elimination of Output Gating Performance Overhead for Critical Paths in Scan Test. *Int. J. Circuit Archit. Des.* **2013**, *1*, 62–72. [CrossRef]
44. Calhoun, B.H.; Honore, F.A.; Chandrakasan, A. Design Methodology for Fine-Grained Leakage Control in MTCMOS. In Proceedings of the 2003 International Symposium on Low Power Electronics and Design, Seoul, Korea, 25–27 August 2003; pp. 104–109.
45. Roy, K.; Mukhopadhyay, S.; Mahmoodi, H. Leakage Current Mechanism and Leakage Reduction Techniques in Deep-Submicrometer CMOS circuits. *Proc. IEEE* **2003**, *91*, 305–327. [CrossRef]