Journal of
Low Power Electronics and Applications

MDPI

Article

A Fully Integrated 2:1 Self-Oscillating Switched-Capacitor DC–DC Converter in 28 nm UTBB FD-SOI †

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† This paper is an extension of our article from A-SSCC 2015 titled "A Fully Integrated Self-Oscillating Switched-Capacitor DC-DC Converter for Near-Threshold Loads".

Academic Editor: Tony Tae-Hyoung Kim
Received: 18 May 2016; Accepted: 29 August 2016; Published: 8 September 2016

Abstract: The importance of energy-constrained processors continues to grow especially for ultra-portable sensor-based platforms for the Internet-of-Things (IoT). Processors for these IoT applications primarily operate at near-threshold (NT) voltages and have multiple power modes. Achieving high conversion efficiency within the DC–DC converter that supplies these processors is critical since energy consumption of the DC–DC/processor system is proportional to the DC–DC converter efficiency. The DC–DC converter must maintain high efficiency over a large load range generated from the multiple power modes of the processor. This paper presents a fully integrated step-down self-oscillating switched-capacitor DC–DC converter that is capable of meeting these challenges. The area of the converter is 0.0104 mm^2 and is designed in 28 nm ultra-thin body and buried oxide fully-depleted SOI (UTBB FD-SOI). Back-gate biasing within FD-SOI is utilized to increase the load power range of the converter. With an input of 1 V and output of 460 mV, measurements of the converter show a minimum efficiency of 75% for 79 nW to 200 µW loads. Measurements with an off-chip NT processor load show efficiency up to 86%. The converter's large load power range and high efficiency make it an excellent fit for energy-constrained processors.

Keywords: switched-capacitor; DC–DC converter; near-threshold voltage; self-oscillating; ultra-thin body and buried oxide fully-depleted SOI (UTBB FD-SOI); fully-depleted SOI (UTBB FD-SOI); sub-threshold; low voltage regulation

1. Introduction

The relevance of energy-constrained processors [1–6] in sensor-based platforms for Internet-of-Things (IoT) applications continues to grow. These processors typically operate at near-threshold (NT) voltages since operation at NT significantly reduces energy consumption but avoids the large variance and performance penalties associated with sub-threshold voltages [1]. While operating at NT, energy-constrained processors utilize multiple active and standby power modes to achieve further energy savings [2–4]. The NT voltage must be supplied during each of these power modes to ensure functionality within always-on blocks such as memory, timers, and interrupt controllers [3,4]. As shown in Figure 1, NT voltages are typically supplied to energy-constrained processors by a DC–DC converter with a system supply or battery. The DC–DC converter is a critical block since the energy consumption of the DC–DC/processor system is proportional to the efficiency of the DC–DC converter. Achieving high efficiency in the DC–DC converter is therefore essential to realize energy savings associated with NT operation of the processor. Maintaining high efficiency over a large load range is

also required since toggling between active and standby power modes induces 200× [2] to 6000× [3] changes in load power.

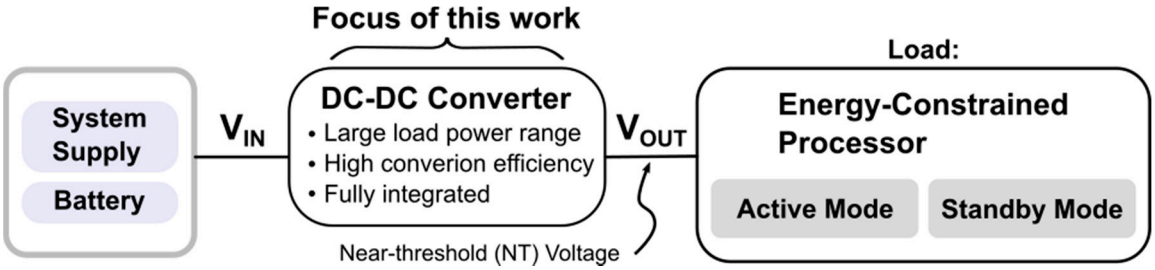


Figure 1. This work is focused on the DC–DC converter that supplies energy-constrained processor loads.

Fully integrated switched-capacitor (SC) DC–DC converters are a logical choice for supplying energy-constrained processors as they can achieve high efficiency within digital CMOS processes [7]. However, achieving high efficiency in a SC DC–DC converter is challenging for the multiple order-of-magnitude changes in load power associated with different processor power modes. The SC self-oscillating topology [8] is a promising choice to meet this challenge due to its minimal control circuitry overhead and interleaved structure. The step-up self-oscillating topology introduced in [8] showed an efficiency of over 70% over a five order-of-magnitude change in load power. This excellent performance was achieved with a step-up configuration, a varying (above-threshold) output voltage, and with charge-transfer switches operating well above the threshold voltage.

In this work, the first (2:1) step-down self-oscillating DC–DC converter with a NT output voltage (V_{OUT}) is presented [9]. It is designed in 28 nm ultra-thin body and buried oxide fully-depleted SOI (UTBB FD-SOI). The NT output voltage levels limit the maximum load power range within the self-oscillating topology since the $|V_{GS}|$ of the charge-transfer switches is at or below the threshold voltage. This results in a low overdrive voltage, which subsequently limits the maximum load current that the charge-transfer switches can handle. Additionally, the maximum oscillation frequency of the self-oscillating topology is limited from such low $|V_{GS}|$ voltages. To address both of these previous limitations associated with low $|V_{GS}|$, this work utilizes body-biasing, or back-gate biasing, within the converter to increase the maximum load power. Back-gate biasing and the self-oscillating topology together enable a large load power range with high efficiency. Section 2 describes the similarities and differences of a conventional SC converter to the self-oscillating converter. The operation of the self-oscillating converter and the details of back-gate biasing are also described. Section 3 presents measurement results. Section 4 concludes the paper.

2. Self-Oscillating DC–DC Converter

2.1. Conventional Switched-Capacitor DC–DC Converter

A conventional 2:1 SC DC–DC converter is shown in Figure 2. This converter steps down the input voltage (V_{IN}) through a Switched-Capacitor Network (SCN). During a charge phase (φ_{charge}), V_{IN} charges C_{fly} and delivers charge to the output. A charge phase requires that only S_1 and S_3 be turned *ON*. During a discharge phase ($\varphi_{discharge}$), the charge stored previously on C_{fly} is discharged to the output. The discharge phase requires that only S_2 and S_4 to be *ON*. The Clock Generator and Switch Signal Generator blocks provide signals to the gates of the switches (S_1–S_4) that ensure the correct charge or discharge phase configuration. The self-oscillating converter, which is explained in the subsequent paragraph, has an SCN that operates in the same manner as the conventional converter, but it does not require the Clock Generator and Switch Signal Generator blocks. Eliminating the need for clock generation and level conversion overhead is advantageous for low power systems since they are the dominant power losses at sub-5 μW loads [8,10].

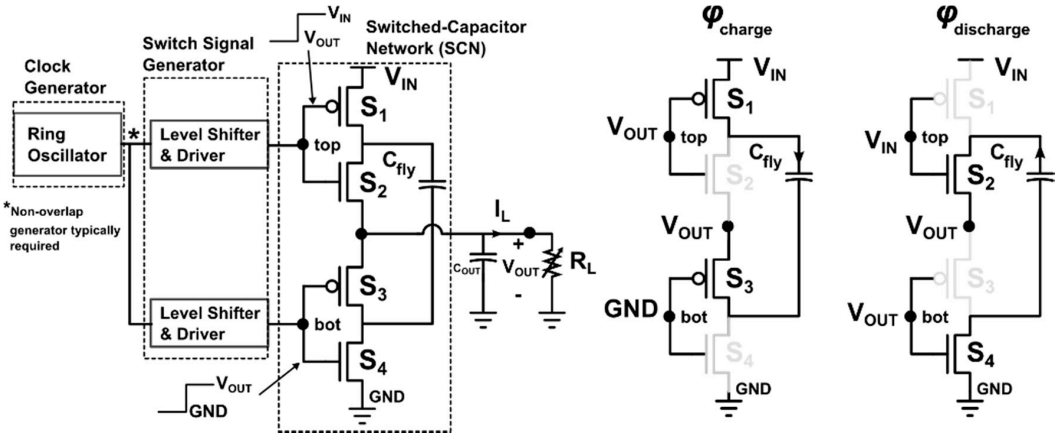


Figure 2. A conventional 2:1 switched-capacitor topology.

2.2. Step-Down Self-Oscillating DC–DC Converter

The 2:1 self-oscillating DC–DC converter is shown in Figure 3a. It is comprised of two stacked ring oscillators. The oscillators are synchronized through the fly capacitors ($C_{fly,1–5}$) and coupling capacitors C_c within the delay cell. The delay cell determines the oscillation frequency of the stacked ring oscillators. Modulating the oscillation frequency is used to maintain the output voltage over changes in load power.

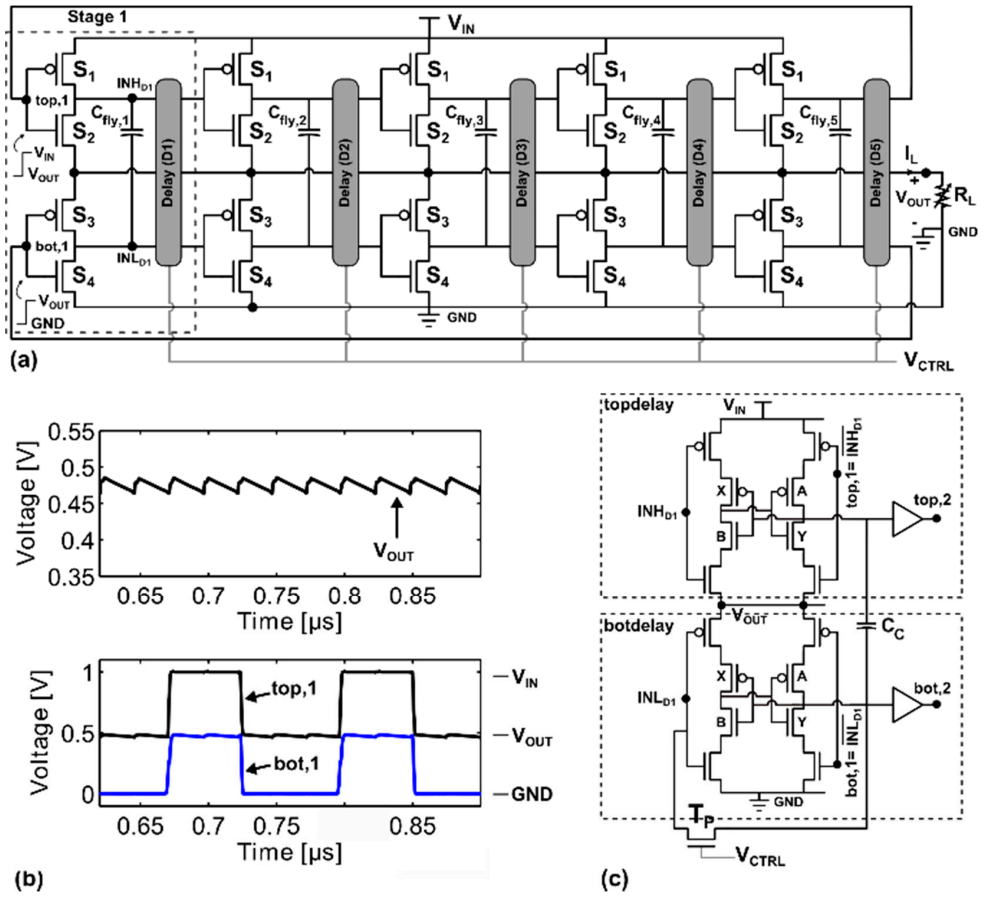


Figure 3. (**a**) 2:1 self-oscillating DC–DC converter; (**b**) Simulated output of the converter at Stage 1; (**c**) Delay cell schematic.

During oscillation, the SCN within each of the five stages alternates between a charge phase and discharge phase in the same manner as the conventional 2:1 converter shown previously in Figure 2. The converter is interleaved since each of the five stages delivers charge at different phase times. The simulated output from a single stage is shown in Figure 3b. The charge-transfer transistor lengths in each stage are twice the size of the minimum length to ensure leakage does not affect functionality at nW loads [11]. Only thin-oxide transistors are used within the converter. The fly capacitor in each stage is a 27pF MIM capacitor. In other words, there is 5×27 pF fly capacitance. Unlike MOS capacitors, the MIM capacitor does not suffer from large voltage dependences at near-threshold voltages or large bottom-plate capacitance losses. For the (active) load power levels in this design, bottom-plate capacitance is a dominant loss component.

The converter adjusts to changes in load power by tuning the delay within the delay cell. The delay cell (Di) within each stage determines the frequency of oscillation of the converter. As shown in Figure 3c, the delay cell consists of two leakage-based delay blocks [8] (*topdelay* and *botdelay*). These delay blocks operate identically and are coupled through a 0.2 pF MIM coupling capacitor C_c. The *botdelay* delay element from Stage 1 operates as follows. When the input to the delay cell (INL_{D1}) transitions, two transistors within the positive feedback loop begin to leak between the drain and source. For example, for a low-to-high transition at INL_{D1}, transistor A (B) has source-drain (drain-source) leakage. At some point, the leakage in A and B flips the state of the positive feedback loop and drives bot,2 low-to-high. The transistor T_P is used to increase (decrease) the time to flip the state of the positive feedback loop by lowering (increasing) V_{CTRL}. Unlike [8], this design does not use an additional coupling capacitor between top,2 and bot,2 since simulations showed that it had minimal effect on the converter performance.

This subsection described the operation of the step-down self-oscillating converter. In the next subsection, the effects of back-gate biasing on the converter's performance are presented. Back-gate biasing affects both the delay cell and charge-transfer switches within the converter.

2.3. Back-Gate Biasing

Back-gate biasing is used to improve the performance of the converter. More specifically, back-gate biasing increases the maximum load power of the converter for two reasons. First, back-gate biasing increases the maximum drive strength of the charge-transfer switches. Since charge-transfer switches operate at or below the threshold voltage, the effect of back-gate biasing on drive strength is large. Second, back-gate biasing on the transistors within the delay cell increase leakage between the drain and source within the positive feedback loop, and thus, shift the oscillation frequency range to a higher values.

Back-gate biasing in UTBB FD-SOI is more effective in altering a transistor's threshold voltage (V_{th}) than in nanoscale bulk CMOS for two reasons [12]. First, the range of bias voltages is not limited by diode conduction since the back-gate node is isolated from the drain and source. Second, the body-bias factor (γ) is much larger than bulk CMOS. For example, 28 nm UTBB FD-SOI has $\gamma \approx 85$ mV/V, while bulk 28 nm CMOS has $\gamma \approx 25$ mV/V. The converter takes advantage of the large bias range and high body-bias factor in order to increases its load power range.

The back-gate biasing configuration for the converter is shown in Figure 4. The (LVT) PMOS transistors have a back-gate biasing voltage source opposite in polarity but equal in magnitude to the (LVT) NMOS transistors. Increasing the back-gate bias voltage (V_{BB}) pushes both the PMOS and NMOS transistors further into forward body bias (FBB). As shown in Figure 4c, the effect of increasing V_{BB} on a single charge-transfer switch in linear mode is larger at near-threshold values of V_{GS}. The $|V_{GS}|$ of each switch within the converter is near the threshold voltage since the output of the converter is a near-threshold voltage. Thus, there is strong motivation to utilize back-gate biasing within the converter.

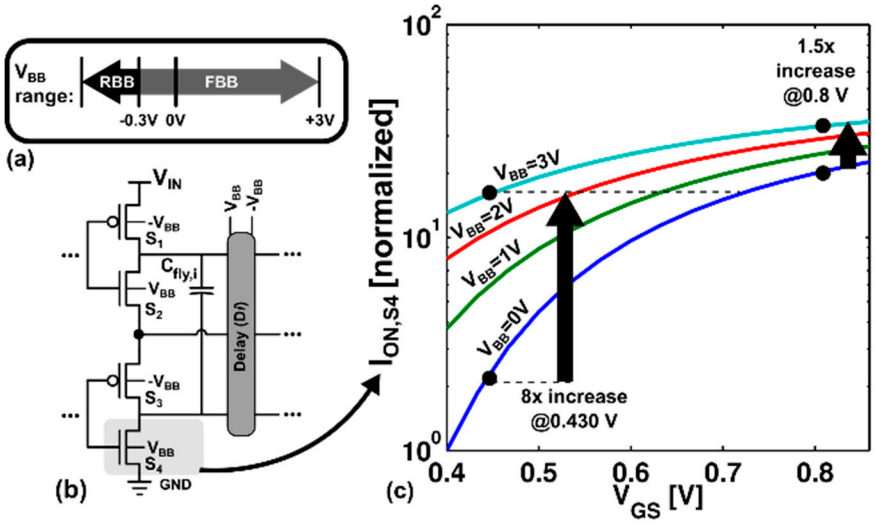


Figure 4. (**a**) Back-gate biasing range; (**b**) Back-gate bias connections within the converter; (**c**) Simulated change in the drive strength of a single switch (S_4) in linear mode.

The overall impact of back-gate biasing on the converter is found by examining the converter's total output impedance (R_O). The total output impedance depends on contributions from both the slow-switching regime impedance (R_{SSL}) and the fast switching impedance (R_{FSL}) as in [13]:

$$R_O = \sqrt{(R_{SSL})^2 + (R_{FSL})^2} = \sqrt{\left(\frac{K_c}{C_{tot} f_{SW}}\right)^2 + \left(\frac{2K_S}{G_{tot}}\right)^2}, \quad (1)$$

where K_C is $\frac{1}{4}$ and K_S is 4 for the 2:1 converter, C_{tot} is the total fly capacitance (135 pF), and G_{tot} is the summed switch conductance. In order to account for back-gate bias voltages in R_O, G_{tot} needs to be identified. G_{tot} is described by

$$G_{tot} = k\left(\frac{W_i}{L_i}\sum_{i=1}^{m} K_i\left(V_{GSi} - V_{th,i}\right)\right), \quad (2)$$

where m is the number of switches in one stage of the converter, k is the total number of stages within the converter, L_i and W_i are the charge-transfer switch sizes, K_i is the technology constant, and V_{GSi} is the gate-source voltage of the charge-transfer switch. From Equation (2), it can be seen that decreasing the threshold voltage ($V_{th,i}$) through increased V_{BB} results in a larger overdrive voltage, and thus, a larger G_{tot}. Using the back-gate biasing configuration from Figure 4, Equation (2) expands to

$$G_{tot} = \begin{array}{c} 5\left(K_n \frac{W_n}{L_n}\left(V_{IN} - 2V_{thn} + \gamma_n\left(2V_{BB} - V_{OUT}\right)\right)\right) \\ +5\left(K_p \frac{W_p}{L_p}\left(-V_{IN} - 2V_{thp} + \gamma_p\left(-2V_{BB} - V_{IN} - V_{OUT}\right)\right)\right). \end{array} \quad (3)$$

Using G_{tot} from Equation (3), the converter's total output impedance R_O from Equation (1) is plotted as a function of the converter's switching frequency (f_{SW}) as shown in Figure 5. The R_O is plotted with two sets of back-gate bias voltages: V_{BB} = 0 V and V_{BB} = 1 V in Figure 5a and V_{BB} = 0 V and V_{BB} = 2 V in Figure 5b. Increasing the back-gate bias has two effects on the converter's R_O. First, increasing V_{BB} shifts the range of f_{SW} to larger values. This is a result of a decreased delay within the delay cells. Larger values of f_{SW} enable larger load powers since R_{SSL} decreases with increased f_{SW}. Second, a larger V_{BB} increases the overdrive voltage of the converter, and thus, decreases the R_{FSL}. This lowers R_O and allows for larger load powers. In summary, increasing the back-gate bias decreases R_O. A lower R_O enables a larger maximum power ($P_{OUT,max}$) since $P_{OUT} \propto 1/R_O$.

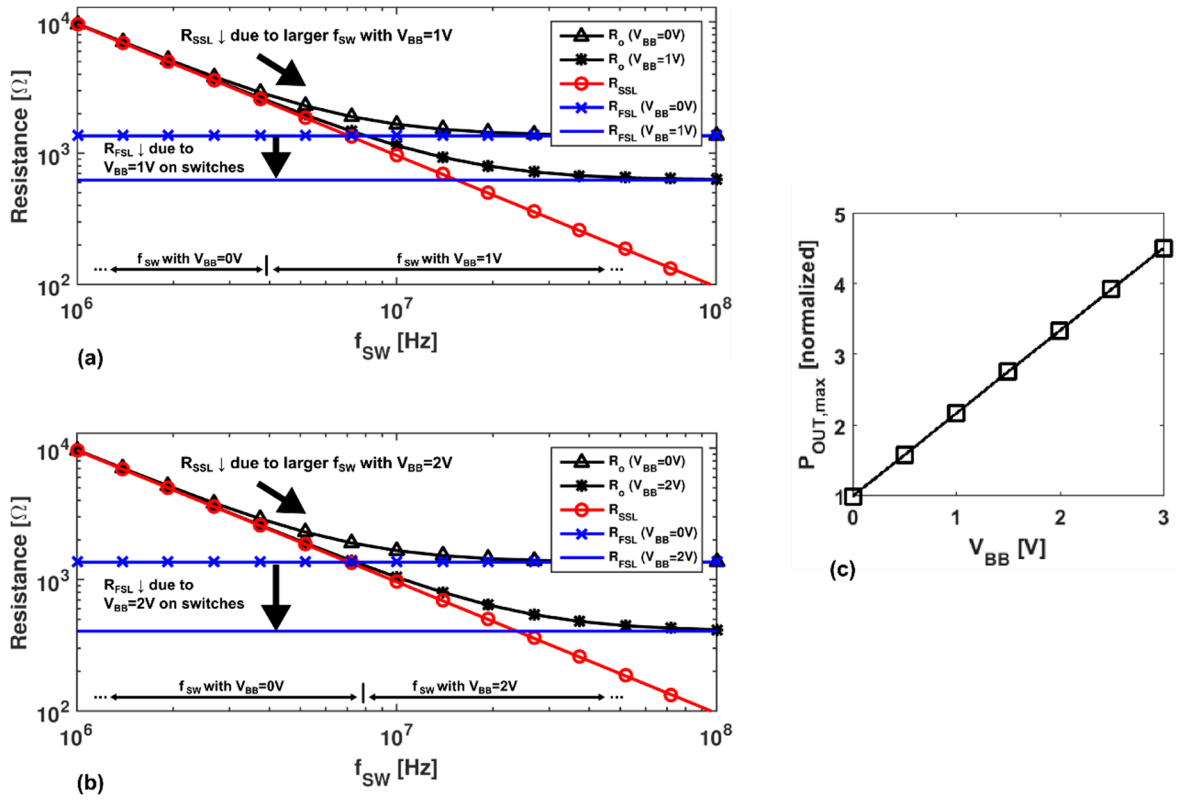


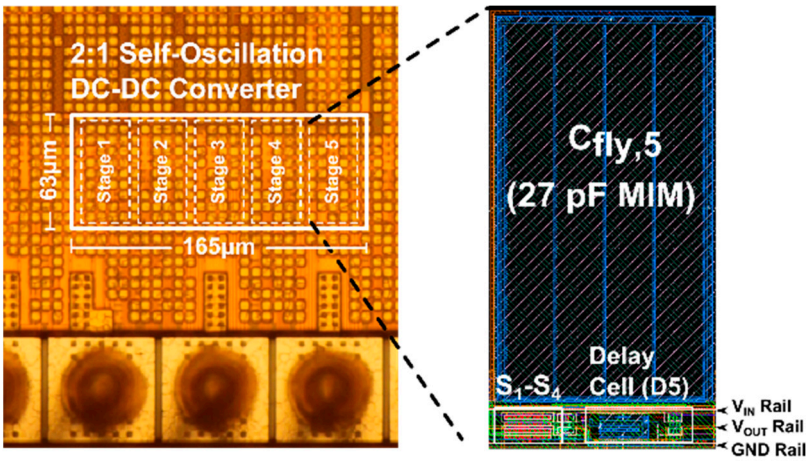
Figure 5. Analytical prediction of the converter output impedance from Equation (1). (**a**) V_{BB} = 0 V and V_{BB} = 1 V; (**b**) V_{BB} = 0 V and V_{BB} = 2 V; (**c**) Sweeping the maximum power $P_{OUT,max}$ as a function of V_{BB}. $P_{OUT,max}$ is normalized to the $P_{OUT,max}$ at V_{BB} = 0 V and uses only R_{FSL} contributions.

To further clarify the effects of V_{BB} on $P_{OUT,max}$, Figure 5c shows the increase in $P_{OUT,max}$ as V_{BB} is increased from 0 to 3 V. $P_{OUT,max}$ is estimated from Equation (1) using only the R_{FSL} contribution and is normalized to the value of $P_{OUT,max}$ with V_{BB} = 0 V. Increasing V_{BB} in the proposed converter from 0 to 3 V increases the $P_{OUT,max}$ by 4.5×.

3. Measurement Results

Measurement results from the 28 nm UTBB FD-SOI test chip are presented in this section. As shown in the annotated microphotograph of the test chip (Figure 6), all blocks within the converter are placed into a standard cell frame consisting of three power rails. This block organization simplifies the power routing and back-gate bias well connections between the five stages. The total area of the converter is 0.0104 mm^2. The back-gate bias well area increases the total converter area by 3.7%.

Due to the stacked ring oscillators, the self-oscillating converter is able to start-up without any auxiliary start-up control circuitry. Removing this control circuitry is especially beneficial in terms of efficiency at nW load powers (e.g., standby mode). A measurement of the converter at start-up is shown in Figure 7. An input voltage (V_{IN}) is stepped from 0 V to 1 V using the maximum slew-rate of an off-chip voltage source. For both output power levels (P_{OUT} = 0 µW and P_{OUT} = 100 µW), the converter stabilizes at approximately the same time that V_{IN} reaches 1 V. At P_{OUT} = 0 µW, the power consumption of the DC–DC converter is 15.6 nW.



Technology	28 nm UTBB FD-SOI
Area	0.0104 mm^2
C_{out}	0
C_{fly}	135 pF (MIM)

Figure 6. Annotated microphotograph of the 2:1 converter.

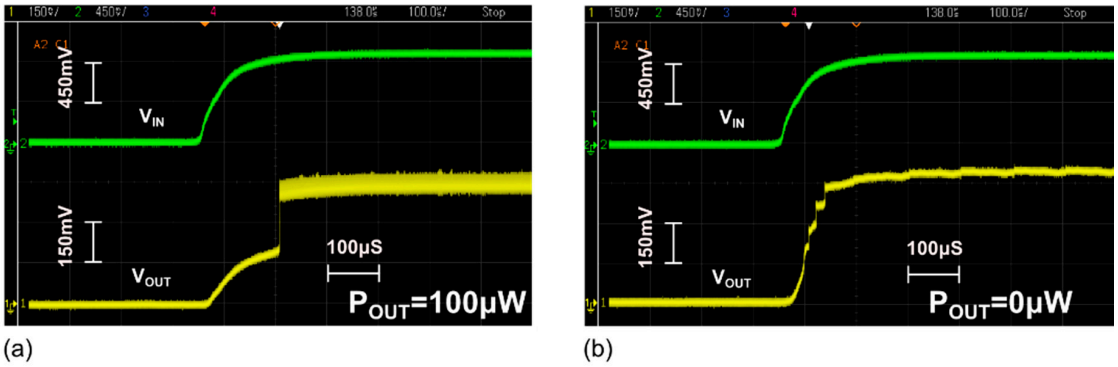


Figure 7. Measured start-up of the self-oscillating converter as V_{IN} is increased from 0 V to 1 V at (**a**) P_{OUT} = 100 µW and (**b**) P_{OUT} = 0 µW.

The converter's efficiency versus the output load power (P_{OUT}) is shown in Figure 8a. The efficiency is measured at two near-threshold output voltages (V_{OUT} = 430 mV and V_{OUT} = 460 mV). The converter's load power range is extended significantly by applying a back-gate bias of V_{BB} = 1 V (i.e., PMOS back-gate biased with −1 V and NMOS with 1 V). The 1 V is generated from V_{IN}, while the −1 V is from an off-chip voltage source. Negative body bias generators can produce −1 V with nW power consumption [14], and thus, have minimal impact on efficiency at µW load power. At V_{OUT} = 460 mV, and using V_{BB} = 1 V, the converter achieves a minimum efficiency of 75% for 79 nW to 200 µW (current source). With an off-chip 32-bit processor load, the converter's efficiency closely matches the efficiency of the (current source) test load. With the processor load at f_{CPU} = 6 MHz, the converter operates with a peak efficiency of 86%. The processor's load power is adjusted by changing the operation frequency of the processor load (f_{CPU}) over a range of 5 MHz to 25 MHz.

To adjust for changes in the load, the control voltage (V_{CTRL}) needs to be adjusted. Figure 8b shows the control voltage (V_{CTRL}) required to tune the converter's oscillation frequency (f_{SW}) in order to achieve the efficiencies shown previously in Figure 8a. At V_{BB} = 0 V, increasing the V_{CTRL} is effective in increasing the P_{OUT} up to approximately 5 µW. At P_{OUT} = 5 µW, the drive strength of the charge-transfer is limited with V_{BB} = 0 V. Moving to larger P_{OUT} (>5 µW) requires the back-gate

biasing to be increased to V_{BB} = 1 V. The measured results of nine test chips in Figure 8b show the distribution of V_{CTRL} required to meet a sleep ($P_{OUT} \approx$ 200 nW) and an active load ($P_{OUT} \approx$ 100 µW). The standard deviation of V_{CTRL} at the larger load power (i.e., active load) is a result of the larger V_{BB} (i.e., 1 V). Increasing V_{BB} decreases the transistors V_{th}. For a fixed VGS, a lower V_{th} results in an increased inversion level within the (leakage-based) delay cell transistors. As a result, V_{CTRL} is less sensitive to intra-die variations at the active load. The V_{CTRL} is adjusted using an off-chip voltage source; adding closed-loop control circuitry of V_{CTRL} to meet load power demands has minimal impact on conversion efficiency [8], even by the lowest load power supported in this work (i.e., 79 nW).

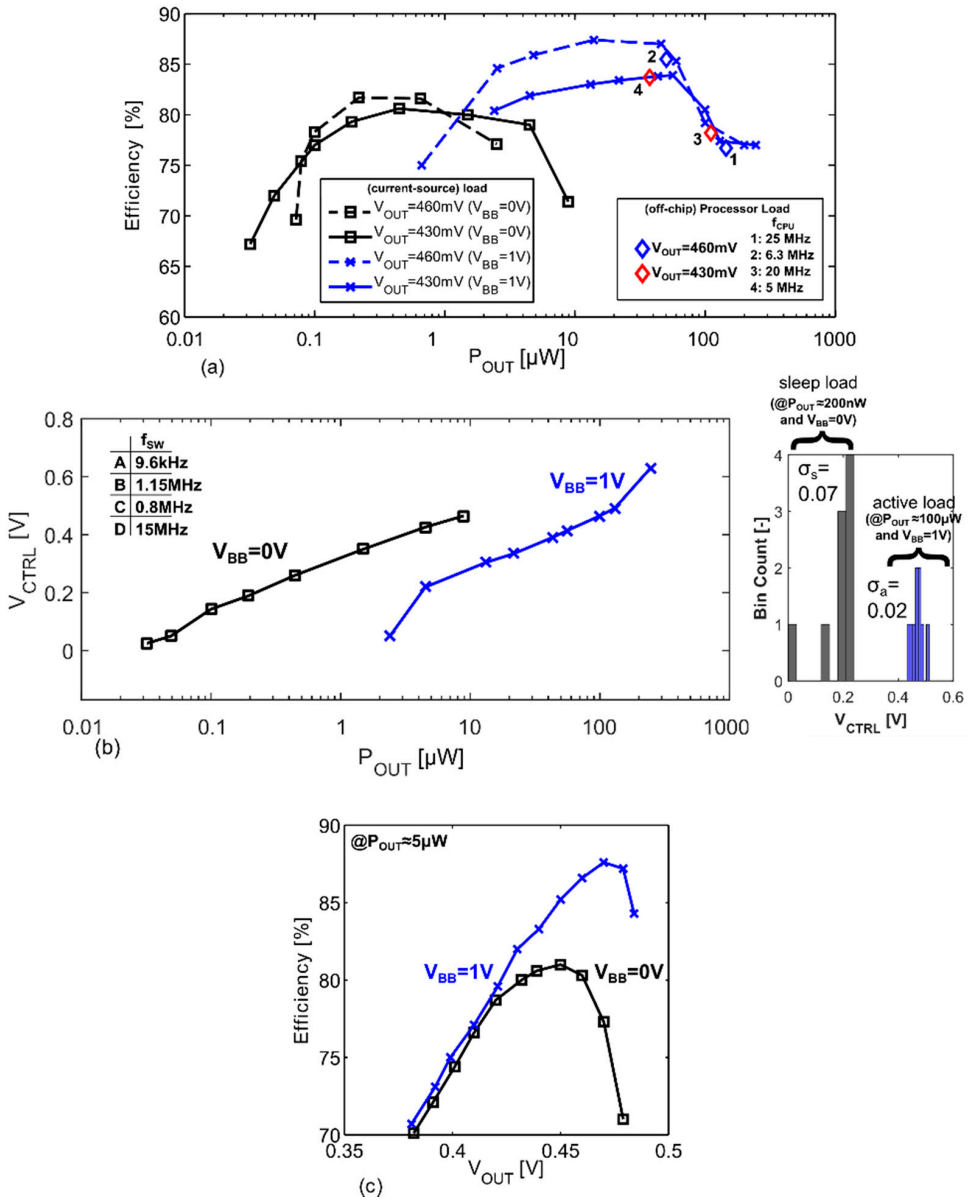


Figure 8. Measurement results of the 2:1 converter; (**a**) Efficiency vs. load power; (**b**) V_{CTRL} vs. load power at V_{OUT} = 430 mV and the standard deviation of V_{CTRL} at a sleep load power of 200 nW and an active load power of 100 µW from nine test chips; (**c**) Efficiency at $P_{OUT} \approx$ 5 µW.

The efficiency of the converter as a function of V_{OUT} at P_{OUT} = 5 µW is shown in Figure 8c. The output impedance of the converter is reduced by increasing V_{BB} to 1 V. A large V_{BB} increases the switching frequency and drive strength of the charge-transfer switches. This allows for the converter

to achieve larger values of V_{OUT} before efficiency tapers off. At V_{BB} = 0 V and V_{BB} = 1 V, the peak efficiency is at V_{OUT} = 0.45 V and V_{OUT} = 0.47 V, respectively.

In addition to achieving high efficiencies, the converter needs to have high power density (mW/mm^2) in order to be a cost-effective fully integrated solution. Achieving high power density in converters that operate with below-threshold voltage levels is challenging to the low overdrive voltages of the charge-transfer switches [15]. State-of-the-art power densities for DC–DC converters with near-threshold output voltages are between 2 and 20 mW/mm^2. By using a self-oscillating converter topology with back-gate biasing, the power density can be significantly improved over the state-of-the-art. The measured power density of the converter for multiple back-gate bias voltages is shown in Figure 9. The power density of the converter can be increased by applying a larger V_{BB}. At V_{IN} = 1 V, the maximum power density is 65 mW/mm^2. At V_{IN} = 1.2 V, the maximum power density is 184 mW/mm^2. The maximum power density is larger at V_{IN} = 1.2 V since there is a larger overdrive on all the switches within the top ring oscillator (switches S_1 and S_2) of the converter. The larger overdrive voltage allows for a larger output current to be driven through the switches, thus giving a larger power density.

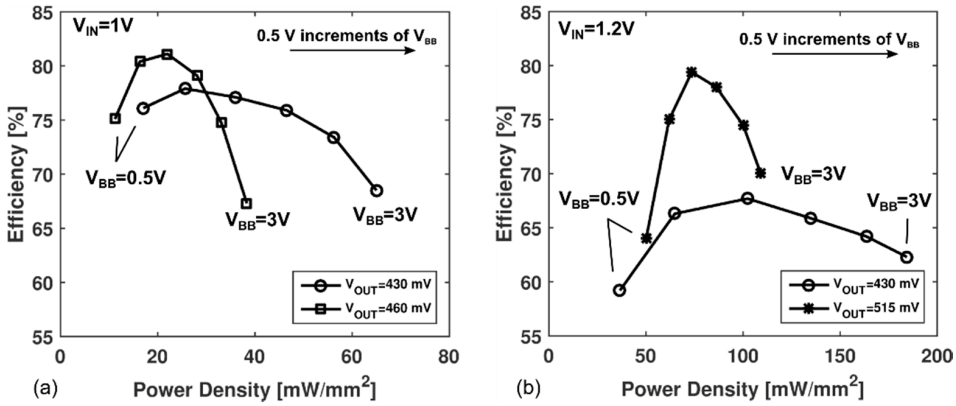


Figure 9. Measurement results of efficiency vs. power density for increasing back-gate bias voltages at (**a**) V_{IN} = 1 V and (**b**) V_{IN} = 1.2 V.

The converter is compared to state-of-the-art SC DC–DC converters in Table 1. The converter from [16] achieves the closest load range performance to the proposed converter, but at a lower power density. The converter in [5] has the closest power density, but it has a much smaller load range. Additionally, the size of C_{OUT} in [5] is not reported. The proposed converter does not use any additional on- or off-chip C_{OUT} and maintains a ripple $\leq$10% of V_{OUT}. In relation to others, the proposed converter has a higher power density and is able to achieve a high minimum efficiency over a larger load power range as highlighted in Figure 10. The load power range is defined as the maximum ($P_{OUT,max}$) and minimum ($P_{OUT,min}$) load power levels at the output of the DC–DC converter.

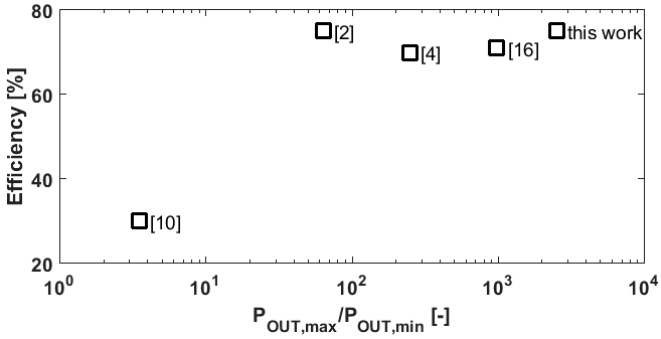


Figure 10. Comparison to state-of-the-art in terms of efficiency and load range (P_{OUTmax}/P_{OUTmin}).

Table 1. Comparison of the self-oscillating 2:1 converter with state-of-the-art SC DC–DC converters.

	[5]	[2]	[4]	[10]	[16]	This Work
Technology	28 nm UTBB FD-SOI	65 nm CMOS	65 nm CMOS	130 nm CMOS	28 nm UTBB FD-SOI	28 nm UTBB FD-SOI
Topology	Step-down SC	Step-down SC	Step-down SC	Step-down SC/LDO	Step-down SC	self-oscillating Step-down SC
C_{OUT}	N/R	3.3 nF	0	0	110 pF	0
Conversion Ratio	3:1, 2:1	2:1	3:1, 2:1, 3:2	5:1	3:1	2:1
Tested Input/Output Voltage	1.1/(0.33, 0.45)	(1–1.2 V)/(0.32–0.48 V)	1.2 V/(0.3–0.6 V)	(2.5–3.6 V)/(0.44 V)	(1–1.8 V)/(0.3–0.55 V)	(1–1.2 V)/(0.380–0.485 V)
Load Range	130–5000 µW [1]	5–320 µW [1]	2–500 µW [1]	100–350 nW [1]	209 nW–205 µW	[3] 79 nW–200 µW
Load Range in Ratio	1:39	1:64	1:250	1:125	1:981	[3] 1:2532
Load Range Min. Efficiency (η_{MIN})	N/R	η_{MIN} = 75%	η_{MIN} = 70%	η_{MIN} = 30%	η_{MIN} = 71%	[3] η_{MIN} = 75%
Efficiency peak	75%@0.45 V	81%@0.4 V	78%@0.5 V	56%@0.44 V	76%@0.415 V	87%@0.46 V
Efficiency (η) @ Sub-/Near-V_{th}	75%@0.45 V	76%@0.4 V	75%@0.5 V	56%@0.4 V	76%@0.415 V	75%@0.515 V 77%@0.46 V
Power Density @ η (mW/mm^2)	18.4@0.45 V	[2] 4.6@0.4 V	2.05@0.5 V	0.0006@0.4 V	5.5@0.415 V	62@0.515 V 19.2@0.46 V

[1] Estimated from paper; [2] does not include area of C_{out}; [3] V_{IN} = 1 V and V_{OUT} = 460 mV; N/R: not reported.

4. Conclusions

A fully integrated step-down self-oscillating switched-capacitor DC–DC converter was presented. The converter was fabricated in 28 nm UTBB FD-SOI. The self-oscillating topology and utilization of back-gate biasing allowed the converter to achieve high efficiency over a large load power range. A minimum efficiency of 75% for 79 nW to 200 µW loads was achieved. Similar efficiency results were achieved with an off-chip processor in active mode. The converter's peak efficiency with an off-chip processor load is 86% at V_{OUT} = 460 mV. The power density is over 60 mW/mm^2 with back-gate biasing of $V_{BB} \geq 1$ V. The large load power range, high power density, and high efficiency make the proposed converter an excellent match for near-threshold energy-constrained processors.

Acknowledgments: Academy of Finland #270585, Almari EU grant #621439, T.I.F.C.F., and the (former) Graduate School in Electronics, Telecommunications and Automation.

Author Contributions: Matthew Turnquist designed the reported DC–DC converter, performed the circuit analysis, and wrote the manuscript. Markus Hiienkari assisted in the measurements. Jani Mäkipää and Markus Hiienkari reviewed the manuscript. Lauri Koskinen supervised the work and contributed to the idea.

Conflicts of Interest: The authors declare no conflict of interest.

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