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A 300-mV ΔΣ Modulator Using a Gain-Enhanced, Inverter-Based Amplifier for Medical Implant Devices

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Abstract: An ultra-low-voltage low-power switched-capacitor (SC) delta-sigma (ΔΣ) modulator running at a supply voltage as low as 300 mV is presented for biomedical implant devices, e.g., cardiac pacemakers. To reduce the supply voltage, an inverter-based amplifier is used in the integrators, whose DC gain and gain-bandwidth (GBW) are boosted by a simple current-mirror output stage. The full input-feedforward loop topology offers low integrators internal swing, supporting ultra-low-voltage operation. To demonstrate the concept, a second-order loop topology was chosen. The entire modulator operates reliably against process, voltage and temperature (PVT) variations from a 300 mV ± 10% supply voltage only, while the switches are driven by a charge pump clock boosting scheme. Designed in a 65 nm CMOS technology and clocked at 256 kHz, the simulation results show that the modulator can achieve a 64.4 dB signal-to-noise ratio (SNR) and a 60.7 dB signal-to-noise and distortion ratio (SNDR) over a 1.0 kHz signal bandwidth while consuming 0.85 μW of power.

Keywords: delta-sigma modulator; gain-enhanced inverter-based amplifier; biomedical implant devices; clock boosting; ultra-low voltage; low power

1. Introduction

Supply voltage reduction, as a direct consequence of the process technologies' scaling, is further enforced by battery-operated biomedical implant devices, such as pacemakers, cardiac defibrillators and neural recording integrated circuits, to make their operating supply compatible with human body potentials [1,2], in the range of few hundreds of mVs. Therefore, designing analogue-to-digital converters (ADCs) operating at a very low supply voltage is inevitable for the measurement of various electrophysiological signals (e.g., ECGs, EEGs, *etc.*).

Pacemakers need to sense the cardiac signals, which mainly are situated in very low frequencies from nearly DC to several hundred hertz [3–7]. The cardiac signals are sensed by the low-noise amplifier, amplified by a gain stage; the undesired interferences are filtered out, and then, the detected analog signal is digitized by a back-end ADC. The ADC architecture and circuit design play a key role in maintaining ultra-low-power efficiency while providing a high conversion accuracy (or resolution). ADC resolutions from eight bit to 13 bit have been reported previously [5–7]. The low frequency noise, including flicker noise, needs to be treated properly in the circuit implementation.

There are two critical factors that can determine the lowest operating power supply of the traditional sigma-delta (ΔΣ) modulators: operational transconductance amplifiers (OTAs) in the integrators and the adequate driving voltage of the switching transistors [8–14]. The conventional analog circuit topologies are no longer practical in ultra-low-voltage operations (below 0.6 V), and also, stacking more than two transistors is impossible due to the limited overdrive and voltage headroom. The inverter is the simplest amplifier, which can sustain a supply voltage of less than the sum of

the absolute threshold voltages of the NMOS and PMOS transistors [12], also known as a Class-C inverter. The DC gain and gain-bandwidth product (GBW) of the CMOS inverter degrade significantly at supplies far below the nominal $V_{TN} + |V_{TP}| = 0.62$ V and need to be enhanced for a robust and high-performance modulator design. Chae and Han [12] proposed an inverter-based ΔΣ modulator using a cascode inverter for boosting the DC gain. In this paper, we present a fully-differential second-order feedforward ΔΣ modulator for ultra-low-voltage low-power biomedical applications, which uses a novel gain-enhanced inverter-based, current mirror amplifier to replace the OTA in the integrators. Moreover, a clock boosting scheme is used to sufficiently drive the switching transistors. While all transistors operate at gate voltage less than 300 mV, the effective gate voltage of the switches is 600 mV with the aid of a charge pump clock doubler [13]. The single-bit quantizer, including the preamplifier, dynamic comparator and latch, was designed in a deep sub-threshold regime, providing very high power efficiency.

The rest of the paper is organized as follows: Section 2 describes the proposed gain-enhanced inverter-based amplifier and its advantages and drawbacks. Section 3 discusses the modulator architecture and its low-voltage and low-power design considerations. Section 4 presents the modulator circuit design. Section 5 discusses the simulation results. In Section 6, the proposed modulator is compared to the reported state-of-the-art ultra-low-voltage modulators. Conclusions are drawn in Section 7.

2. Proposed Gain-Enhanced Inverter-Based OTA

A novel inverter-based amplifier is proposed for ultra-low-voltage applications, which is composed of a Class-C inverter and a current mirror output stage. Figure 1 shows the schematics of the basic CMOS inverter, the cascode inverter and the proposed inverter-based, current mirror OTA (Figure 1c).

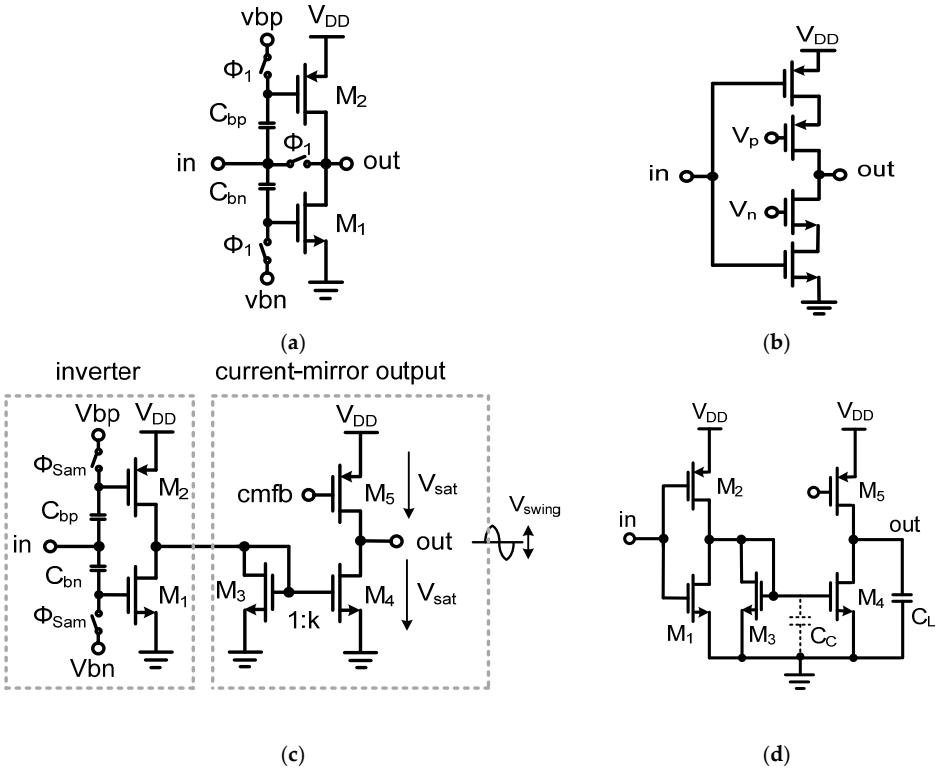


Figure 1. Schematic of the inverter amplifiers: (**a**) conventional CMOS inverter with biasing; (**b**) cascode inverter; (**c**) inverter-based current-mirror operational transconductance amplifier (OTA) using an input inverter stage and a current mirror output stage; single-ended is shown; (**d**) parasitic capacitance at internal node.

A switched-capacitor (SC) biasing scheme using floating capacitors C_{bp} and C_{bn} (Figure 1c) is used to define the operating point of the inverter M_1–M_2. These capacitors are periodically refreshed by the bias voltages *Vbn* and *Vbp* during the sampling phase ϕ_{Sam} ($\phi_{Sam} = \phi_{1d}$ in the first integrator; $\phi_{Sam} = \phi_{2d}$ in the second integrator) and work as floating batteries between the input and the gates of the transistors. It is worth mentioning that the pre-charging *Vbn* and *Vbp* occurs simultaneously with sampling the signal onto C_{S1} (C_{S2}) and the inverter offset onto C_{C1} (C_{C2}) in phase ϕ_{Sam} (Figure 4). The sampling clock speed is low (*i.e.*, 256 kHz), so initially, the $C_{bp} = C_{bn} = 0.5$ pF are charged in the early phase of ϕ_{Sam} ($C_{bp} = C_{bn} << C_{Ci}$), and then, the amplifier is placed in the unity feedback configuration for offset sampling when its biasing was set appropriately. The *Vbp* and *Vbn* are generated using a constant-g_m biasing circuit followed by a level shifter to eliminate the V_{sat} problem as in [15], which provides wider overdrive voltage and, in turn, a smaller transistor width. At the output stage, an energy-efficient SC common-mode feedback (CMFB) circuit is employed [8], which derives the gate of PMOS transistor M_5, in order to set the output CM level at the middle of the supply voltage for the maximum output swing.

The DC gain and GBW of the CMOS inverter degrade significantly at supplies far below the nominal $V_{TN} + |V_{TP}|$, which need to be enhanced for a robust and high-performance modulator design. The aim of the proposed technique is to boost the gain and GBW simultaneously by mirroring a small fraction (~10%) of the bias current of the inverter M_1–M_2 through transistor M_3 to the output. The factor *k* is the current ratio of the current mirror M_3–M_4 and is defined as $(W/L)_{M4}/(W/L)_{M3}$. The approximate gain and GBW of the proposed amplifier shown in Figure 1c can be determined from its small-signal model using sub-threshold current as:

$$A_{en} = \frac{g_{m1} + g_{m2}}{g_{m3} + g_{ds1} + g_{ds2} + g_{ds3}} . \frac{g_{m4}}{g_{ds4} + g_{ds5}}$$

$$\cong (g_{m1} + g_{m2}) \times k \times R_{out} \quad (1)$$

$$GBW = \frac{k \times (g_{m1} + g_{m2})}{2\pi C_L} = \frac{k(2-\alpha) I_{D2}}{2\pi C_L n V_T} \quad (2)$$

where g_{mi} and g_{dsi} represent the transconductance and output conductance of the *i*-th transistor, respectively. R_{out} is the total output resistance, which is equal to $(g_{ds4} + g_{ds5})^{-1}$. C_L is the total load capacitor for the frequency compensation. *n* and V_T are the sub-threshold parameters. We consider $\boldsymbol{\alpha} = I_{D3}/I_{D2}$ as the ratio of the currents of M_3 and M_2. In addition, it can be shown that the term $g_{m4}/(g_{m3+}\ g_{ds1} + g_{ds2} + g_{ds3})$ is approximately equal to *k*. A large device size of M_1–M_2 has to be prevented, as it creates large parasitic capacitors, which can limit the amplifier speed.

To explain the gain-enhancement technique, the DC gain of the basic inverter (Figure 1a) and the proposed amplifier (Figure 1c) given by Equation (1) can be written in the following forms in Equations (3) and (6):

$$A_0 = (g_{m1} + g_{m2}) R_{out} = \frac{2I_D}{nV_T} \times \frac{1}{\lambda I_D} = \frac{2}{n\lambda V_T} \quad (3)$$

V_T is the thermal voltage; *n* is the non-ideality factor; and $\boldsymbol{\lambda}$ is the channel length modulation coefficient. A_0 is the intrinsic gain achieved by an inverter in the sub-threshold regime. In deep submicron technologies, by shrinking the transistor length, the effect of channel length modulation becomes more important. As a consequence, the output resistance and, thus, the DC gain of the inverter are normally low.

In Figure 1c, the bias current of the diode-connected device (*i.e.*, I_{D3}) is equal to $\boldsymbol{\alpha}\ I_{D2}$, where $\boldsymbol{\alpha}$ in this design is approximately 0.1. The M_1 transistor then shunts the rest of the current to the ground. Assuming M_1 carries $(1 - \boldsymbol{\alpha}) \times I_{D2}$, from Equation (1), the gain of the proposed OTA can be expressed as:

$$A_{en} = (g_{m1} + g_{m2}) \times k \times R_{out} = \left[\frac{(1-\alpha) I_{D2}}{nV_T} + \frac{I_{D2}}{nV_T} \right] \times k \times \frac{1}{\lambda_4 I_{D4}} \quad (4)$$

Now, the biasing current of M_4 is:

$$I_{D4} = k \times I_{D3} = k \times \alpha I_{D2} \tag{5}$$

Finally, the enhanced gain of the OTA is given by:

$$A_{en} = \frac{2-\alpha}{2\alpha} \times \frac{2}{n\lambda V_T} = (\frac{1}{\alpha} - 0.5)A_0 \tag{6}$$

From Equation (6), it can be seen that the gain is enhanced $(1/\alpha - 0.5)$-times. The gain increase can be adjusted by the α factor during the design. With α = 0.1 in this design, the gain can be enhanced 9.5-times directly from Equation (6). With $\alpha = I_{D3}/I_{D2}$ as the ratio of the currents in M_3 and M_2, the current mismatch can affect the gain enhancement (Section 2.2). In typical corner simulation from a 0.3 V supply, the α factor is about 0.12, which corresponds to a gain enhancement of eight-times, whereas in the worst-case corner, it is approximately 0.13, corresponding to a gain enhancement of seven-times.

Figure 2a shows the variations of the DC gain with respect to the supply voltage (V_{DD}) for the basic inverter shown in Figure 1a and the gain-enhanced inverter shown in Figure 1c. Figure 2b,c also shows the variations of the GBW as a function of the V_{DD} for both the basic inverter and the gain-enhanced inverter. For PMOS transistor M_2, the overdrive voltage (*i.e.*, $V_{DD} - Vbp - |V_{TP}|$) depends on V_{DD} and increases by increasing V_{DD}. Similarly, for NMOS device M_1, the overdrive voltage (*i.e.*, $Vbn - V_{TN}$) is enhanced linearly with V_{DD} to accommodate a wider input linear range in this analysis.

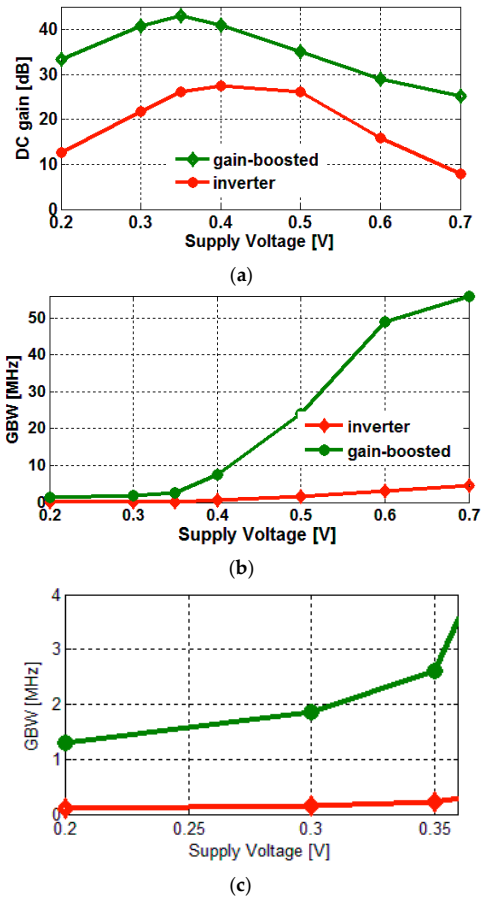


Figure 2. (**a**) DC gain and (**b**) gain-bandwidth (GBW) variations *versus* supply voltage for the CMOS inverter shown in Figure 1a and the proposed gain-enhanced, inverter-based amplifier shown in Figure 1c; (**c**) the zoomed version of the Figure 2b for clarity.

For V_{DD}s far below $V_{TN} + |V_{TP}|$, the DC gain and GBW degrade significantly. A large device size in M_1–M_2 has to be avoided, as this creates large parasitic capacitances, which can limit the OTA performance. The aim of this work is to enhance the gain and GBW simultaneously by mirroring a small fraction of the bias current of the inverter M_1–M_2 to the output stage (with $\alpha \sim 10\%$ and $k = 8$).

Shown in Figure 2, with the current mirror gain-enhancement technique, the simulated DC gain and GBW increase to 40 dB and 1.9 MHz from 22 dB and 0.38 MHz, respectively, from a 0.3 V supply and a 3 pF load capacitance in a typical (TT) process corner, at 27 °C. The phase margin is 66 °C. The transistors sizes of the developed inverter-based current mirror amplifier are summarized in Table 1. The DC gain gets worse in FS (fast NMOS, slow PMOS) and SF (slow NMOS, fast PMOS) process corners (*i.e.*, 37 dB at V_{DD} = 0.3 V), whereas its deviation is trivial for FF and SS corners (*i.e.*, 39 dB at V_{DD} = 0.3 V).

Table 1. Transistor aspect ratios and bias setting for the gain-enhanced current mirror inverter amplifier in a 65 nm CMOS.

Transistor	W/L (μm/μm)
M_1	1/0.8
M_2	9/0.8
M_3	2/0.2
M_4	16/0.2
M_5	5/0.25
Capacitor	**Value (pF)**
$C_{bn} = C_{bp}$	0.5
C_{Load}	3.0

In practice, the gain enhancement can be restricted by several factors: phase margin, matching of bias currents between the M_1 and M_3 transistors and thermal noise. These factors are discussed below.

2.1. Frequency Response and Internal Parasitic Pole

Using the gain-enhancement technique increases the impedance of the internal node at the gate of the diode-connected M_3. The total parasitic capacitance at this node is represented by C_P in Figure 1d. The parasitic non-dominant pole due to the impedance $1/g_{m3}$ of the transistor M_3 operating in the sub-threshold regime and the parasitic capacitor C_P can be expressed as:

$$P_{nd} = \frac{g_{m3}}{2\pi C_P} = \frac{\alpha I_{D2}}{2\pi C_P n V_T} \tag{7}$$

where C_P is approximately $C_{gs3} + C_{gs4}$. To maintain a reasonably safe phase margin, the P_{nd} has to be placed more than three-times the unity GBW given by Equation (2). Thus, the following criteria for α can be derived with respect to C_P/C_L and k:

$$\frac{1}{\alpha} - 0.5 \leqslant \frac{1}{6k}\frac{C_L}{C_P} \tag{8}$$

Recalling $(1/\alpha - 0.5)$ in Equation (6) as the gain-enhancement factor, Equation (8) represents the maximum gain-enhancement that can be achieved by the proposed technique. The larger the C_L/C_P, the greater is the gain enhancement and the phase margin, but this costs more power. The dominant pole in this design is set by C_L, which can be expressed by:

$$P_1 = \frac{1}{2\pi R_{out} C_L} = \frac{g_{ds4} + g_{ds5}}{2\pi C_L} \tag{9}$$

2.2. Bias Current Matching

As described earlier, the ratio of the bias currents of transistors M_3 and M_2, defined as $\alpha = I_{D3}/I_{D2}$, plays an important role for enhancing the amplifier gain given by Equation (6). Practically, the matching between $I_{D3} = \alpha\ I_{D2}$ and $I_{D1} = (1 - \alpha)\ I_{D2}$ determines the real α factor and, thus, the gain enhancement. To ensure good matching between those currents, the gate bias voltages of M_1–M_2 both are generated from the same reference current source using current mirrors. For good matching, transistors should be sized properly.

2.3. Thermal Noise

A drawback of the gain-enhanced, inverter-based amplifier, as compared to the basic CMOS inverter, is that it exhibits more input-referred thermal noise, related to the g_{m3} of the device M_3. Since the correlated double-sampling (CDS) technique, as an auto-zeroing technique, is used in the corresponding integrator, the low frequency flicker noise is attenuated at the cost of an increased white noise floor due to the noise folding accompanied by the sampling [16]. The foldover thermal noise of the integrator is the dominant source of the noise, in which the thermal noise is amplified by a factor GBW/f_S, with sampling frequency f_S [16]. As a result, the input-referred noise power of the Class-C inverter and the gain-enhanced inverter shown in Figure 1c, denoted by *GE-inv*, can be expressed, respectively, as:

$$\overline{V^2_{n-fold,inv}} = \frac{GBW}{f_s}.\frac{4kT\gamma}{g_{m1}+g_{m2}}\left[v^2/Hz\right] \tag{10}$$

$$\overline{V^2_{n-fold,GE-inv}} = \frac{GBW}{f_s}.\frac{4kT\gamma}{g_{m1}+g_{m2}}(1+\frac{g_{m3}}{g_{m1}+g_{m2}})\left[v^2/Hz\right] \tag{11}$$

where the noise of the gain-enhanced amplifier has an additional term corresponding to g_{m3}. Therefore, M_3 has to be sized carefully, such that the thermal noise is minimized and the non-dominant pole, *i.e.*, $g_{m3}/2\pi C_P$ with C_P the parasitic capacitance at the gate of M_3 and M_4, is placed more than 3× the GBW for a reasonably safe phase margin.

3. Modulator Architecture

Output swing is of great importance in ultra-low-voltage low-power designs, which directly determines the modulator dynamic range (DR) and, ultimately, the power consumption. The minimum swing V_{swing} that the amplifier shown in Figure 1c can still operate with imposes a hard limit equal to $2V_{sat} + V_{swing}$ for the supply voltage scaling, with saturation voltage V_{sat}. The limited voltage swing is therefore translated into the demanding requirement of a low-swing loop topology. Compared to the traditional feedback topology, the full input-feedforward architecture suggests the integrators to process only the quantization error, thereby reducing the integrators' swing considerably [17]. This is beneficial for the amplifiers' relaxed requirements for slew-rate. Figure 3a shows the input-feedforward loop architecture for a second-order modulator. Half-cycle delay integrators are adopted in this structure to realize the CDS scheme for the inverter's offset cancellation. The loop coefficients were optimized with behavioral simulations as ($a_1\ a_2\ c_1\ c_2\ c_3$) = (0.1 0.6 1 7 1). The coefficients are determined from the loop stability constraint, the maximum linear swing of the integrators and the required SNR. Figure 3b depicts the magnitude of the signal transfer function (STF) and the noise transfer function (NTF) of the target modulator. As expected, the STF is unity, and the NTF has a 40 dB/dec noise suppression in the baseband.

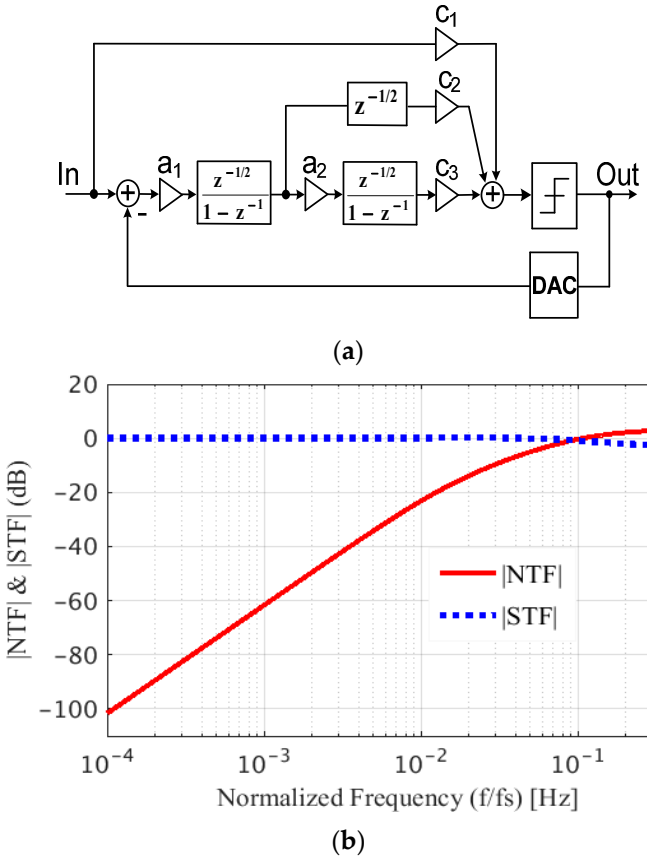


Figure 3. (**a**) The scaled modulator input-feedforward architecture using a second-order loop filter and a single-bit quantizer. Integrators with half-cycle delay were used to adopt the built-in correlated double-sampling (CDS) scheme for offset cancellation and 1/f noise attenuation; (**b**) the magnitude of the noise transfer function (NTF) and signal transfer function (STF) of the modulator with respect to the normalized frequency.

The single-bit quantizer is inherently linear. A multi-bit quantizer is not preferable for the low power and moderate resolution in this application, because the internal DAC becomes nonlinear, requiring dynamic element matching (DEM) or other complementary techniques for DAC linearization, which increase the hardware complexity and, thus, the total power consumption.

4. Modulator Circuit Design and Building Blocks

In this section, the details of modulator circuit design and its building blocks are discussed.

4.1. Modulator Circuit

Figure 4 shows the schematic of the designed second-order SC ΔΣ modulator using the proposed pseudo-differential integrators. The SC CMFB circuit is not shown and is omitted for simplicity. The proposed inverter-based amplifier in feedback configuration does not provide a virtual ground at the integrator input, because it has only one input terminal (Figure 1c). Combined with the CDS technique to cancel out the input offset and to attenuate the 1/f noise [16], two instances of the designed inverter-based amplifier are used to realize a pseudo-differential integrator with a virtual ground. There is a half-cycle delay between the integrators, *i.e.*, when the first integrator samples the input onto C_{S1} and the offset of the inverter onto C_{C1}, the second integrator is in charge transfer phase and *vice versa*. Since all feedforward paths have to create full delay paths according to Figure 3a, a half-cycle delay element is inserted in the internal feedforward path using SC implementation.

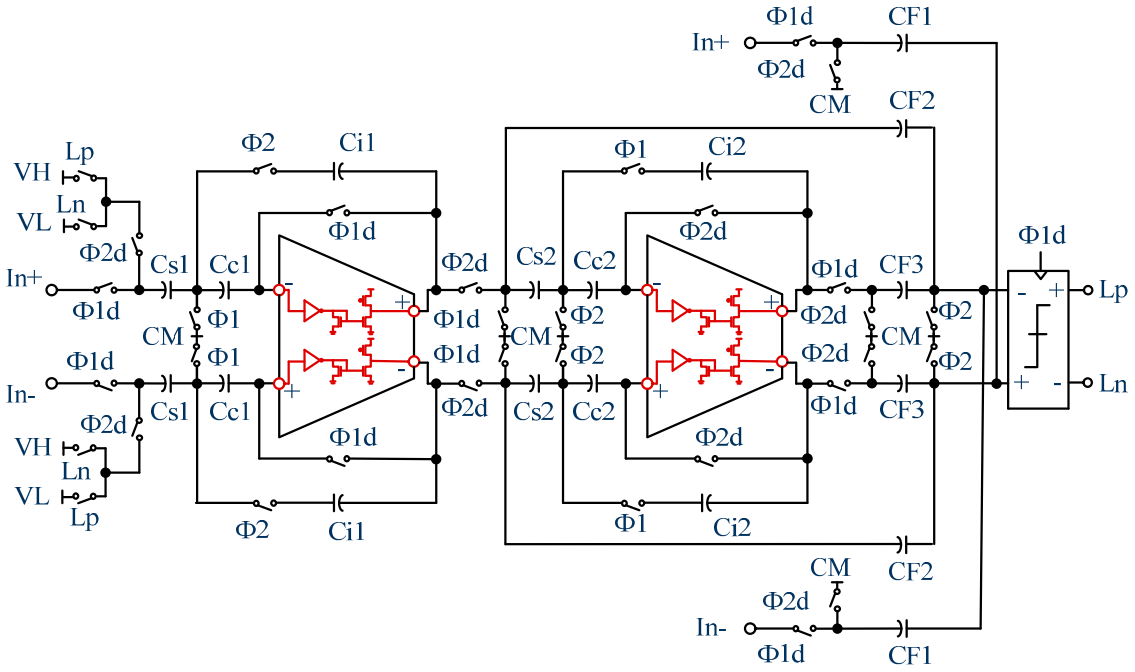


Figure 4. Schematic diagram of the one-bit second-order switched-capacitor (SC) delta-sigma modulator using pseudo-differential integrators. Each integrator circuit shown in red represents the proposed inverter-based current mirror amplifier discussed in Section 2. VH and VL denote the positive and negative reference voltages. CM, common mode.

The summation of the feedforward paths is realized by the parallel capacitor branches at the quantizer input by using an SC passive network. The feedforward architecture is preferable due to its relaxed OTA's performance requirements and low internal swings.

4.2. Low-Voltage Clocking and Clock-Boosting Circuitries

Figure 5 shows the non-overlapping clock generation circuitry used to provide the clock timing required by the modulator. The entire circuit employs low-V_{TH} low-power (LVTLP) devices enabling operation at 300 mV. The transistor aspect ratios of the CMOS inverters and the output buffers are specified in µm/µm in the figure. The aspect ratios of the CMOS NAND gate for PMOS and NMOS devices are 0.24 µm/1.5 µm and 0.135 µm/1.5 µm, respectively. In order to open and close the switches properly, they are implemented as transmission gates with low-V_{TH} transistors, driven by an ultra-low-voltage charge-pump clock doubler [13].

Figure 6 shows the schematic of the clock boosting circuit, which is composed of a charge-pump voltage doubler with two cross-coupled NMOS devices, two capacitors as large as 5 pF and two inverters as the buffer and level shifter. Low-V_{TH} devices were employed in the charge-pump circuit and level shifters for low voltage operation at 300 mV. The $\phi 1L$ and $\phi 2L$ are two non-overlapping clocks generated by the circuit in Figure 5 with a voltage level equal to 0.3 V, whereas $\phi 1H$ and $\phi 2H$ are level shifted up to 0.6 V. Hereafter, for simplicity, we denote $\phi 1H$ and $\phi 2H$ as $\phi 1$ and $\phi 2$, as in Figure 4. In a similar way, the $\phi 1d$ and $\phi 2d$ are generated and level shifted.

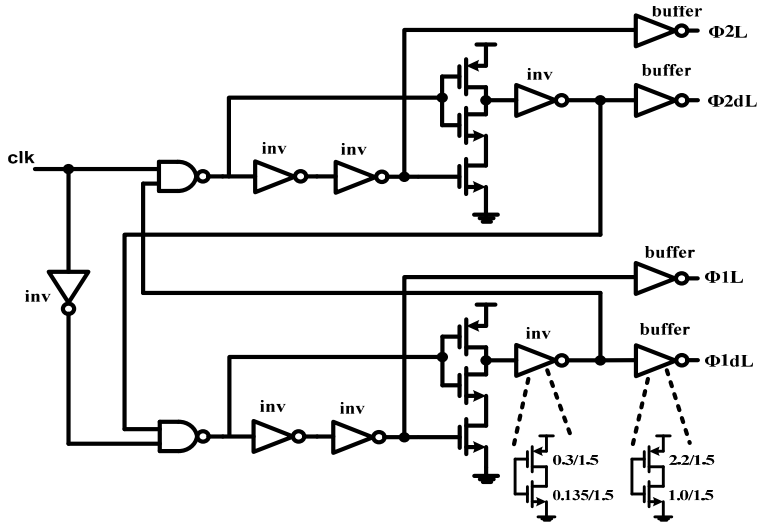


Figure 5. Clock generation circuitry using low-V_{TH} low-power (LVTLP) devices. The transistor aspect ratios of the inverters and the output buffers are given in μm/μm. This provides two non-overlapping clocks ($\phi 1L$, $\phi 2L$) and their delays ($\phi 1dL$, $\phi 2dL$) to avoid signal-dependent charge injection.

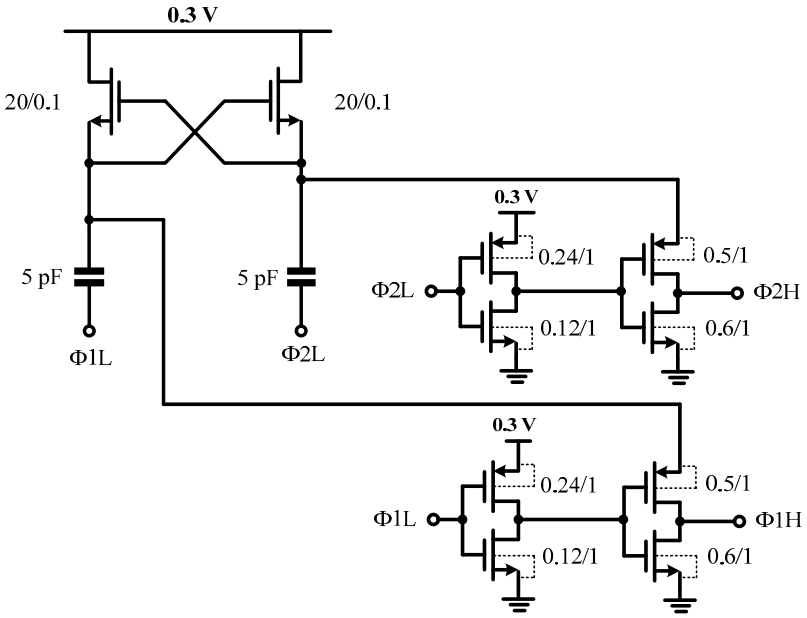


Figure 6. Clock doubler with a charge-pump circuit and level shifters using low-V_{TH} devices. The transistor aspect ratios are specified in μm/μm.

4.3. Ultra-Low-Voltage Sub-Threshold Quantizer

The single-bit quantizer is implemented using a dynamic comparator preceded by a single-stage preamplifier, as shown in Figure 7. Table 2 summarizes the transistors dimension in μm. At a 0.3 V supply, the regular preamplifier and comparator circuits do not function properly in the strong inversion.

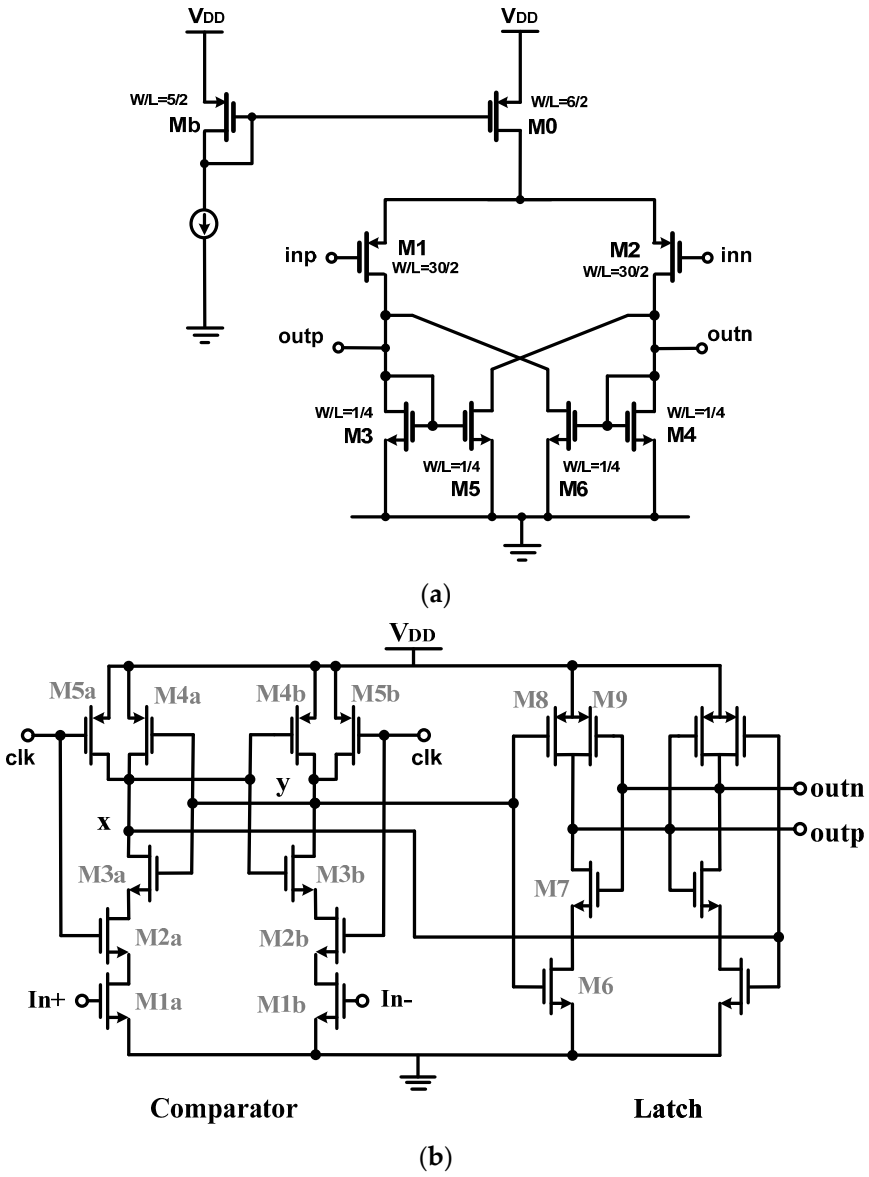


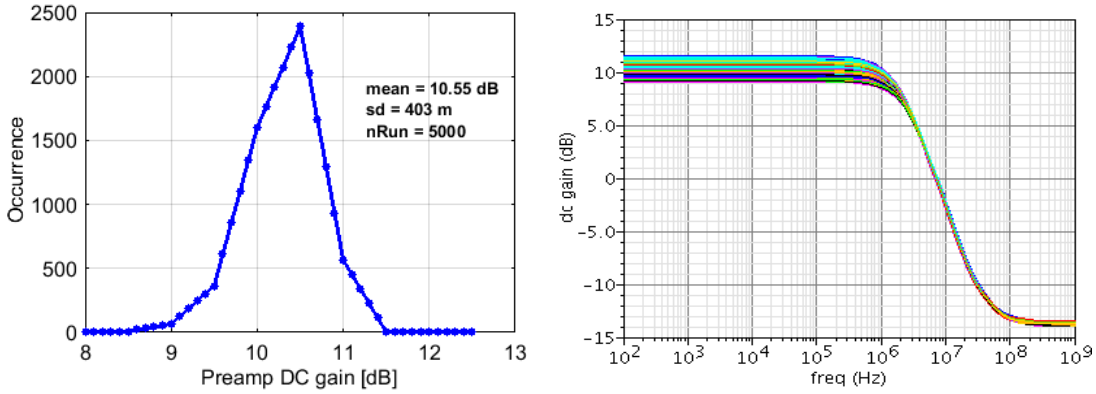
Figure 7. (**a**) Low-voltage differential gain-enhanced preamplifier circuit operating in the sub-threshold regime. The transistors aspect ratios are specified in μm/μm. (**b**) Low-voltage dynamic comparator and latch designed in the sub-threshold regime. The transistors aspect ratios are summarized in Table 2.

Table 2. Transistor aspect ratios of the clocked comparator and latch designed in the sub-threshold regime.

Transistors in Comparator	W/L (μm/μm)
M_{1a}/M_{1b}	8/0.18
M_{2a}/M_{2b}	4/0.18
M_{3a}/M_{3b}	3/0.18
M_{4a}/M_{4b}	25/0.18
M_{5a}/M_{5b}	30/0.18
Transistors in Latch	**W/L (μm/μm)**
M_6	1/0.18
M_7	0.5/0.18
M_8	1/0.18
M_9	1/0.18

The input signals have a common-mode level equal to 0.15 V (*i.e.*, $V_{DD}/2$), which is not adequate to turn on the input transistors. The threshold voltage of the used low-V_{TH} transistors in this technology itself is more than 0.15 V. On the other hand, stacking more than three transistors is impractical. Therefore, the single-bit quantizer (including the preamplifier circuit and the dynamic comparator and latch) is designed in the deep sub-threshold regime, providing very high power efficiency. The entire circuit dissipates only 6 nW, while clocked at 256 kHz. The quantizer operating at 0.3 V $\pm$ 10% was simulated against process, voltage and temperature (PVT) variations. It is capable of detecting an input signal as low as 200 µV, whereas the modulator's least significant bit (LSB) is 300 µV for a full-scale reference voltage of 300 mV and 10 bit resolution.

The gain of the preamplifier degrades to 5 dB at a 0.3 V supply. Thus, it employs a gain-enhanced positive feedback in order to boost the low-frequency gain [2]. The preamplifier exploits low-V_{TH} transistors, providing more headroom for ultra-low voltage operation. For robust function against PVT variations, the effect of mismatch and process variations over DC gain was simulated using Monte Carlo analysis. Figure 8a shows the histogram of the DC gain for 5000 runs, which demonstrates the mean value of 10.55 dB. The frequency response was also simulated for 1000 runs, as depicted in Figure 8b. The worst-case DC gain in this plot is more than 9 dB.



(**a**) (**b**)

Figure 8. (**a**) Histogram of the DC gain of the low-voltage preamplifier shown in Figure 7a operating in the sub-threshold regime from the Monte Carlo simulations; (**b**) Bode plot of the frequency response from Monte Carlo simulations.

5. Simulation Results

The proposed 0.3 V delta-sigma modulator was designed and simulated in a 65 nm CMOS process. Figure 9 shows the output power spectrum for a −2 dB full-scale (dBFS), 226 Hz sine-wave input. Figure 10 shows the power spectrum for a 960 Hz input, near the signal bandwidth edge, with a full scale input amplitude (*i.e.*, 0 dBFS). The differential input signal range is 500 mV_{pp}. The modulator performance is simulated against process corners and 10% supply voltage variations, the achieved worst-case peak SNR and SNDR are 64.4 dB and 60.7 dB, respectively, within a 1.0 kHz signal bandwidth with a 256 kHz sampling clock frequency. The total power consumption from a 0.3 V power supply is 0.85 µW, in which the digital power is only 9%, including clock generation and clock boosting circuitries. Figure 11 presents the modulator SNDR *versus* the input differential amplitude in dBFS. The performance metrics are summarized in Table 3. The resulting figure of merit (FOM) is 0.46 pJ/conversion-step, by calculating FOM = power/($2^{ENOB} \times 2 \times$ bandwidth) with ENOB as the effective number of bits. The modulator can work up to a 0.5 V power supply.

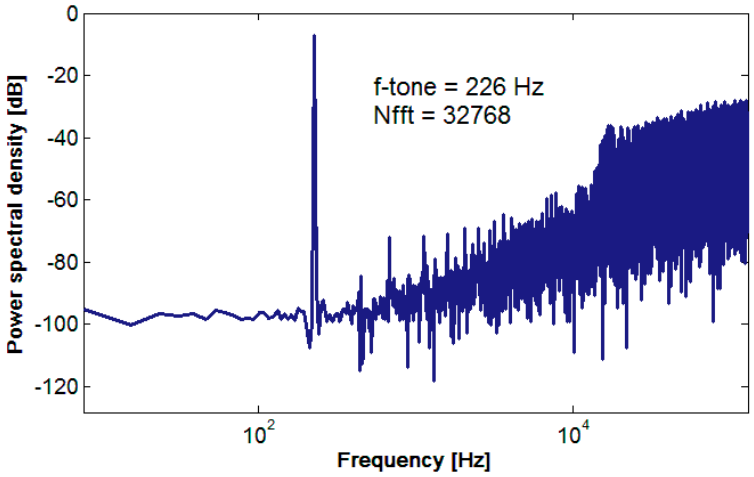


Figure 9. Simulated output power spectrum of the designed modulator for the input signal frequency of 226 Hz with a −2 dBFS amplitude.

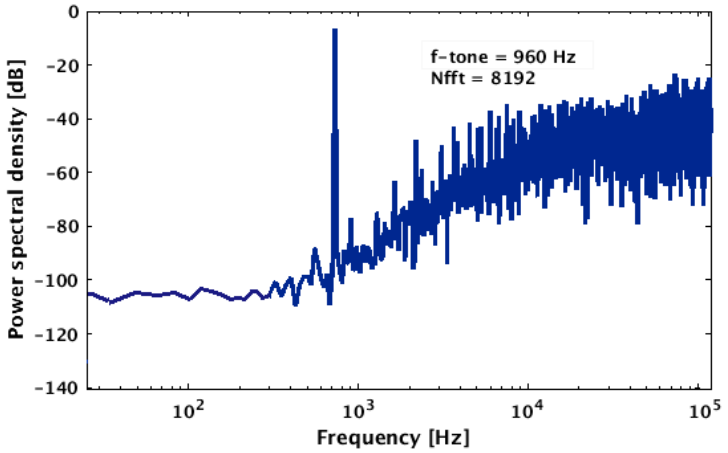


Figure 10. Simulated output power spectrum of the designed modulator for the input signal frequency of 960 Hz and a full-scale amplitude (0 dBFS). The effective signal bandwidth is 1 kHz.

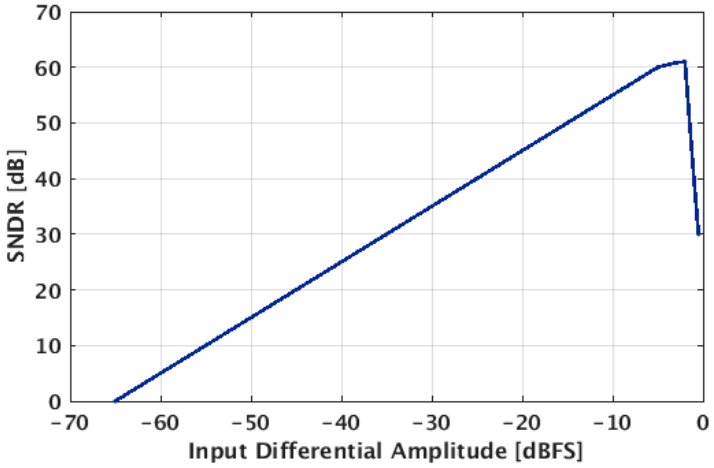


Figure 11. Simulated signal-to-noise and distortion ratio (SNDR) *versus* input differential amplitude in dBFS.

Table 3. Simulated performance results.

Metrics	Simulated Value
Supply voltage	0.3 V
Technology	65 nm CMOS
Clock frequency	256 kHz
Signal bandwidth	1 kHz
Differential input range	0.5 $V_{peak-to-peak}$
Temperature range	0 to 100 °C
Peak SNR	slow corner 64.4 dB typical corner 65.5 dB fast corner 67 dB
Peak SNDR	slow corner 60.7 dB typical corner 62 dB fast corner 63.2 dB
Dynamic range	65 dB
Power consumption	0.85 µW

6. Comparison of the Power Efficiency

The performance of the presented modulator in Sections 4 and 5 is compared to previous state-of-the-art low-voltage modulators in Table 4. Two commonly-used FOMs are employed, which are defined below:

$$FOM_1 = \frac{Power}{2^{(SNDR-1.76)/6.02} \times 2 \times BW} \quad (12)$$

$$FOM_2 = DR_{dB} + 10\log(\frac{BW}{Power}) \quad (13)$$

Table 4. Performance comparison with previously-reported low-voltage low-power delta-sigma modulators. FOM, figure of merit.

Parameters	[15]	[18]	[19]	[9] †	[20]	This Work †
V_{DD} (V)	0.25	0.2	0.3	0.4	0.4	0.3
Bandwidth (Hz)	10 k	20 k	20 k	10 k	20 k	1 k
Power consumption (µW)	7.5	7.5	79.3	0.41	140	0.85
Sampling frequency (Hz)	1.4 M	12 M	2.56 M	2 M	3.2 M	256 k
SNDR (dB)	61	60.3	74	58	68	60.7
DR (dB)	64	68.9	77	64	74	65
Technology (nm)	130	90	130	130	130	65
FOM_1 (pJ/step)	0.477	0.222	0.481	0.032	1.7	0.464
FOM_2 (dB)	155	163	161	168	155.5	156
FOM_3 (pJ.V/step)	0.119	0.044	0.144	0.013	0.68	0.139

† Results from simulation. Other references provide experimental results.

The FOM_1 favors high-resolution ADCs, whereas the FOM_2 favors high-DR ADCs. These FOM definitions disregard V_{DD}, the threshold voltage of the corresponding technology, and the available swing. According to the FOM definitions given above, the designed inverter-based, second-order modulator achieves 0.46 pJ/conversion-step and 156 dB, respectively, which are comparable to the other state-of-the-art modulators operating with supply voltages below 0.4 V. Among others, the passive modulator in [2] operating at a 0.5 V supply consumes the lowest power (only 250 nW) while gaining moderate resolution (65 dB SNDR) and 72 dB DR. It looks attractive when using both FOM definitions given by Equations (12) and (13).

The modulator design in the ultra-low voltage domain (below 0.5 V) is becoming more and more challenging due to the limited available signal swing and switch overdrive voltage. The output swing

of an OTA directly determines the integrators' swing, which indeed defines the modulator reference voltage. As a consequence, the maximum input signal, $V_{in.max}$, that determines the DR of the ADC at a given input-referred noise floor P_n is limited by the reference voltage or the integrators' swing. The DR can be derived as:

$$DR = 10\log\frac{V_{in.\max}^2/2}{P_n + P_D} \tag{14}$$

where P_D is the input-referred distortion. To maintain the same DR in lower supply voltages, the noise floor and distortion power have to be decreased, requiring higher power consumption [21]. Generally speaking, for a better power efficiency, it is not desirable to reduce the supply voltage, because the analog power increases. However, specific applications, such as body implants (e.g., cardiac pacemakers, cochlear implants, *etc.*), demand ultra-low-voltage operation in the order of human body potentials.

It should be noted that the threshold voltage does not scale at the same proportion as the supply voltage, which limits the available overdrive voltage of the operating switches in SC designs. For fair comparisons of the modulators listed in Table 4, in addition to the commonly-used FOM_1 and FOM_2, the proposed FOM_3 takes into account the V_{DD}, as well.

$$FOM_3 = \frac{Power \times V_{DD}}{2^{(SNDR-1.76)/6.02} \times 2 \times BW} \tag{15}$$

In fact, the most effective comparison among different modulators is when we consider the threshold voltage in addition to the supply voltage, V_{DD}, because the available voltage headroom for analog blocks and the overdrive voltage for the switching transistors (*i.e.*, $V_{GS} - V_{TH}$) depend directly on V_{TH}. Therefore, for a fair comparison, we need to consider the term $V_{DD} - V_{TH}$ in the numerator of the FOM_3 given by Equation (15), rather than merely V_{DD}. For simplicity, we assume all technologies used in Table 4 have the same V_{TH}. According to FOM_3 and considering operating V_{DD}, the proposed modulator achieves a competitive figure of merit of 0.139 pJ.V/conversion-step.

7. Conclusions

An ultra-low-voltage, energy-efficient $\Delta\Sigma$ modulator is introduced in this paper for medical implant devices. In the absence of cascoding, a new gain-enhanced inverter-based amplifier was proposed to compensate for the reduced inverter's DC gain and GBW. To overcome the switches' overdrive limitation, the charge pump clock doublers were used to boost the clock signals' level. The single-bit quantizer, including the preamplifier, dynamic comparator and latch, was designed in the deep sub-threshold regime, providing very high power efficiency. The entire modulator operates reliably against PVT variations from a 300 mV $\pm$ 10% supply voltage. The modulator design is compatible with human body potentials, as well as the energy efficiency intended for the target applications.

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Author Contributions: In this research work, the author Ali Fazli Yeknami contributed to the literature search and came up with the idea of the new gain-enhanced inverter-based amplifier technique that can reliably work at supply voltages near 300 mV. He was responsible for simulating the entire delta-sigma modulator against PVT variations, for a comprehensive comparison with other ultra-low voltage designs. The manuscript was written by Ali Fazli Yeknami and proofread for the technical writing and formatting aspects by Gabor C. Temes of Oregon State University. The author also had extensive discussions with Atila Alvandpour at Linköping University from the standpoint of the project specifications and biomedical design requirements.

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