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Article

Assessment of Global Variability in UTBB MOSFETs in Subthreshold Regime †

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Abstract: The global variability of ultra-thin body and buried oxide (UTBB) MOSFETs in subthreshold and off regimes of operation is analyzed. The variability of the off-state drain current, subthreshold slope, drain-induced barrier lowering (DIBL), gate leakage current, threshold voltage and their correlations are considered. Two threshold voltage extraction techniques were used. It is shown that the transconductance over drain current (g_m/I_d) method is preferable for variability studies. It is demonstrated that the subthreshold drain current variability in short channel devices cannot be described by threshold voltage variability. It is suggested to include the effective body factor incorporating short channel effects in order to properly model the subthreshold drain current variability.

Keywords: FD SOI; ultra-thin body and buried oxide (UTBB); variability; subthreshold; threshold voltage; short channel effects

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1. Introduction

Ultra-thin body and buried oxide (UTBB) technology is promising for future MOSFET nodes due to its short channel effects immunity [1] and low variability [2]. The quantification of global variability improves fabrication process optimization and MOSFET model extraction. Whereas threshold voltage variability has been widely studied [3–5], subthreshold variability has received little attention. Characterization of subthreshold variability has become essential nowadays. Design is shifting towards the subthreshold regime for low power applications. Furthermore, the off-state drain current variability is important for stand-by power considerations.

The variability of MOSFET parameters is due to geometry fluctuations, the granularity of materials and doping randomness [6]. Doping randomness affects MOSFET variability through random dopant fluctuations (RDF) in the channel, the source and drain extensions and in the ground plane. Fabrication imperfections cause the variability of device dimensions, such as line edge roughness (LER), as well as Si channel and buried oxide (BOX) thicknesses. The granularity of gate material also contributes to the parameter variability of a device. Typically, the channel of an FD SOI device (including UTBB) is left undoped, thus eradicating RDF in the channel. In general, well-controlled process, small, short channel effects [3] and low series resistance [7] contribute to the low variability of FD SOI [1,2,5,7].

The aim of the study is to perform a qualitative analysis of global subthreshold parameter variability. Such an analysis can be carried out even on devices that are not yet fully optimized from the short channel effects perspective. The parameters of interest for the subthreshold regime are the off-state drain current ($I_{d\text{-}off}$) and gate current ($I_{g\text{-}off}$), threshold voltage (V_{th}), subthreshold slope (S) and drain-induced barrier lowering (DIBL). The off-state currents were extracted at gate voltage V_g = 0 V. Absolute values of the correlation coefficients are presented in this work. This paper is an extended version of our previous work [8]. It also incorporates some results from [9]. The data from [9] were improved by doubling the number of characterized devices, thus enhancing statistics.

2. Experimental Details

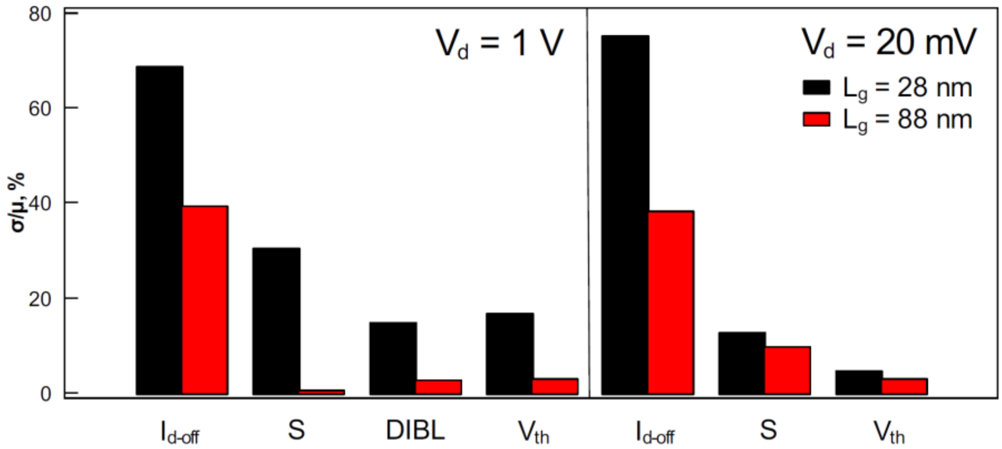
The devices studied in this work are fully-depleted (FD) silicon-on-insulator (SOI) n-channel MOSFETs fabricated on 25 nm-thick BOX. The top Si layer is 7.5 nm-thick. The channel is left undoped allowing the avoidance of RDF. The n-type ground plane was incorporated below BOX. The equivalent oxide thickness of the gate dielectric is 1.2 nm. Devices with gate lengths L_g from 28 to 88 nm and a gate width W_g of 10 μm are characterized. 106 transistors of each gate length are measured across the wafer. A 3-sigma normality test was carried out to exclude outliers.

Two threshold voltage extraction techniques are used in this work: using the constant current method, V_{th} is obtained as V_g, where $I_d/(W_g/L_g)) = 10^{-7}$ A; the transconductance over drain current (g_m/I_d) method is described in [10–12]. Both extraction methods are widely used in the linear and saturation regimes of operation.

3. Results and Discussion

Figure 1 shows the ratios of standard deviations (σ) to mean values (μ) of $I_{d\text{-}off}$, S, DIBL and V_{th} extracted using the g_m/I_d technique at drain voltages V_d of 1 V and 20 mV. As expected, shorter devices exhibit stronger variation in both regimes of operation. It can be seen that $I_{d\text{-}off}$ variability is rather strong and presumably impacted by the variability of other parameters (e.g., V_{th}, S and DIBL).

Figure 1. The ratio of standard deviation over the mean value of the off-state drain current ($I_{d\text{-}off}$), subthreshold slope (S), drain-induced barrier lowering (DIBL) and threshold voltage (V_{th}) extracted using the g_m/I_d method in devices with gate lengths of 28 and 88 nm.



3.1. Off-State Gate Current

Figure 2 shows $\sigma I_{d\text{-}off}$ in devices with gate lengths from 28 nm to 88 nm in linear and saturation regimes. The higher variability of $I_{d\text{-}off}$ is observed in shorter devices. Different parameters, such as short channel effects, I_g and V_{th}, have an impact on I_d in the off-state.

First, $I_{g\text{-}off}$ is considered. The standard deviation of $I_{g\text{-}off}$ is shown in Figure 2. An increase of $\sigma I_{g\text{-}off}$ with V_d can be related to the amplified generation current, which is a function of V_d [13]. There is no pronounced dependence of $I_{g\text{-}off}$ variability on the gate length. Furthermore, $\sigma I_{g\text{-}off}$ remains small compared with $\sigma I_{d\text{-}off}$, except for the longest devices at V_d of 1 V. Absolute values of $I_{g\text{-}off}$ are also negligibly small compared with $I_{d\text{-}off}$ (except for devices with a gate length of 88 nm at V_d of 1 V). Therefore, the effect of $I_{g\text{-}off}$ variability on $I_{d\text{-}off}$ is expected to be negligible. In order to confirm this, Figure 3 plots coefficients of correlation between $I_{g\text{-}off}$ and $I_{d\text{-}off}$ for devices with various gate lengths at V_d of 1 V and 20 mV and at temperatures of 25 and 125 °C. Only in the case of V_d of 1 V and a temperature of 25 °C does the correlation become stronger with a gate length increase as the $I_{g\text{-}off}$ component of $I_{d\text{-}off}$ increases. $I_{g\text{-}off}$ is small at low V_d, as the gate-induced drain leakage (GIDL) is alleviated. This is confirmed by weak $I_{g\text{-}off}$ and $I_{d\text{-}off}$ correlation at V_d of 20 mV for all gate lengths. With a temperature rise, due to V_{th} shift and S degradation, I_d increases stronger than I_g. Thus, the effect of I_g on I_d decreases, and the correlation between $I_{d\text{-}off}$ and $I_{g\text{-}off}$ reduces (Figure 3). The above discussion suggests that the effect of $I_{g\text{-}off}$ variability on $I_{d\text{-}off}$ variability should be accounted for only in relatively long devices at high V_d and room temperature, whereas in other cases, it can be neglected.

Figure 2. $\sigma I_{d\text{-}off}$ and $\sigma I_{g\text{-}off}$ variations with gate length at drain voltages (V_d) of 20 mV and 1 V.

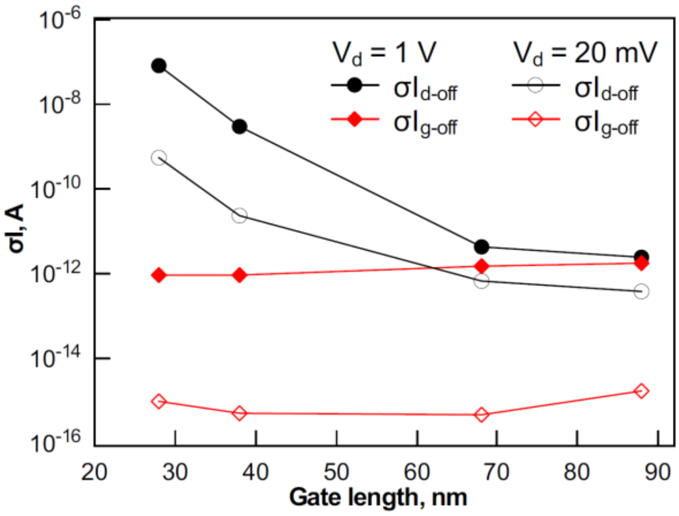
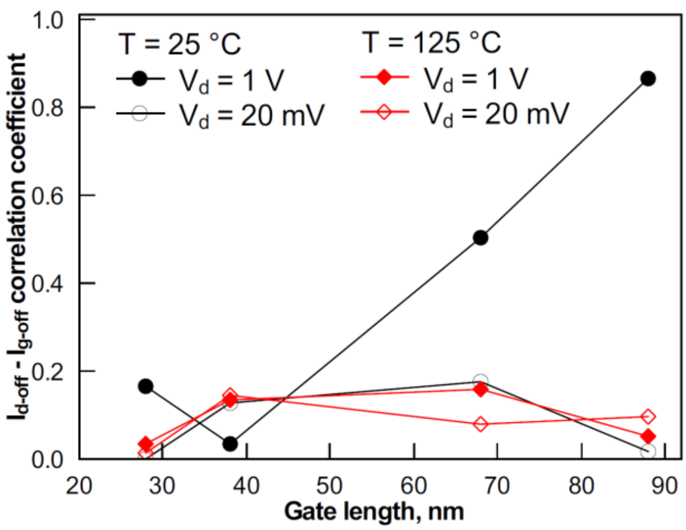


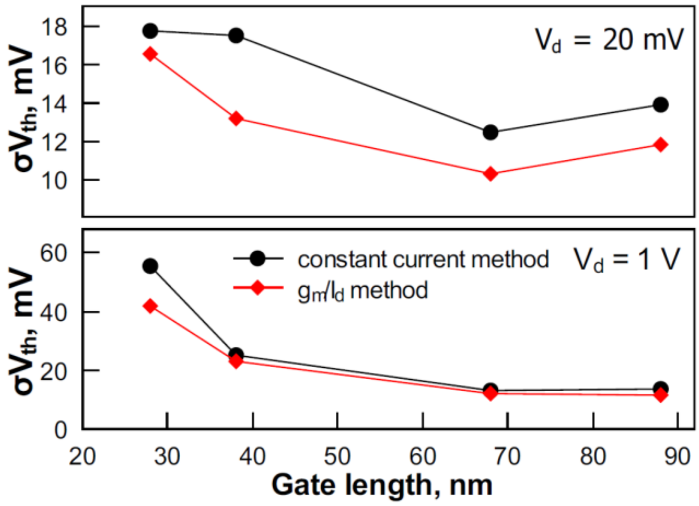
Figure 3. The $I_{d\text{-}off}$-$I_{g\text{-}off}$ correlation in devices with various gate lengths at V_d of 20 mV and 1 V and temperatures of 25 °C and 125 °C.



3.2. Threshold Voltage

Secondly, the effect of V_{th} variability on $\sigma I_{d\text{-}off}$ is considered. Figure 4 shows σV_{th} for devices with gate lengths from 28 to 88 nm at V_d of 20 mV and 1 V. The variability in shorter devices is obviously stronger than in long devices. At V_d of 1 V, σV_{th} is larger than at V_d of 20 mV in short devices. However, in long devices, values of σV_{th} are similar in both regimes of operation. At V_d of 1 V in the shortest devices, σV_{th} is considerably different for two V_{th} extraction methods. The g_m/I_d method results in a lower V_{th} variability than the constant current method. This is due to V_{th} extraction from different parts of current-voltage characteristics and the smaller sensitivity of the g_m/I_d method to short channel effects (S, DIBL), as discussed in [9]. This difference vanishes in long devices.

Figure 4. σV_{th} obtained using the constant current and g_m/I_d methods at V_d of 20 mV (**top**); and V_d of 1 V (**bottom**).



Since in the subthreshold regime, I_d exponentially depends on V_{th}, it is generally assumed that σI_d in this region is dominated by σV_{th}. This holds true for the relatively long devices studied in this work. Correlation between $I_{d\text{-}off}$ and V_{th} at V_d of 1 V is plotted in Figure 5 for 28 nm- and 100 nm-long devices. V_{th} was extracted using the constant current and g_m/I_d methods. To quantify the correlation, Figure 6 plots the coefficients of correlation between I_d and V_{th} (extracted using the constant current method) as a function of V_g in devices with various gate lengths. In the subthreshold region, correlation is strong for 68 and 88 nm-long devices. In strong inversion, the correlation reduces due to the dominance of mobility and series resistance variability [13]. However, in shorter devices, the I_d and V_{th} correlation significantly decreases, not only in strong inversion, but also in the subthreshold regime. This effect is also seen in Figure 7, where variation of the $I_{d\text{-}off}$ and V_{th} correlation coefficients with the gate length is plotted. Therefore, the variability of other parameters apart from $I_{g\text{-}off}$ and V_{th} has to be taken into account.

Figure 5. The variation of $I_{d\text{-}off}$ at V_d = 1.0 V with V_{th} extracted using the constant current and g_m/I_d methods at V_d = 1 V in devices with gate lengths of 28 nm and 88 nm.

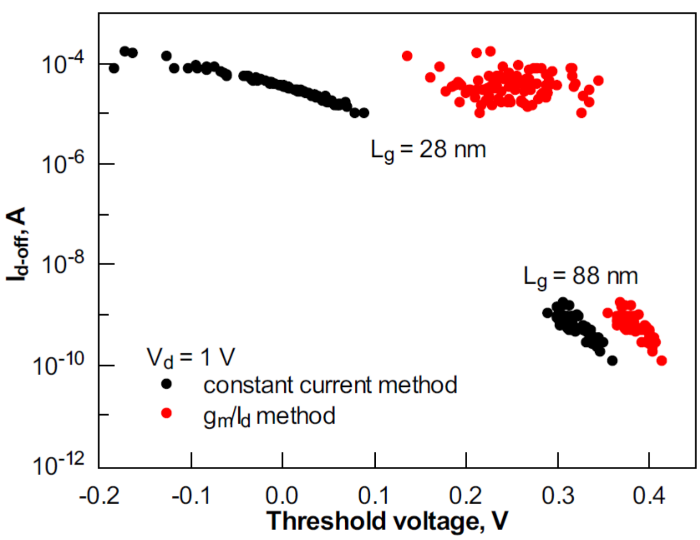
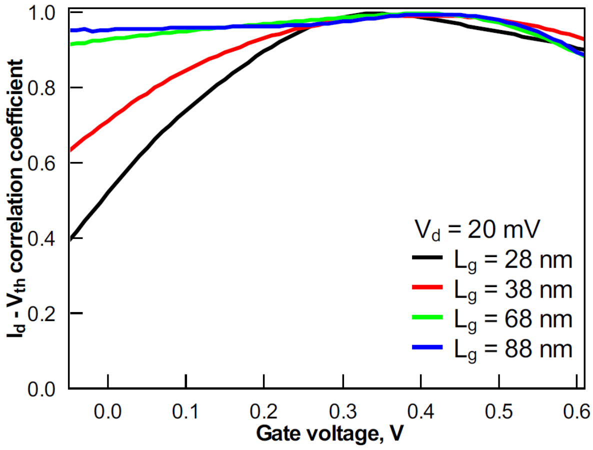
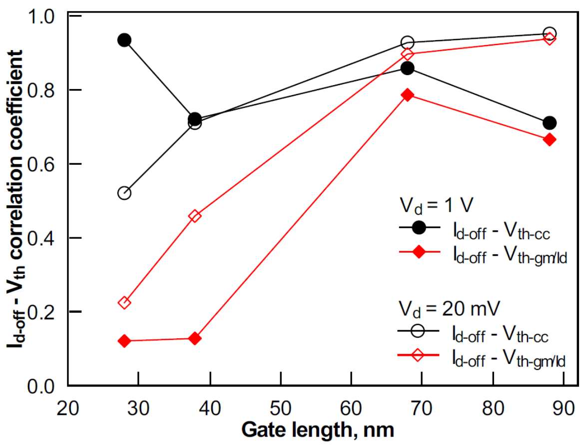


Figure 6. The variation of the I_d-V_{th} correlation coefficient with V_g in devices with various gate lengths. V_{th} was obtained using the constant current method.



It is important to note the importance of the V_{th} extraction method in variability studies. In [9], it was shown that the g_m/I_d V_{th} extraction method is beneficial over other techniques from the short channel effects perspective. A similar property can be observed in Figure 7. The low correlation of $V_{th\text{-}gm/Id}$ and $I_{d\text{-}off}$ in short devices suggests the parasitic effect immunity of V_{th} extraction using the g_m/I_d technique [11,12] compared with the constant current method, as the latter is obviously sensitive to DIBL [9].

Figure 7. The V_{th}-$I_{d\text{-}off}$ correlation coefficients in devices with various gate lengths. V_{th} was obtained using the constant current (cc) and g_m/I_d methods.



3.3. Short Channel Effects

Thirdly, an impact of short channel effect variability on subthreshold I_d is considered. The data in Figure 8 show strong correlation between $I_{d\text{-}off}$ and DIBL in shorter devices. The correlation coefficient decreases to ~0.2 and even more for devices with gate lengths of 68 nm and 88 nm, where the average DIBL is below 60 mV/V. Correlation between $I_{d\text{-}off}$ and V_{th} (extracted at V_d of 20 mV) featured an opposite trend increasing with the gate length, as seen from Figure 7. Therefore, in devices with gate lengths of 68 and 88 nm, $I_{d\text{-}off}$ and V_{th} variability is caused by the same mechanisms, while the variability of DIBL and subthreshold slope dominates in short devices.

Figure 8. The DIBL-$I_{d\text{-}off}$ correlation coefficients in devices with various gate lengths.

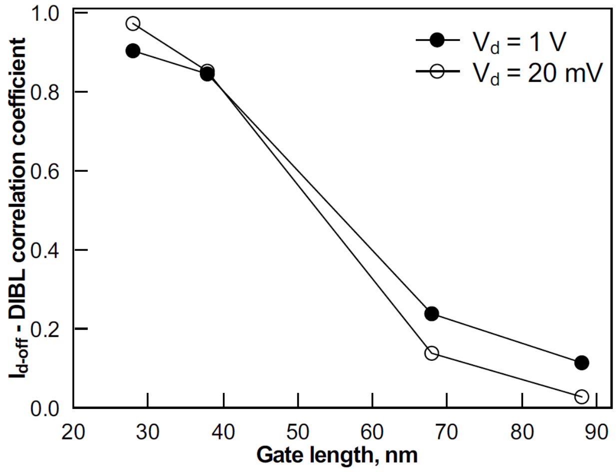


Figure 9 presents the variation of the subthreshold slope and V_{th} extracted using the constant current and the g_m/I_d methods, at high V_d in saturation. Scatter is much stronger in short devices than in longer ones, as expected. Furthermore, in short devices, the correlation of the subthreshold slope with $V_{th\text{-}cc}$ is stronger than the correlation with $V_{th\text{-}gm/Id}$. This correlation is quantified in Figure 10. Figure 10 shows DIBL and V_{th}, as well as the S and V_{th} correlation in 28 nm- and 88 nm-long devices at 25 °C and 125 °C. V_{th} was extracted with the g_m/I_d and constant current methods. V_{th} extracted using the g_m/I_d technique shows little dependence on short channel effects, even at high temperatures. V_{th} obtained with the constant current method shows very strong correlation with DIBL at room and elevated temperatures. This comparison confirms that the g_m/I_d technique enables an evaluation of intrinsic V_{th}, only slightly affected by short channel effects. Evaluation of V_{th} free of short channel effects is of interest for device models that incorporate variability. If variability is imposed on each of the correlating parameters in a model, the total performance variability might be overestimated [9]. This can be avoided either by including correlation factors in the models or using independent (zero correlation) parameters.

Figure 9. Variations of V_{th} obtained using the g_m/I_d and constant current methods as a function of the subthreshold slope.

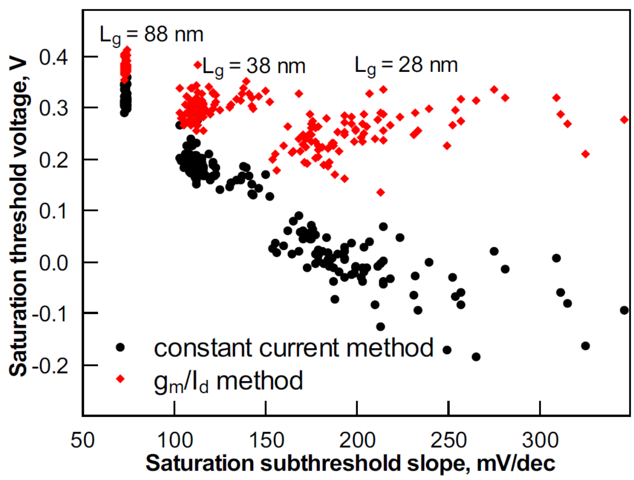
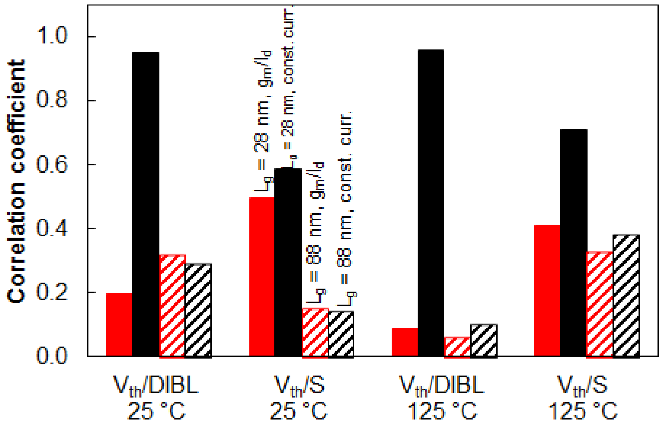
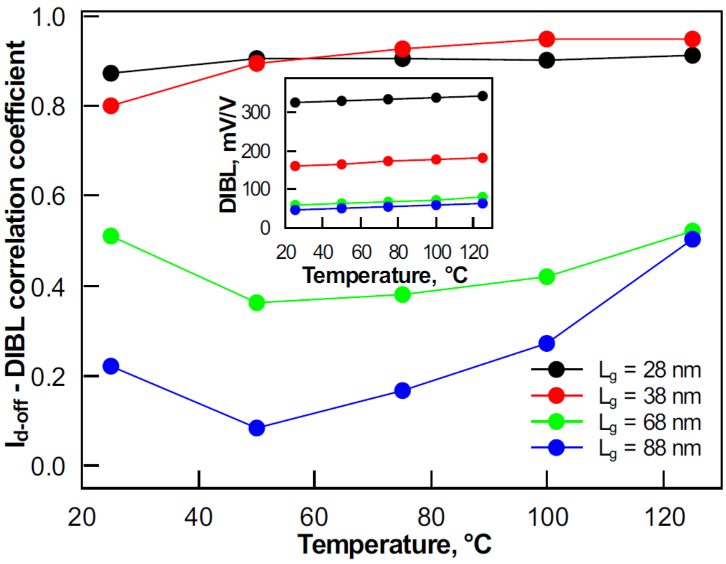


Figure 10. The V_{th}-DIBL and V_{th}-S correlation coefficients in devices with gate lengths of 28 nm and 88 nm at 25 °C and 125 °C temperatures. V_{th} was obtained using the constant current and g_m/I_d methods.



The temperature dependence of the $I_{d\text{-}off}$ and DIBL correlation is shown in Figure 11. In the case of short devices (gate lengths of 28 nm and 38 nm), the correlation factor being very strong shows nearly no dependence on temperature. However, in long devices (gate lengths of 68 nm and 88 nm), the correlation between $I_{d\text{-}off}$ and DIBL rises with temperature. This can be explained by the DIBL increase with temperature, as the inset in Figure 11 shows.

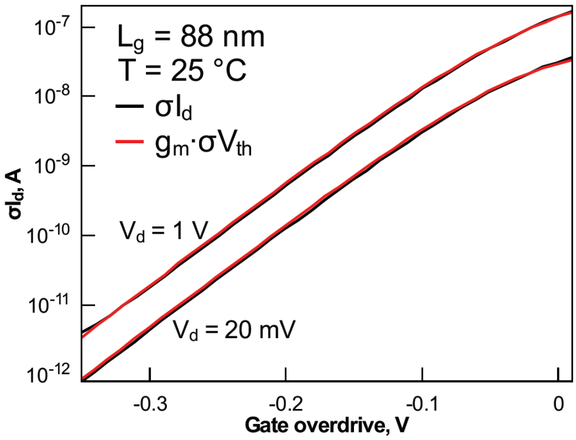
Figure 11. The $I_{d\text{-}off}$–DIBL correlation in devices with various gate lengths in the 25–125 °C temperature range at V_d of 1 V. The inset shows the DIBL temperature dependence.



3.4. Drain Current Variability Modelling

Following the above discussion, Figure 12 compares σI_d and $g_m \cdot \sigma V_{th}$ dependences on V_g in devices with a gate length of 88 nm at V_d of 1 V and 20 mV. σI_d agrees well with $g_m \cdot \sigma V_{th}$ in around-threshold and subthreshold regions, *i.e.*, moderate and weak inversion. In order to ease the comparison of devices with different gate lengths and at various temperatures, the results are plotted as a function of the gate overdrive $V_g–V_{th}$.

Figure 12. Variation of σI_d and its components with gate overdrive at V_d of 20 mV and 1 V at 25 °C in devices with a gate length of 88 nm. V_{th} was extracted using the g_m/I_d method.



The situation is different in short channel devices. As seen from Figure 13, σI_d can be described by $g_m \cdot \sigma V_{th}$ only in a very narrow V_g range around V_{th}. In the subthreshold, the curves strongly deviate. In [14], it was suggested to consider the variability of the body factor in weak inversion in addition to V_{th}. The impact of the body factor dependences on V_g and temperature was emphasized and related to depletion width variation [14]. The UTBB devices studied here remain fully-depleted in the whole weak-to-moderate inversion range at any temperature. Furthermore, Si and oxide thickness fluctuations are not significant, due to the well-controlled fabrication process [2,9]. In [2], reflectometry was used to evaluate top silicon layer thickness variability and correlate it with electrically obtained data. Furthermore, in [9], it was found that global variability does not degrade with temperature through Si layer thickness variation, confirming that the process matches σI_d sufficiently well (Figure 12). As this is not the case in the shortest device (Figure 13), we consider the effective body factor n, which includes short channel effects. Thus, in our case, n dependence on V_g originates from the gate and the drain counteraction on electrostatics. In this work, n (V_g) is derived in the first approximation from S(V_g) according to $S = nkT/q \cdot \ln(10)$, where q is the elementary charge, k is the Boltzmann constant and T is the temperature. At V_d of 20 mV, the combined effect of σV_{th} and σn can fit σI_d sufficiently well:

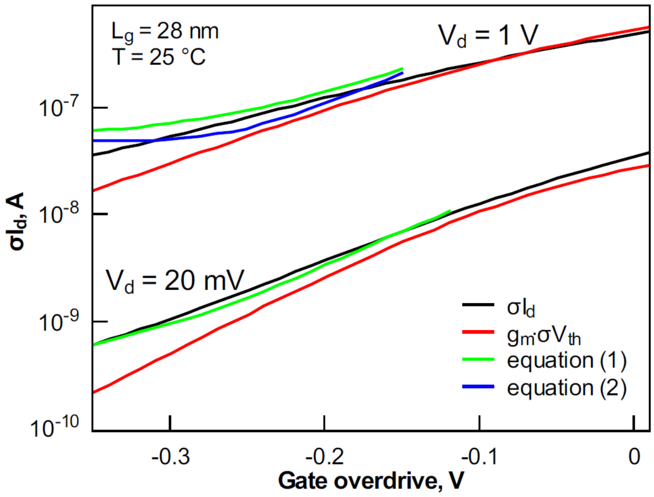
$$\sigma I_d = \sqrt{(g_m \sigma V_{th})^2 + (I_d \sigma n)^2} \quad (1)$$

However at V_d of 1 V, Equation (1) does not allow one to fit σI_d. This is due to amplification of short channel effects at V_d of 1 V and, thus, their stronger impact on V_{th}. In order to fit σI_d, V_{th} and n, correlation coefficient ρ has to be accounted for:

$$\sigma I_d = \sqrt{(g_m \sigma V_{th})^2 + (I_d \sigma n)^2 - 2\rho g_m \sigma V_{th} I_d \sigma n} \quad (2)$$

This approach is shown to work sufficiently well at elevated temperature. In Figure 14, it is shown that σI_d at 125 °C is fitted well when the V_g-dependent effective body factor and its correlation with the V_{th} are considered (Equation (2)).

Figure 13. Variation of σI_d and its components with gate overdrive at V_d of 20 mV and 1 V at 25 °C in devices with a gate length of 28 nm. V_{th} was extracted using the g_m/I_d method.



The results presented in Figure 12, Figure 13 and Figure 14 were obtained using the g_m/I_d V_{th} extraction technique. Figure 15 shows σI_d fitting in 28 nm-long devices at 25 °C with V_{th} obtained using the constant current method. The fitting is acceptable at V_d of 20 mV, as short channel effects are not strongly pronounced. However, at V_d of 1 V, the fitting works only in a very narrow V_g region close to V_{th}. This can be explained by the strong impact of short channel effects on the constant current extraction of V_{th}. This again confirms the advantages of the g_m/I_d V_{th} extraction method for variability assessment.

Further σI_d modelling improvement can be done by accounting for GIDL in the very low V_g region. In strong inversion, mobility and series resistance should be considered [13].

Figure 14. Variation of σI_d and its components with gate overdrive at V_d of 20 mV and 1 V at 125 °C in devices with a gate length of 28 nm. V_{th} was extracted using the g_m/I_d method.

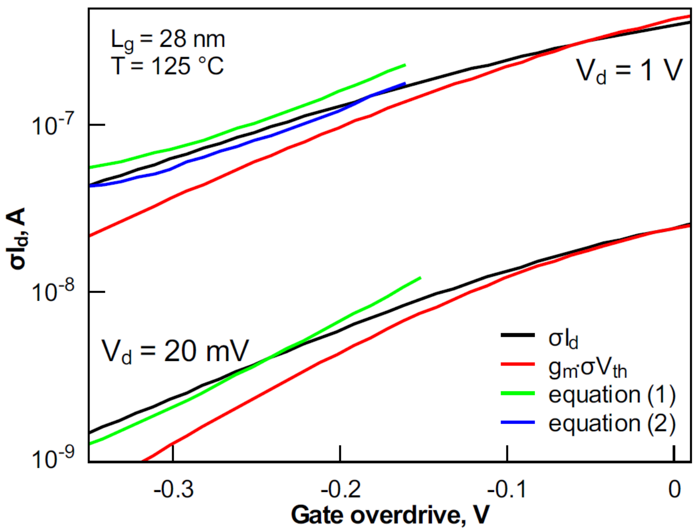
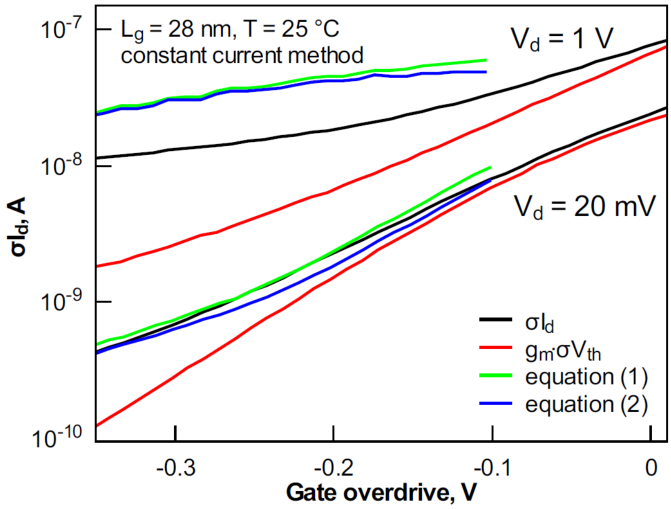


Figure 15. Variation of σI_d and its components with gate overdrive at V_d of 20 mV and 1 V at 25 °C in devices with a gate length of 28 nm. V_{th} was extracted using the constant current method.



4. Conclusions

The global variability of UTBB devices in the subthreshold has been analyzed through $I_{d\text{-}off}$, $I_{g\text{-}off}$, S, V_{th}, DIBL and their correlations. A generally used approach to model σI_d using σV_{th} is shown to work well for long devices. For short channel devices, an improved procedure that accounts for the V_g-dependent effective body factor (incorporating short channel effects) was proposed and validated in the temperature range from 25 °C to 125 °C. This is important for power consumption considerations and compact model parameter extraction in the off-regime. It was shown that the g_m/I_d V_{th} extraction technique is beneficial for accurate variability assessment and modeling.

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Author Contributions

Sergej Makovejev, Jean-Pierre Raskin, Denis Flandre and Valeriya Kilchytska performed in-depth analysis and contributed to paper writing. Babak Kazemi Esfeh performed measurements and the initial results analysis. François Andrieu provided devices for this work.

Conflicts of Interest

The authors declare no conflict of interest.

References

1. Liu, Q.; Yagishita, A.; Loubet, N.; Khakifirooz, A.; Kulkarni, P.; Yamamoto, T.; Cheng, K.; Fujiwara, M.; Cai, J.; Dorman, D.; *et al*. Ultra-Thin-Body and BOX (UTBB) Fully Depleted (FD) device integration for 22 nm node and beyond. *Symp. VLSI Technol.* **2010**, 61–62, doi:10.1109/VLSIT.2010.5556120.
2. Weber, O.; Faynot, O.; Andrieu, F.; Buj-Dufournet, C.; Allain, F.; Scheiblin, P.; Foucher, J.; Daval, N.; Lafond, D.; Tosti, L.; *et al*. High Immunity to Threshold Voltage Variability in Undoped Ultra-Thin FDSOI MOSFETS and Its Physical Understanding. In Proceedings of the International Electron Devices Meeting IEDM, San Francisco, CA, USA, 15–17 December 2008.
3. Sugii, N.; Tsuchiya, R.; Ishigaki, T.; Morita, Y. Local Vth variability and scalability in silicon-on-thin-box (SOTB) CMOS With small random-dopant fluctuation. *IEEE Trans. Electron. Devices* **2010**, *57*, 835–845.
4. Khakifirooz, A.; Cheng, K.; Kulkarni, P.; Cai, J.; Ponoth, S.; Kuss, J.; Haran, B.S.; Kimball, A.; Edge, L.F.; Reznicek, A.; *et al*. Challenges and Opportunities of Extremely Thin SOI (ETSOI) CMOS Technology for Future Low Power and General Purpose System-on-Chip Applications. In Proceedings of the International Symposium on VLSI Technology, Systems and Applications, Hsin Chu, Taiwan, 26–28 April 2010; pp. 110–111.
5. Mazurier, J.; Weber, O.; Andrieu, F.; Toffoli, A.; Rozeau, O.; Poiroux, T.; Allain, F.; Perreau, P.; Fenouillet-Beranger, C.; Thomas, O.; *et al*. On the variability in planar FDSOI technology: From MOSFETs to SRAM cells. *IEEE Trans. Electron. Devices* **2011**, *58*, 2326–2336.
6. Asenov, A.; Cheng, B. Modeling and simulation of statistical variability in nanometer CMOS technologies. In *Analog Circuit Design*; Casier, H., Steyaert, M., van Roermund, A.H.M., Eds.; Springer: Dordrecht, The Netherlands, 2011.
7. Mazurier, J.; Weber, O.; Andrieu, F.; Allain, F.; Tosti, L.; Brévard, L.; Rozeau, O.; Jaud, M.-A.; Perreau, P.; Fenouillet-Beranger, C.; *et al*. Drain Current Variability and MOSFET Parameters Correlations in Planar FDSOI Technology. In Proceedings of the International Electron Devices Meeting IEDM, San Francisco, CA, USA, 15–17 December 2008; pp. 575–578.
8. Makovejev, S.; Esfeh, B.K.; Andrieu, F.; Raskin, J.; Flandre, D.; Kilchytska, V. Global Variability of UTBB MOSFET in Subthreshold. In Proceedings of the IEEE SOI-3D-Subthreshold Microelectronics Technology Unified Conference, Monterey, CA, USA, 7 October 2013.
9. Makovejev, S.; Kazemi Esfeh, B.; Raskin, J.-P.; Flandre, D.; Kilchytska, V. Threshold Voltage Extraction Techniques and Temperature Effect in Context of Global Variability in UTBB MOSFETs. In Proceedings of the European Solid-State Device Research Conference ESSDERC, Venice, Italy, 16–20 September 2013.
10. Flandre, D.; Kilchytska, V.; Rudenko, T. gm/Id Method for threshold voltage extraction applicable in advanced MOSFETs with nonlinear behavior above threshold. *IEEE Electron. Device Lett.* **2010**, *31*, 930–932.
11. Rudenko, T.; Kilchytska, V.; Arshad, M.K.; Raskin, J.-P.; Nazarov, A.; Flandre, D. On the MOSFET threshold voltage extraction by transconductance and transconductance-to-current ratio change methods: Part I—Effect of gate-voltage-dependent mobility. *IEEE Trans. Electron. Devices* **2011**, *58*, 4172–4179.

12. Rudenko, T.; Kilchytska, V.; Arshad, M.K.; Raskin, J.-P.; Nazarov, A.; Flandre, D. On the MOSFET threshold voltage extraction by transconductance and transconductance-to-current ratio change methods: Part II—Effect of drain voltage. *IEEE Trans. Electron. Devices* **2011**, *58*, 4180–4188.
13. Croon, J.A.; Rosmeulen, M.; Decoutere, S.; Sansen, W.; Maes, H.E. An easy-to-use mismatch model for the MOS transistor. *IEEE J. Solid-State Circuits* **2002**, *37*, 1056–1064.
14. Vancaillie, L.; Silveira, F.; Linares-Barranco, B.; Serrano-Gotarredona, T.; Flandre, D. MOSFET Mismatch in Weak/Moderate Inversion: Model Needs and Implications for Analog Design. In Proceedings of the European Solid-State Circuits Conference ESSCIRC, Estoril, Portugal, 16–18 September 2003.