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Three-Way Wideband Power Divider in X-Band Frequency

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Abstract

This article presents the design and analysis of a three-way wideband Wilkinson power divider using a lump-type transmission line circuit instead of quarter-wave transmission lines, and a two-section cascaded lumped transmission line circuit technique instead of a single-section lumped transmission line to improve bandwidth efficiency. The proposed circuit is analyzed using even-mode and odd-mode techniques to find the synthesized parameters. Due to the design challenges in X-band applications, parasitic capacitors play a crucial role in layout design. This work presents a parasitic extraction method using the Y-parameter to analyze the layout of each input/output port. The layout is designed to be compact at $(0.03\lambda_0 \times 0.03\lambda_0)$ on 0.12 um GaN on SiC Technology. The resulting measurement yields a −10 dB fractional bandwidth of 80.39%, while the amplitude and phase balance are 0.1 dB and 5.8° (−13 dB fractional bandwidth of 52.4%, while the amplitude and phase balance are 0.04 dB and 4.9°). Overall, the circuit is compact and provides good performance for X-band frequency applications.

Keywords: Wilkinson power divider; two-section lumped transmission line; wideband; X-band applications

1. Introduction

Power dividers are used in parts of many RF circuits, such as power amplifiers and low-noise amplifiers. In current applications, many RF blocks are implemented on-chip. Therefore, the use of on-chip power dividers is more convenient.

In this work, a power divider for the X-band frequency range supporting wideband applications was designed. Although there have been many research reports on 2-way Wilkinson power dividers, L. Wang et al. found that using a cascaded 2-way Wilkinson power divider resulted in power loss, increased reflection, and increased space requirements [1]. Therefore, S. Cheng and M. Pavlick presented an N-way Wilkinson power divider, which allows for the study of Wilkinson power dividers with a larger number of output ports [2]. However, since Wilkinson power dividers generally have a relatively large circuit area, several research papers have focused on reducing the size of the transmission line of the Wilkinson power divider by using the lumped transmission line technique, which uses inductor, capacitor, and resistor devices connected in various networks [3–5]. However, using lumped transmission lines instead of quarter-wave transmission lines still does not provide sufficient bandwidth efficiency, leading to the use of multi-section lumped transmission lines to expand bandwidth [6–9]. Despite extensive research on power dividers, the demand for three-way power dividers continues to grow. Currently, research on on-chip three-way power dividers is relatively limited.

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Although several on-chip Wilkinson power dividers (WPDs) have been reported, most architectures focus on 2-way splits [3,7,8] or 4-way splits [9,10]. Cascading standard 2-way dividers to feed odd-numbered array channels leads to asymmetric layouts, larger chip areas, and additional insertion losses. On the other hand, existing 3-way dividers, such as [11], rely on a single-section lumped $\lambda/4$ replacement using LTCC technology, which offers limited operating bandwidth and suffers from performance degradation due to parasitic losses when translated to semiconductor substrates.

In this work, we propose a novel compact 3-way power divider monolithically integrated on a GaN process. To overcome the bandwidth limitations of traditional single-section designs [11] and mitigate GaN substrate losses, a two-stage cascaded lumped-element network is implemented. This topology achieves a significantly broader bandwidth while maintaining a compact chip footprint suitable for on-chip integration.

The three-way power divider can be used for applications such as distributing power for an odd number of elements in an antenna array. By using an even number of 1:N power divider with a single 3-way power divider, an odd-way power divider can be formed. Figure 1 shows the system. This paper is aimed at developing a 3-way power divider for the wide X-band.

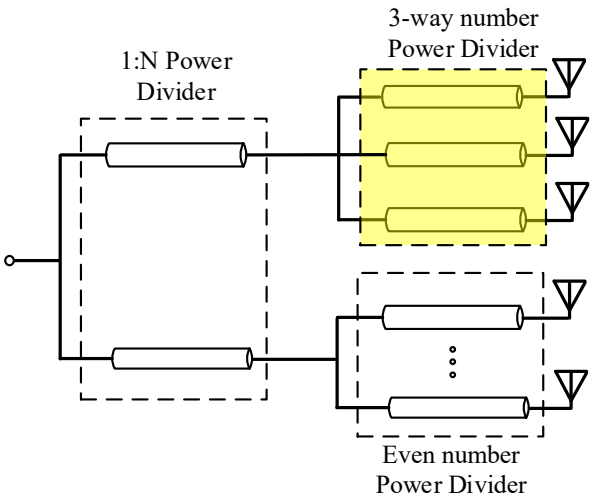


Figure 1. An odd-number power divider system.

2. Lumped Transmission Line Circuit

2.1. Design with Lumped Transmission Line

Research designs to increase the bandwidth of Wilkinson Power Divider (WPD) circuits typically rely on quarter-wave transmission lines. However, the relatively large physical size of distributed transmission lines makes them less suitable for integrated circuits (ICs). Therefore, lumped-element transmission lines have been investigated as an alternative for implementing compact on-chip WPDs [12–14]. In these approaches, conventional transmission lines are replaced by equivalent lumped-element networks, such as π-type structures consisting of series inductors and shunt capacitors [13]. Lumped-element transmission lines have also been employed to achieve wideband WPDs in CMOS technology [14]. The lumped transmission line structure used in this work is constructed from series inductors and shunt capacitors, as shown in Figure 2.

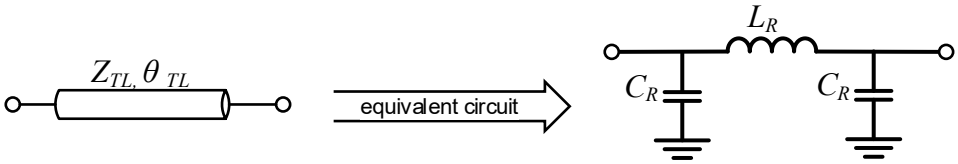


Figure 2. A distributed transmission line is represented by an equivalent lumped-element circuit, where a lumped π-network is employed to model the electrical behavior of the distributed transmission line.

This right-handed lumped transmission line structure can mimic the behavior of a distributed transmission line; however, its continuously varying impedance with frequency results in a relatively narrow bandwidth. The values of the lumped transmission-line components can be calculated using the equations reported in [15]. To improve bandwidth and provide greater design flexibility, two-section Wilkinson power dividers have been investigated [8], while lumped-element and π-type structures have been employed to replace conventional quarter-wavelength transmission lines for circuit miniaturization and wideband operation [16]. Furthermore, multi-section lumped-element structures using cascaded LC π-networks have been demonstrated to approximate a quarter-wavelength transmission line and achieve wideband operation [17,18]. In this work, the transmission line is divided into cascaded sections with shorter electrical lengths to form an equivalent distributed transmission line, as shown in Figure 3.

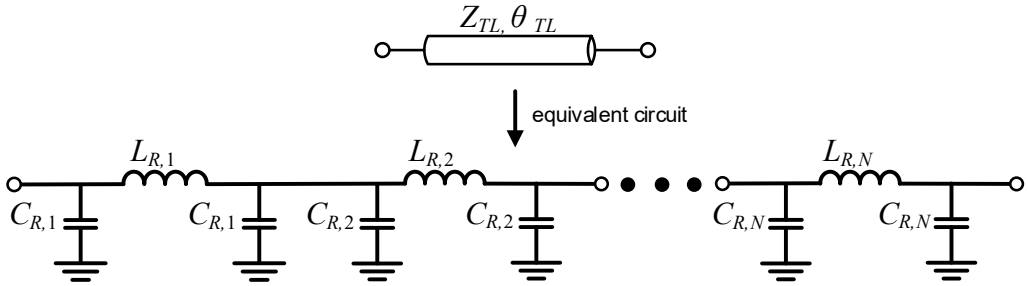


Figure 3. Equivalent cascaded lumped-element circuit representation of a distributed transmission line.

2.2. Loss Study of Lumped Transmission Line Circuit

A cascaded lumped transmission line circuit can be used to maintain characteristic impedance over a range of frequencies. This section investigates the impedance and phase deviations from those of an ideal distributed transmission line. In this work, identical transmission line sections are cascaded to form the overall lumped transmission line. The ABCD matrix approach can be used to characterize the electrical behavior of each lumped transmission line section and the cascaded structure [18]. Accordingly, the ABCD matrix of the cascaded transmission line can be obtained from the ABCD matrix of a single lumped transmission-line section, $[ABCD]_{single}$, as follows:

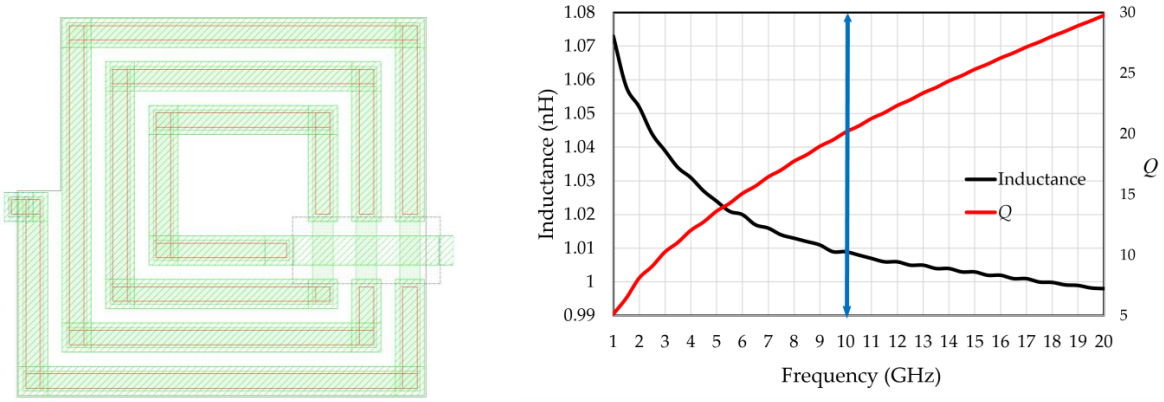
$$\begin{bmatrix} A & B \\ C & D \end{bmatrix} = \begin{bmatrix} A_{single} & B_{single} \\ C_{snigle} & D_{single} \end{bmatrix}^N = \begin{bmatrix} \cosh\left(\theta_{TL,single}\right) & Z_{TL,single}\sinh\left(\theta_{TL,single}\right) \\ \frac{\sinh\left(\theta_{TL,single}\right)}{Z_{TL,single}} & \cosh\left(\theta_{TL,single}\right) \end{bmatrix}^N \quad (1)$$

where $\theta_{TL,single}$, $Z_{TL,single}$, $[ABCD]_{single}$ are the electrical length, the characteristic impedance and the ABCD matrix of each transmission line section and $[ABCD]$ is the ABCD matrix of the cascaded line. The characteristic impedance of the cascaded line can be found from the total ABCD matrix as follows:

$$\theta_{TL} = \cosh^{-1}(A) \quad (2)$$

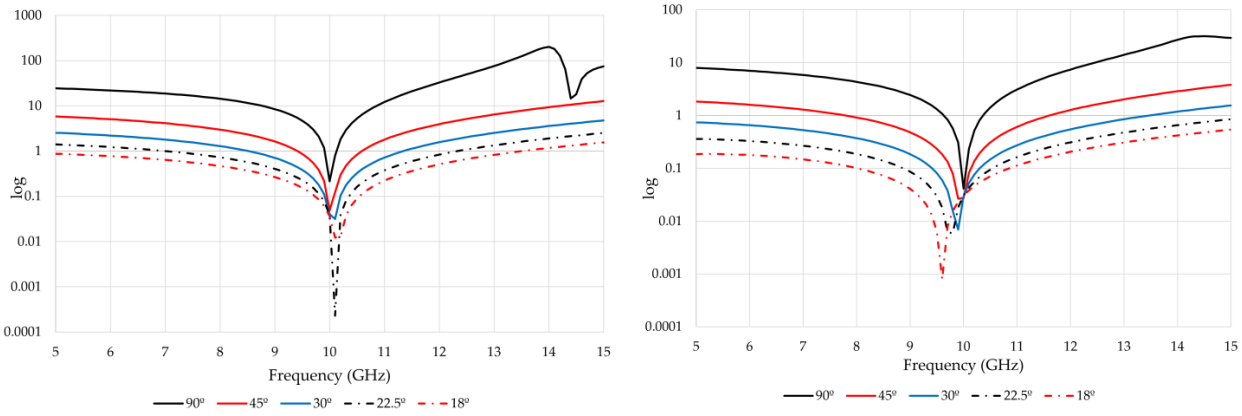
$$Z_{TL} = \frac{B}{\sinh(\theta_{TL})} \tag{3}$$

Since lumped element devices in the form of a π-network are lossy in general, their quality factor (Q) must be considered in the design, especially the quality factor of the inductors. The Q-factor of an integrated inductor depends on its layout, conductor and substrate losses, and fabrication process [19,20]. In this work, the chip was implemented on the GaN process. Therefore, the Q-factor was evaluated based on the implemented inductor rather than assuming a general Q-factor range. To evaluate the quality factor (Q) of the inductor, a 1 nH spiral inductor is utilized in the dividercircuit. Figure 4 illustrates its physical layout, inductance, and Q-factor curve. As observed from the figure, the inductor achieves a Q-factor of 19.45 at 10 GHz. Therefore, in the following simulation study, the inductor is set to have a Q value of 20. Multi-section transmission lines using lossy inductors are formed to have an overall electrical length of 90° and a characteristic impedance of $\sqrt{3}Z_0$ at 10 GHz. The lines in the simulation are of different subsections, e.g., electrical lengths of 90°, 45°, 30°, 22.5°, and 18°. Their behaviors are compared with those of a theoretical 90° transmission line over 5–15 GHz. The percentage errors in the characteristic impedance and the electrical length are shown in Figure 5. Note that Z_0 denotes the port impedance, which is 50 Ω in this work.



(**a**) (**b**)

Figure 4. Simulation study of a 1 nH inductor. (**a**) layout of the inductor (**b**) inductance and Q-factor curves.



(**a**) (**b**)

Figure 5. Theoretical simulation results of comparison of the percentage error of (**a**) characteristic impedance (Z_{TL}) and (**b**) electrical length (θ) for cascaded lumped transmission line circuits with sub-section.

3. Even and Odd Mode Analysis of WPD Circuits

3.1. Conventional Lumped Circuit Transmission Line WPD

The WPD shown in Figure 6 exhibits a symmetric configuration, which allows the circuit to be divided into three identical parts for even- and odd-mode analysis [21,22]. In the even mode, the plane of symmetry is open when the signals at Ports 2, 3, and 4 have the same magnitude and phase. Therefore, no current flows through the common point containing the resistor R, and the corresponding equivalent circuit is shown in Figure 7a. In the odd mode, Port 1 is short-circuited, while the common point between the output ports also becomes a short circuit. The corresponding equivalent circuit is shown in Figure 7b.

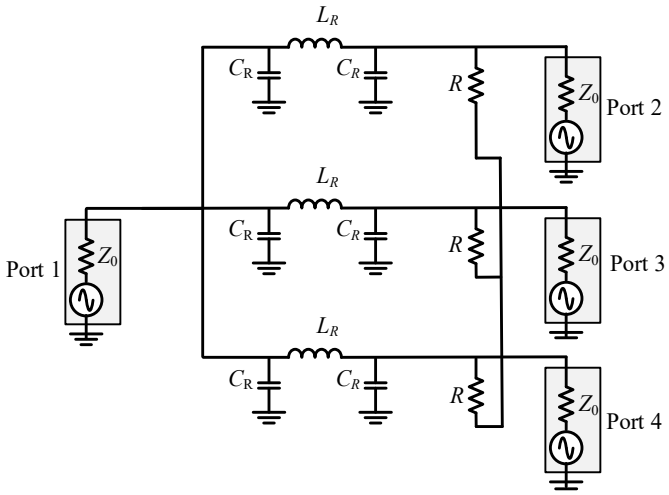


Figure 6. Conventional one-Section 3-way Wilkinson power divider.

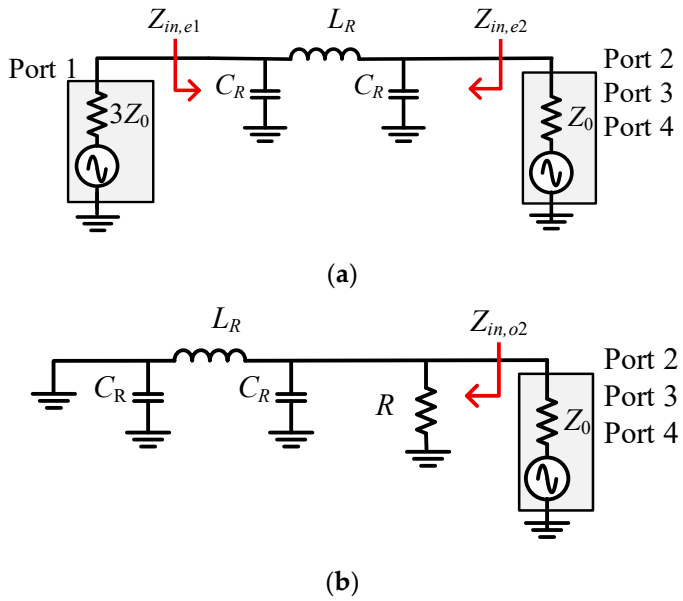


Figure 7. Circuit analysis of the one-section power divider in (**a**) even mode and (**b**) odd mode. The input impedance looking into Port 1 and Port 2 for the even and odd modes are indicated by the red arrow.

In the even mode, the impedance $Z_{in,e1}$ and $Z_{in,e2}$ are calculated as follows.

$$Z_{in,e1} = \frac{Z_0 + j\omega L_R - \omega^2 L_R C_R Z_0}{1 - \omega^2 L_R C_R + j\omega C_R Z_0 (2 - \omega^2 L_R C_R)} \quad (4)$$

$$Z_{in,e2} = \frac{3Z_0 + j\omega L_R - 3\omega^2 L_R C_R Z_0}{1 - \omega^2 L_R C_R + j3\omega C_R Z_0 (2 - \omega^2 L_R C_R)} \quad (5)$$

In the odd-mode analysis, the value of $Z_{in,o2}$ can be found as follows.

$$Z_{in,o2} = \frac{j\omega L_R R}{R(1 - \omega^2 L_R C_R) + j\omega L_R} \quad (6)$$

All ports must be impedance-matched. In this case, the value of $Z_{in,e1}$ must be equal to 150 Ω, $Z_{in,e2}$ and $Z_{in,o2}$ equal to 50 Ω.

3.2. Two-Section Lumped Transmission Line Circuit WPD

The proposed two-section lumped transmission line circuit WPD is shown in Figure 8. The even and odd mode analysis can be applied similarly to the one-section case. Equivalent circuits for even- and odd-mode analysis are shown in Figure 9.

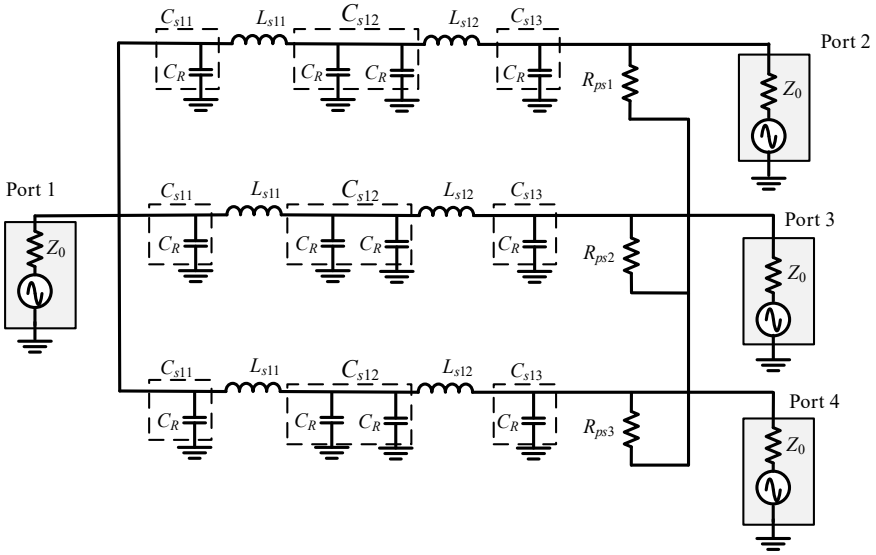


Figure 8. Lossless two-section lumped transmission line in a 3-way Wilkinson power divider.

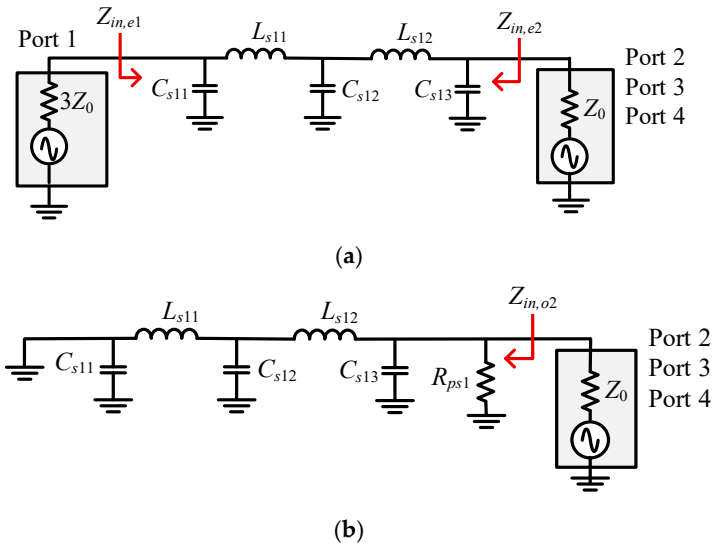


Figure 9. Circuit analysis of the two-section power divider in (**a**) even mode and (**b**) odd mode. The input impedances looking into Ports 1 and 2 for the even and odd modes are indicated by the red arrows.

The input impedance ($Z_{in,e1}$, $Z_{in,e2}$) of the even mode can be calculated using (7)–(9).

$$Z_{in,e1} = \frac{N_1(s)}{D_1(s)} \tag{7}$$

where

$$N_1(s) = Z_0 + s(L_{s11} + L_{s12}) + s^2 Z_0(C_{s12}L_{s11} + C_{s13}L_{s11} + C_{s12}L_{s12}) + s^3 C_{s12}L_{s11}L_{s12} + s^4 C_{s12}C_{s13}L_{s11}L_{s12}Z_0 \tag{8}$$

and

$$D_1(s) = 1 + sZ_0(C_{s11} + C_{s12} + C_{s13}) + s^2[C_{s11}(L_{s11} + L_{s12}) + C_{s12}L_{s12}] + s^3 Z_0[C_{s11}C_{s12}L_{s11} + C_{s11}C_{s13}L_{s11} + C_{s11}C_{s13}L_{s12} + C_{s12}C_{s13}L_{s12}] + s^4 C_{s11}C_{s12}L_{s11}L_{s12} + s^5 C_{s11}C_{s12}C_{s13}L_{s11}L_{s12}Z_0 \tag{9}$$

Also, calculate $Z_{in,e2}$ by (10)–(12).

$$Z_{in,e2} = \frac{N_2(s)}{D_2(s)} \tag{10}$$

where

$$N_2(s) = 3Z_0 + s(L_{s11} + L_{s12}) + 3s^2 Z_0(C_{s12}L_{s11} + C_{s13}L_{s11} + C_{s12}L_{s12}) + s^3 C_{s12}L_{s11}L_{s12} + 3s^4 C_{s12}C_{s13}L_{s11}L_{s12}Z_0 \tag{11}$$

and

$$D_2(s) = 1 + 3sZ_0(C_{s11} + C_{s12} + C_{s13}) + s^2[C_{s11}(L_{s11} + L_{s12}) + C_{s12}L_{s12}] + 3s^3 Z_0[C_{s11}C_{s12}L_{s11} + C_{s11}C_{s13}L_{s11} + C_{s11}C_{s13}L_{s12} + C_{s12}C_{s13}L_{s12}] + s^4 C_{s11}C_{s12}L_{s11}L_{s12} + 3s^5 C_{s11}C_{s12}C_{s13}L_{s11}L_{s12}Z_0 \tag{12}$$

The input impedance ($Z_{in,o2}$) of odd mode can be calculated using (13)–(14).

$$Z_{in,o2} = \frac{s(L_{s11} + L_{s12}) + s^2(C_{s12}L_{s11}L_{12})}{E(s)} \tag{13}$$

where

$$E(s) = R + s(L_{s11} + L_{12}) + Rs^2[C_{s12}L_{s11} + C_{s13}(L_{s11} + L_{12})] + s^3 C_{s12}L_{s11}L_{12} + Rs^4 C_{s12}C_{s13}L_{s11}L_{12} \tag{14}$$

Additionally, all port impedances in Figure 7 must be matched. The values of $Z_{in,e1}$ must be equal to 150 ohms, $Z_{in,e2}$ and $Z_{in,o2}$ equal to 50 ohms. Equations (4)–(14) can be used to calculate the lossless lumped transmission line circuit components. In the next section, loss and parasitic effects from the layout are considered.

4. Simulation and Measurement

The circuit in this work was designed for center frequency of 10 GHz. Simulations are performed using the one-section and two-section lumped transmission line in a Wilkinson power divider. The results of interest are the reflection coefficients, transmission coefficients, and isolation coefficients. Three types of results are compared: schematic simulation, layout simulation, and measurement.

4.1. Schematic Simulation

The lossless WPD using one- and two-section, shown in Figures 6 and 8, was simulated for S-parameters, e.g., reflection coefficients, transmission coefficients, and isolation coefficients. The calculated component values are shown in Table 1.

Table 1. Component values schematic in Figures 6 and 8.

TL	C_1 (pF)	L_1 (nH)	C_2 (pF)	L_2 (nH)	C_3 (pF)	R (Ω)
1 section	0.1837	1.378	0.1837	-	-	50
2 section	0.0761	0.974	0.0761	0.974	0.0761	50

Later, the results are compared with the layout simulation and measurement.

4.2. Layout Simulation

In this section, the layout parasitic extraction is investigated, considering only the TT process corner of the 0.12 um GaN technology. Only a two-section transmission line is used here; however, a one-section can be processed similarly. In this work, electromagnetic (EM) simulations of the layout were performed using the Momentum Microwave solver integrated within Keysight Advanced Design System [23]. The Momentum solver employs a 2.5D Method of Moments (MoM) approach based on multilayer dielectric Green's functions [24]. The circuit layout was fabricated using the 0.12-µm RF GaN-on-SiC Process Design Kit (PDK) from WIN Semiconductors Corp. Bound/interconnection pads and passive device layouts were modeled using the dedicated foundry PDK components and interconnect layout rules. Open-boundary conditions (infinite horizontal substrate layers surrounded by open half-space) were applied. A non-adaptive planar mesh was used with a discretization density of 500 cells per wavelength at the highest simulation frequency. Mesh convergence was verified prior to final analysis. Increasing the mesh density beyond 500 cells per wavelength yielded a change of less than 0.01% in the calculated S-parameters (S_{11} and S_{21}). Because a fixed (non-adaptive) meshing scheme is employed, the numerical results are fully deterministic and repeatable.

For the layout design, parasitic elements cause the circuit components to vary from the schematic ones. The parasitic capacitors vastly affect the layout performance, especially in X-band applications. To extract the parasitic capacitors from the layout, the two-section lumped transmission lines are divided into two circuits. The two circuits have the middle capacitors, C_{s12}, as the common elements. However, in the layout, the physical capacitors are present, along with parasitic capacitors from the layout. Figure 10 shows the parasitic capacitors and the divided circuits. Each single lumped transmission line simulation is studied using Y-parameters, as shown in the figure.

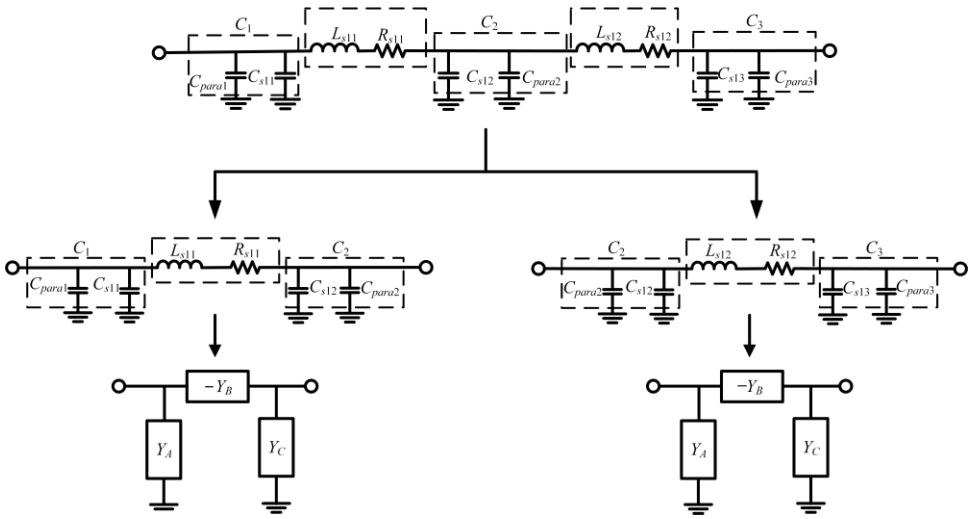


Figure 10. Parasitic extraction using Y-parameter of a two-section transmission line. The arrows indicate the circuit division and Y-parameter extraction process.

The total capacitors, inductors, and resistors can be found from (15)–(17)

$$\mathrm{Im}(Y_A) = \omega C_{1\ or\ 2} \tag{15}$$

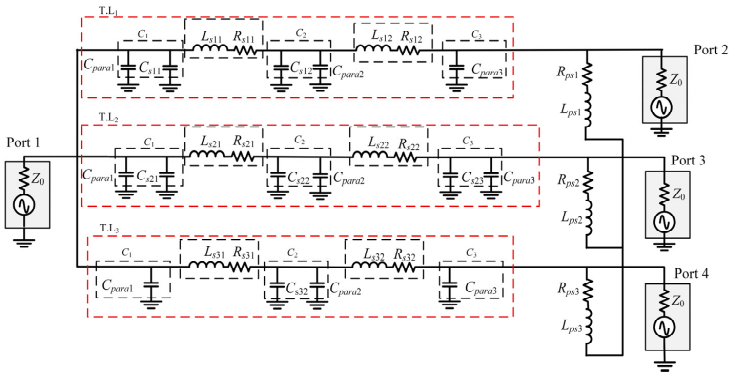
$$\left(-\frac{1}{Y_B}\right) = R_{s11or\,12} + j\omega L_{s11\,or\,s12} \tag{16}$$

$$\mathrm{Im}(Y_C) = \omega C_{2\ or\ 3} \tag{17}$$

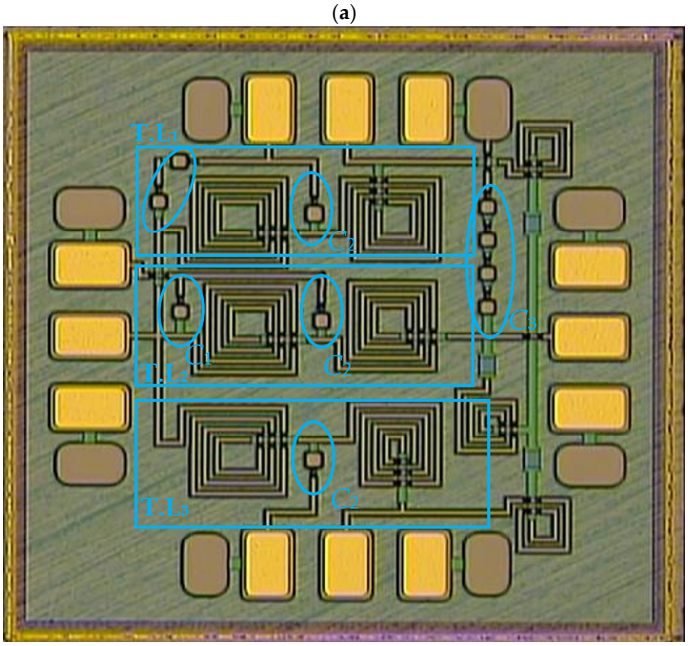
where $C_{1\ or\ 2}$ and $C_{2\ or\ 3}$ are the physical capacitances added to the parasitic capacitance, L_{s11} or L_{s12} are the inductors with losses modeled with resistors R_{s11} or R_{s12}.

The values of L_{sij}, C_{sij} can be found from (7)–(14), allowing us to determine the parasitic capacitor value of the circuit by subtracting them from the total value. The total capacitance value is extracted from (15) and (17). The inductor (including parasitic inductance) and resistor values are found from (16).

The proposed three-way power divider is illustrated in Figure 11, where Figure 11a depicts its equivalent circuit including parasitic capacitances, and Figure 11b shows its layout. The component values obtained from the schematic design cannot be directly applied to the layout because of the parasitic effects introduced by the physical implementation. Therefore, the component values need to be adjusted to account for these parasitic capacitances.



(a)



(b)

Figure 11. Equivalent schematic of three-way power divider layout using two-section lumped transmission circuit. (**a**) Schematic and (**b**) layout.

To optimize the component values, each transmission line section was treated individually. The equivalent circuits extracted from the layout for TL_1, TL_2, and TL_3 are shown in Figures 12–14, respectively. Each transmission line section was further represented by its corresponding even- and odd-mode equivalent circuits for impedance-matching analysis. In the layout design process, the inductors were first placed according to the floorplan, followed by the capacitors. The values of C_1, C_2, and C_3 for each transmission line section

were then optimized to achieve impedance matching for both the even- and odd-mode circuits at their respective ports. Since each transmission line layout has slightly different parasitic characteristics, the optimization was performed separately for each section.

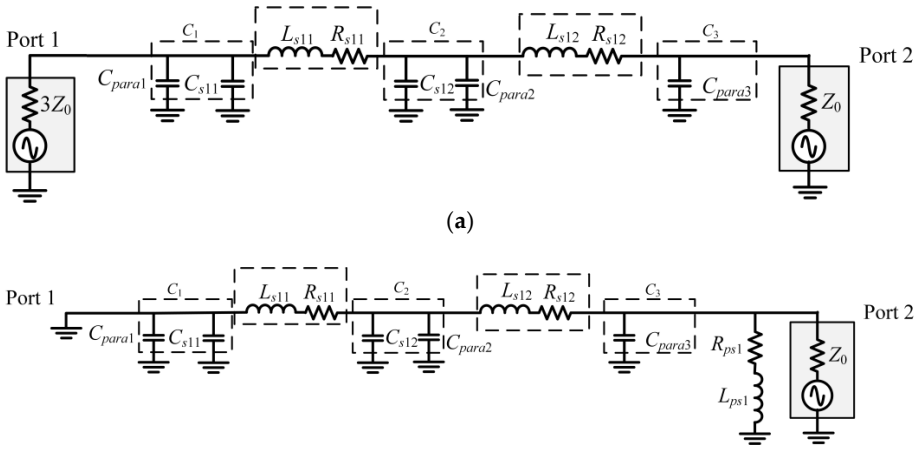


Figure 12. Analysis of port 1 and port 2 (TL_1 in Figure 10) using (**a**) even mode and (**b**) odd mode.

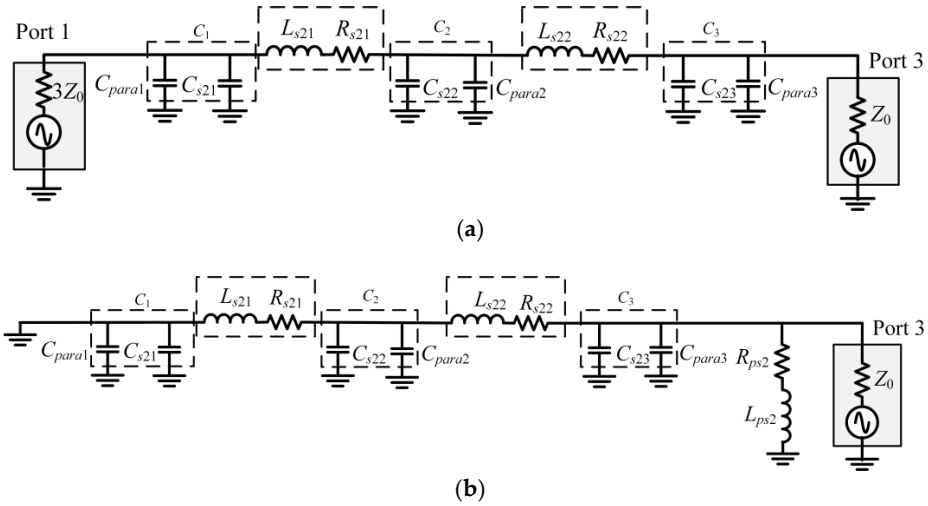


Figure 13. Analysis of port 1 and port 3 (TL_2 in Figure 10) using (**a**) even mode and (**b**) odd mode.

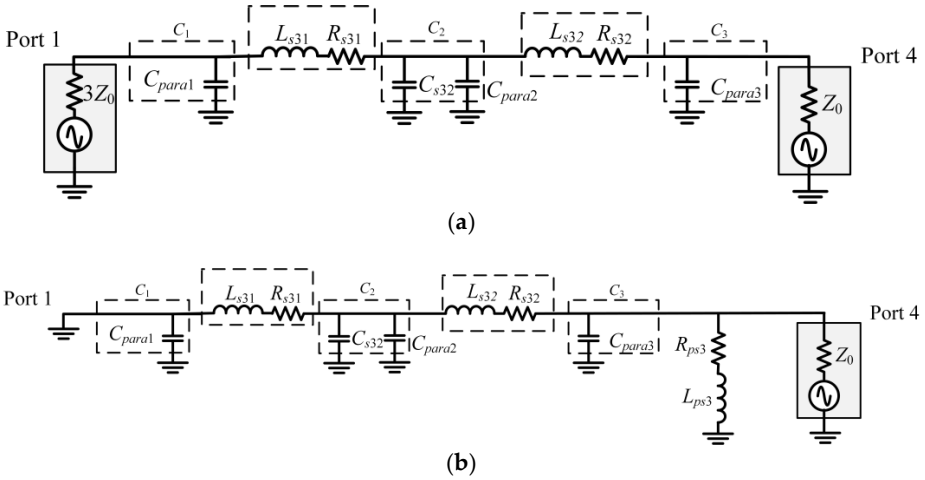


Figure 14. Analysis of port 1 and port 4 (TL_3 in Figure 10) using (**a**) even mode and (**b**) odd mode.

Table 2 shows the physical layout components after the layout optimization at 10 GHz. Note that some of the capacitors are physically omitted since the parasitic capacitance exceeds the required capacitance. Then, the layout circuits are simulated and measured for the reflection coefficients, transmission coefficients, and isolation coefficients, as shown in Figures 15–17. In these figures, the schematic traces represent the ideal lumped-component simulation, the layout traces correspond to the layout EM simulation, and the measurement data represent the measured results. Clearly, the two-section lumped transmission lines WPD yield better reflection coefficients than those of the one-section. Therefore, only the two-section lumped transmission line WPD is used in comparison with the layout and measurement results. The reflection coefficients (S_{11}, S_{22}, S_{33}, and S_{44}) exhibit good agreement among all three results. The maximum reflection coefficient is −10 dB in both the ideal lumped-component simulation and the layout EM simulation, while the measured result is −10.09 dB, indicating an excellent matching performance with only 0.09 dB deviation from the simulated value.

Table 2. Lumped model of TL schematic and layout at 10 GHz.

TL	C_1 (pF)	L_{si1} (nH)	R_{si1} (Ω)	C_2 (pF)	L_{si2} (nH)	R_{si2} (Ω)	C_3 (pF)	Z_{TL}	θ_{TL}
1	0.1203	1.078	4.03	0.1197	0.8728	3.279	0.0556	93.68	89.08
2	0.1315	1.014	3.565	0.1103	1.013	3.783	0.0513	96.30	90.65
3	0.0724	1.096	4.03	0.1143	0.8355	3.383	0.0545	97.05	79.40

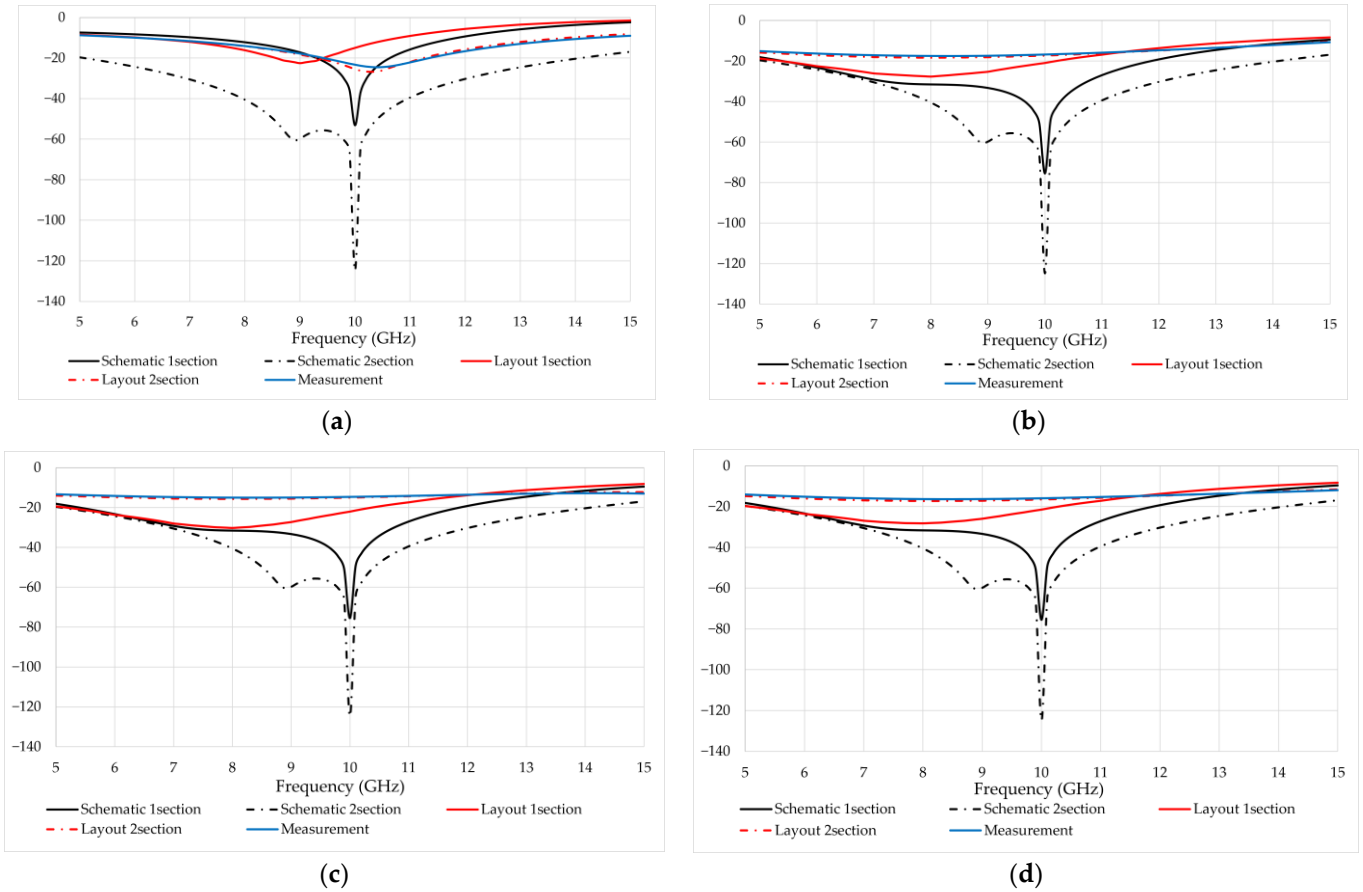


Figure 15. Compare layout simulation of one-section, two-section, and measurement of circuit reflection coefficients for parameters (**a**) $S_{11,}$ (**b**) S_{22}, (**c**) $S_{33,}$ (**d**) S_{44}.

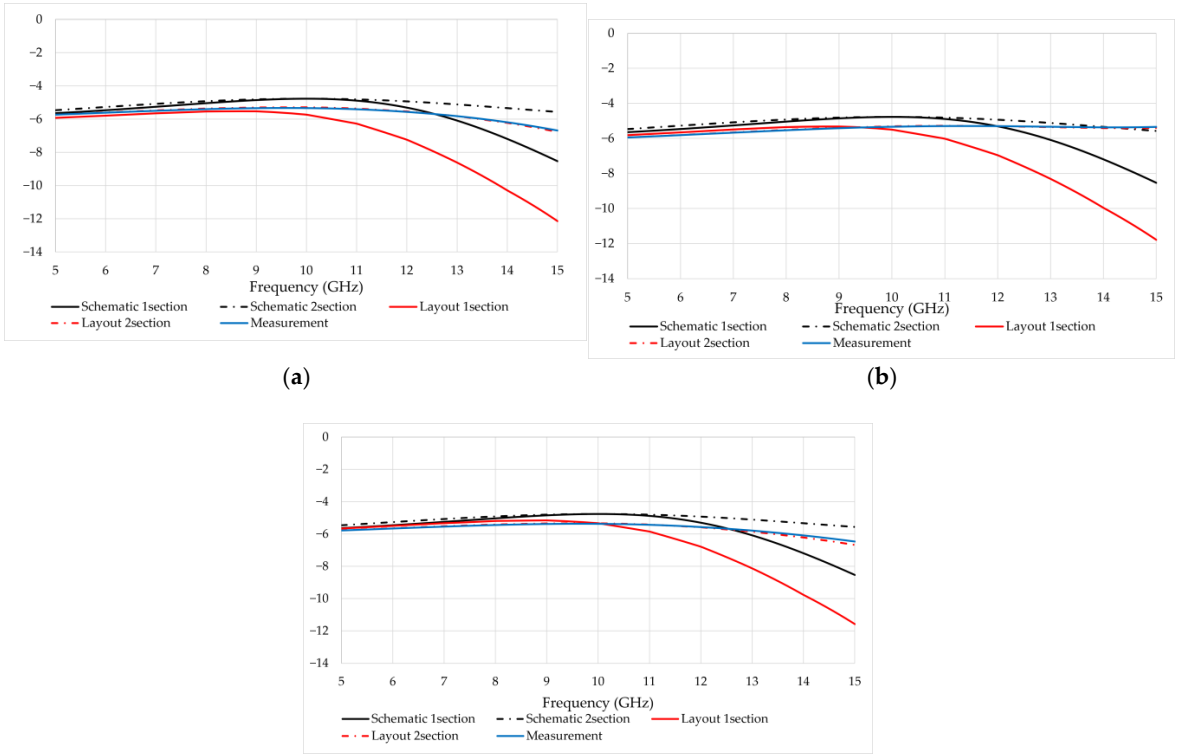


Figure 16. Compare layout simulation of one-section, two-section, and measurement of circuit transmission coefficients for parameters (**a**) S_{12}, (**b**) $S_{13,}$ (**c**) S_{14}.

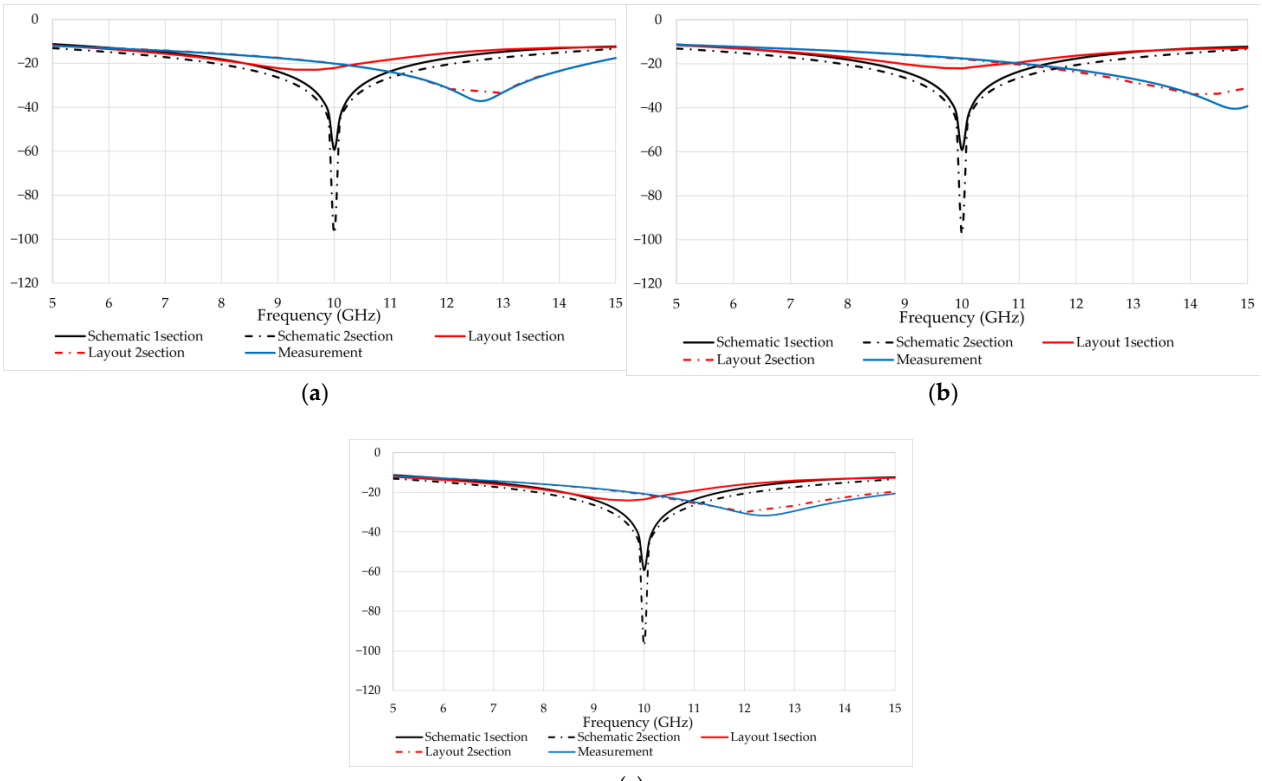


Figure 17. Compare layout simulation of one-section, two-section, and measurement of circuit isolation coefficients for parameters (**a**) S_{23}, (**b**) S_{24}, (**c**) S_{34}.

For the transmission coefficients (S_{12}, S_{13}, and S_{14}), the minimum values are −5.677 dB (ideal lumped-component simulation), −7.632 dB (layout EM simulation), and −6.33 dB (measurement). Compared with the ideal simulation, the measured transmission shows an additional insertion loss of approximately 0.65 dB, whereas it differs from the EM/layout simulation by about 1.30 dB. This indicates that the measured performance lies between the ideal circuit simulation and the EM/layout prediction.

The isolation coefficients (S_{23}, S_{24}, and S_{34}) are −13.9 dB (ideal lumped-component simulation), −15.7 dB (layout EM simulation), and −12.4 dB (measurement). The measured isolation is 1.5 dB higher (worse) than the schematic simulation and 3.3 dB higher than the EM/layout simulation. These discrepancies are mainly attributed to fabrication tolerances, conductor and dielectric losses, connector transitions, and measurement uncertainties, which are not fully captured in the simulations.

Overall, the measured results closely follow the simulated trends, confirming the validity of the proposed design. Although slight degradation in transmission and isolation is observed in the fabricated prototype, the agreement between simulation and measurement demonstrates that the design achieves the intended broadband performance.

For the measured results, a 4-port network analyzer (Keysight N5245B, 10 MHz–50 GHz) was used, with four-port RF GSG probes for contacting the measurement pads. SOLT calibration was performed using three calibration dies. The operating bandwidth of the proposed 3-way power divider is defined based on a −10 dB return loss criterion ($|S_{11}| \leq -10$ dB). As shown in Figure 15, the measured return loss satisfies$|S_{11}| \leq -10$ dB from $f_L = 6.1$ GHz to $f_H = 14.3$ GHz, centered at $f_0 = 10.2$ GHz. This corresponds to a fractional bandwidth (FBW) of 80.39%, calculated via:

$$FBW = \frac{f_H - f_L}{f_0} \times 100\% \tag{18}$$

Across this entire operational frequency band $f_L - f_H$, the worst-case in-band performance parameters are evaluated as follows: Return Loss (S_{11}): $|S_{11}| \leq -10$ dB across $f_L - f_H$; Insertion Loss (S_{21}): The maximum measured insertion loss within the band is 6.3244 dB (including the theoretical 3-way split loss of 4.77 dB); Isolation (S_{23}): The isolation between output ports remains better than 12.401 dB over the entire $f_L - f_H$ window.

Although the measured performance aligns well with the overall predicted trend, slight discrepancies are observed in the insertion loss and input matching (S_{11}). These deviations are primarily attributed to three physical mechanisms. (1) Substrate and ground loss: The finite conductivity of the GaN-on-SiC substrate, along with parasitic inductance/resistance from ground vias, adds unmodeled ohmic loss in the signal path. (2) Unmodeled interconnect parasitics: Micro-scale layout discontinuities, T-junction step capacitances, and via-hole grounding inductances introduce stray parasitics that cause a slight frequency shift and degradation in impedance matching (S_{11}). (3) Measurement setup and probing tolerances: Imperfections in SOLT calibration and probe-to-pad contact resistance during on-wafer GSG probing introduce minor measurement uncertainties that affect both loss and return loss limits.

The chip photograph is shown in Figure 18. Table 3 presents a comparison between the three-way and four-way power dividers. The fractional bandwidth (FBW) is calculated using Equation (11). Because different return-loss criteria are adopted in the reported designs, including −10 dB for [25–28], −12 dB for [29], −12.3 dB for [10], and −13 dB for [30], a −13 dB return-loss criterion is adopted to evaluate the fractional bandwidth (FBW) of the proposed power divider for comparison with the referenced designs.

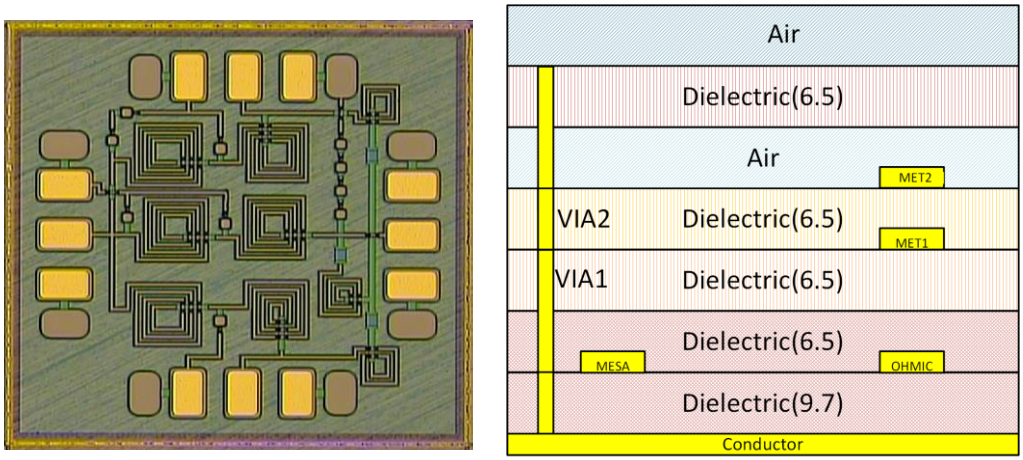


Figure 18. (**a**) Die micrograph and (**b**) schematic cross-sectional view of the metal-layer structure of the proposed lumped-element Wilkinson power divider fabricated using a GaN MMIC process.

Table 3. Comparison Table of Three- and Four-Way Power Dividers.

Refs.	Process	Topology	f_0 (GHz)	IL. (dB)	RL. (dB)	Isolation (dB)	Size ($\lambda_o \times \lambda_o$)	FBW (%)
[10]	GaAs IPD	Bandpass matching	1.95	<1.3	>12.3	>20	0.098 × 0.011	66.7
[25]*	CMOS	N-Coil transformer	4.6	<1.1	>15	>17	0.008 × 0.008	41.87
[26]*	GaAs pHEMT	Coupled line	30	<0.3	>18	>17	0.08 × 0.14	20.69
[27]	Microstrip PCB	Three-Way Planar Power Divider	1	<0.5	>10	<41	0.31 × 0.31	69.4
[28]	IHP SG13S BiCMOS	4–way single-inductor Wilkinson PD	10	<1	>10	>16	0.05 × 0.10	46.67
[29]	45RFE CMOS	Cascaded 4-way WPD Direct 4-way WPD	30	<0.82–1.23 <0.58–1.2	>19 >12	>15 >18	0.021 × 0.033 0.017 × 0.025	40
[30]	Silicon-IPD	2-way Wilkinson PD	94	<1	>13	>15	0.143 × 0.286	37.8
This work	GaN	Cascaded Lumped Pi network	10	<0.8	>13	>13.9	0.03 × 0.03	52.4

[25]* Data obtained from Figure 10, [26]* Data obtained from Figure 5.

As shown in Table 3, under the specified return-loss criterion, the proposed power divider provides a wide fractional bandwidth while maintaining a compact chip size. The comparison is intended to highlight the bandwidth and chip-area characteristics of the proposed design relative to the selected reported works.

5. Conclusions

The design and analysis of a three-way wideband Wilkinson power divider are presented using a two-section cascaded lumped transmission line circuit. By using a smaller electrical-length section, the lumped transmission line circuits expand their characteristic impedance and electrical-length behavior over a wider bandwidth than the conventional single-section lumped transmission line circuit. In the design for X-band applications, parasitic capacitors play an important role in layout design. A parasitic extraction method is presented in this work for capacitor value selection. The layout is designed to have a compact size at ($0.03\lambda_o \times 0.03\lambda_o$). The −10 dB fractional bandwidth is 80.39%. The amplitude balance is 0.1 dB. The phase balance is 5.8° (−13 dB fractional bandwidth of 52.4%, while the amplitude and phase balance are 0.04 dB and 4.9°). Overall, the circuit is compact and has good performance for X-band applications.

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