



Article

A 28.5 nW Analog Circuit Implementing the Pan–Tompkins Algorithm for Heart Rate Monitoring in Pacemakers Dedicated to Small Animals

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Abstract

This article proposes a new integrated analog implementation of the Pan–Tompkins algorithm. This algorithm, generally implemented in the digital domain at the cost of higher power consumption, is one of the most efficient for QRS detection in electrocardiographic signals. This circuit has been designed for use on small mammals like rats for the study of pulmonary arterial hypertension. The specificities of the architecture proposed in this article are a sub-threshold-operated architecture to perform the amplification, noise filtering, and differentiation of the signal in a unique block to limit the power consumption; an analog squarer; and an analog monostable reshaping-circuit followed by a digital counter clocked by an ultra-low power relaxation oscillator. Compared with the state of the art, this circuit, designed with the X-FAB xh018 180 nm CMOS technology, presents one of the lowest power consumptions currently reported, at 28.5 nW, 76% of which is consumed in the current, voltage, and time references. Post-layout simulation results show a reliable 98.57% heart beat detection accuracy using the MIT-BIH arrhythmia database and 99.85% accuracy for healthy sinus rhythm electrocardiograms. The robustness of the circuit is also investigated, and mitigating solutions are proposed for each critical block.

Keywords: ultra-low-power circuit; biomedical circuit; sub-threshold design; electrocardiogram (ECG); Pan–Tompkins algorithm; QRS detection



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1. Introduction

Heart diseases are the leading cause of death worldwide [1] and a major global concern; it has been driving extensive exploratory research into ultra-low-power monitoring devices for decades [2–4]. In this work, we are more specifically interested in pulmonary arterial hypertension (PAH).

PAH is a progressive cardiovascular disease characterized by abnormally high blood pressure in the pulmonary arteries. It burdens patients' daily life and puts them at risk of right heart failure [5]. Researchers from the French National Institute of Health and Medical Research (INSERM) have come up with a hypothesis according to which a prolonged increased heart rate would accelerate the progression of the disease. For this theory to be tested, animal models are essential. Rats offer high experimental reproducibility at moderate cost and provide valuable insights into human health, as their cardiovascular physiology shares key features with that of humans [6]. There is therefore a need for an electrical device capable of modulating a rat's heart rate. A previous work has led to the design of a stimulation circuit tailored for small rodents [7].

The stimulation provided by the aforementioned circuit still has to be monitored. The cardiac electrical activity can be recorded in the form of an electrocardiogram (ECG, Figure 1). The best-defined feature of a mammal ECG signal is the R-peak; most cardiac frequency monitoring techniques therefore revolve around identifying the R-peaks and computing the time interval between them. A trade-off between performance and power consumption has to be taken into account when designing such a circuit as a great variety of methods exists in the state of the art. For instance, some complex approaches such as those based on the Hilbert transform, the wavelet transform, or neural networks achieve great accuracy but rely on power-hungry computational units [8–10]. Their high power consumption (in the μW range) makes these methods unsuitable for implantable ECG sensors. Battery replacement should be avoided, as it requires a surgical procedure that is both costly and associated with procedural risks. This is particularly true in rats, where anatomical constraints limit pacemaker dimensions and smaller devices can accommodate only very small batteries. Other widely used methods include a derivative step that takes advantage of the steep slope of the R-peak to make it easier to identify. First- or second-order derivative-based methods [11–13] have led to very low-power low-area analog implementations consuming as low as 40 nW but may lack accuracy compared to more computation-heavy approaches such as filter banks methods or the Pan–Tompkins algorithm [14]. In this algorithm, the differentiation is followed by squaring, moving averaging, and adaptive thresholding circuits.

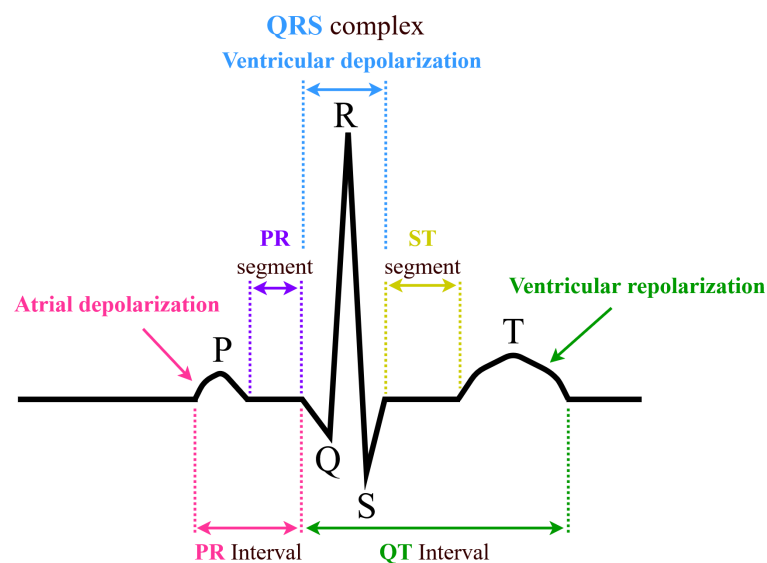


Figure 1. Typical aspect of an ECG signal for mammals.

Pan–Tompkins is often regarded as one of the leading state-of-the-art methods for heart-rate detection in ECGs from healthy subjects with a normal sinus rhythm [15,16].

Both mixed [17] and analog [18,19] architectures are referenced in the state of the art, with mixed/digital approaches showing better accuracy and analog implementations consuming considerably less power [20]. Even deep sub-threshold and very-low-supply-voltage digital circuits cannot reach consumptions as low as the analog state of the art [20,21]. The fact that Pan–Tompkins lends itself well to an analog implementation makes it a very promising method for low-power applications [18] in comparison to typically digital computation-heavy methods like wavelet or Hilbert transforms and neural network-based approaches [22]. Some authors even reported in [19] a deep sub-threshold analog version of the Pan–Tompkins algorithm with a dramatically reduced power consumption of 0.5 nW, nevertheless not taking into account any voltage and current reference circuit nor providing a robustness evaluation.

In this work, we propose an innovative architecture for a mostly analog Pan–Tompkins algorithm for a cardiac frequency detection module suited to murine cardiophysiology realized with X-FAB’s xh018 CMOS technology. Compared to humans, rats have a higher heart rate ranging from 250 bpm to 600 bpm. Another difference with humans is the frequency of the baseline wandering, up to 1.7 Hz, as estimated in Section 2.

This paper is organized as follows: Section 2 describes the experimental protocol that was carried out to observe the specificities of murine intracardiac electrocardiograms (iECGs) and the metrics of interest for our work; system specifications that arose from our experimental observations and sought for performance are then highlighted. Section 3 describes the standard Pan–Tompkins detection algorithm and our proposed adaptation thereof. Section 4 delves into the dimensioning, architecture, and robustness of each individual block, while Section 5 summarizes our post-layout results and provides a comparison with the state of the art.

2. Particularities of a Rat iECG and Specification of the Detection System

Murine electrocardiograms are well documented, especially for Sprague Dawley rats as they are one of the most commonly used strains in cardiovascular experiments [23]. However the vast majority of studies focus on surface ECG recordings, while the input signals of our pacemaker device ought to be intracardiac signals. Human intracardiac signals are known to differ from surface signals in aspect and amplitude [24], and we can only assume that the same goes for rats because of the scarcity of available data. Another aspect of the murine ECG that is not so well documented is its baseline wandering; most ECG recordings and databases present already filtered data without this low-frequency component. These two aspects, combined with the lack of an easily available large database of rat ECG, made it useful to carry out our own unfiltered measurements of surface and intracardiac ECGs on rats.

All experiments were conducted in compliance with the European Community guiding principles in the Care and Use of Animals (2010/63/EU, 22 September 2010), and the French decree no. 2013–118, 1 February 2013 on the protection of animals used for scientific purposes (JORF no. 0032, 7 February 2013, p2199, text no. 24). Authorizations to perform animal experiments according to this decree were obtained from the “Ministère français chargé de l’Enseignement Supérieur et de la Recherche” (authorization APAFIS no. 54132-2025030614382401 v2).

Three male Sprague Dawley rats (231–303 g) were used in this study. Anesthesia was induced with 5% sevoflurane delivered in a mixture of oxygen and air. After induction, a tracheotomy was performed to secure the airway, and the animals were mechanically ventilated with a gas mixture of 40% oxygen and 60% air, continuously supplemented with sevoflurane for maintenance anesthesia (typically 2–3%). Cardiac access for intracardiac measurements was obtained via a median sternotomy. Two wires used as electrodes

were positioned on the right atrium, spaced approximately 2 mm apart. All signals were recorded using WaveForms software v3.25.1 (Digilent, New York, NY, USA) through a 14-bit-resolution Analog Discovery 2 Oscilloscope (Digilent) at a sample rate of 800 Hz. A pre-amplification stage between the electrodes and the oscilloscope was also used; it consisted of an AD621 low-noise instrumentation amplifier (Analog Devices) with a gain set to 10. A picture of the setup is provided in Figure 2. This resulted in the recording of 80 min of surface ECG as well as 4 min of intracardiac ECG.

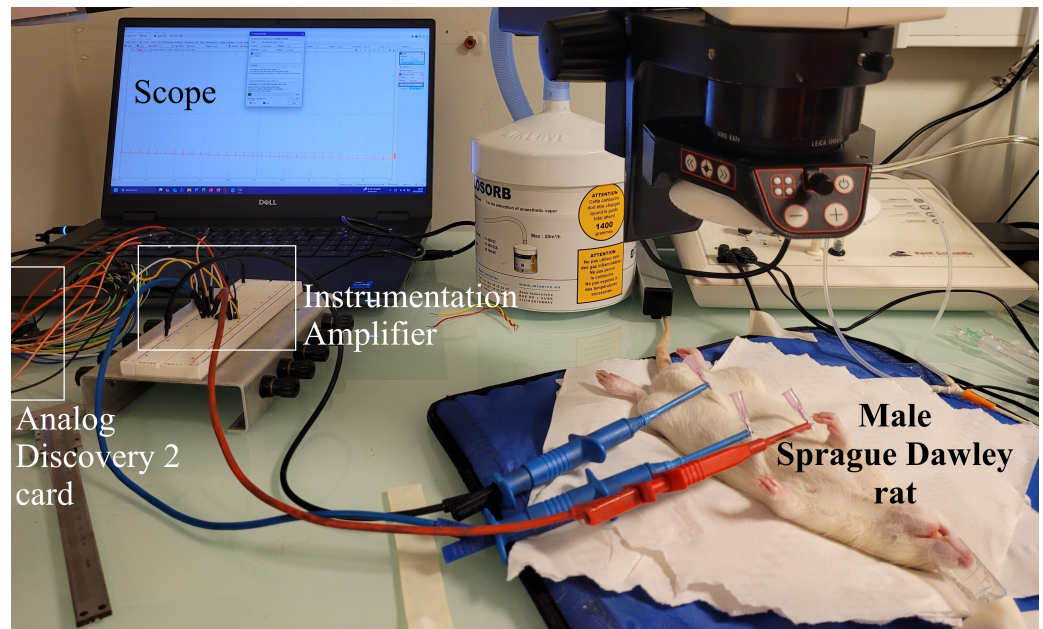


Figure 2. Picture of the experimental setup.

2.1. Characteristics of a Rat iECG Compared to a Standard Human ECG

A typical mammal ECG is shown in Figure 1; it depicts the electrical activity of the heart during a heart beat with the successive depolarization and repolarization of all cardiac chambers, the atria, and the ventricles. Five waves are generally noticeable; they are named P, Q, R, S, and T, with the so-called QRS complex being the most prominent feature.

Figure 3a shows an extract of the surface recording and Figure 3b an extract of the intracardiac recording. The surface recordings show an amplitude of QRS complexes ranging from 0.2 to 1 mV, which is lower than the typical 0.5 to 3 mV observed in humans [25]. These recordings allowed us to measure the low-frequency baseline wandering of our signal. Performing a Fast Fourier Transform on the collected ECGs highlights a low-frequency component that varies from an individual to another and ranges from 0.8 to 1.7 Hz. This is higher than the frequency of human baseline wandering, which is usually below 0.5 Hz [26]. Another main source of noise is the 50 Hz power line disturbance.

Then, the intracardiac recordings give us easily identifiable P waves and QRS complexes (Figure 3b). As expected [23], the QRS complexes of rats are approximately 4 to 5 times shorter (18–25 ms) than those of humans (80–105 ms). In addition, the amplitude of these intracardiac QRS complexes ranges from 5 to 16 mV, significantly higher than for surface ECGs, even human ones.

As a result, our measurements confirmed that the specifications of our heart rate detection module differ from those of the state of the art that is typically meant for human surface ECGs. The higher baseline wandering frequency means a higher high-pass cutoff frequency is needed for the front-end, and the larger amplitude means that we can settle for a lower gain, which is favourable in terms of circuit area and consumption.

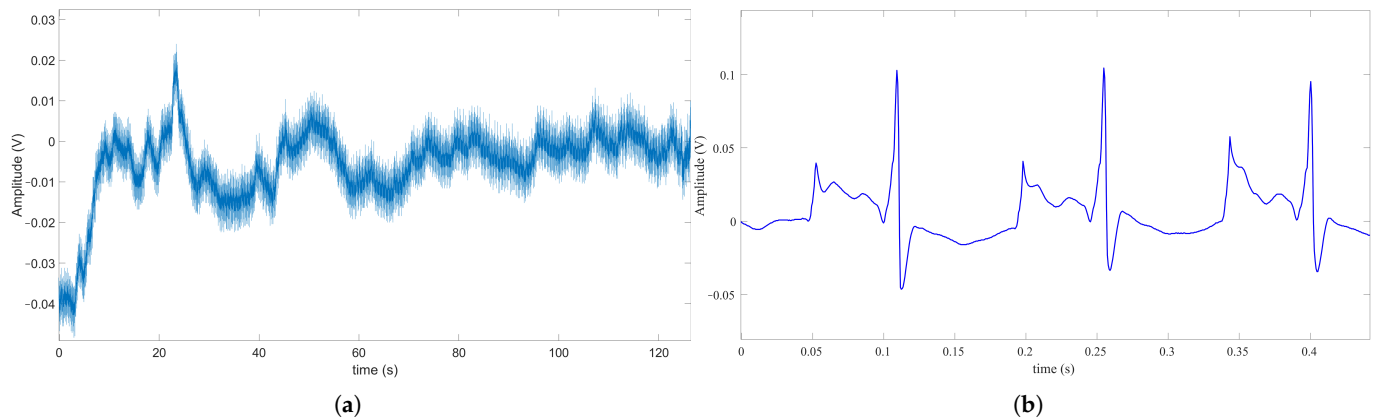


Figure 3. (a) A 125 s segment of the measured rat surface ECG, highlighting the baseline wandering. Applied gain of 10. (b) A 0.45 s segment of the measured rat intracardiac ECG. Applied gain of 10.

2.2. Metrics of Interest and Specifications

When it comes to the evaluation of heart rate detection modules, the Association for the Advancement of Medical Instrumentation (AAMI) encourages the use of two particular metrics: sensitivity (Se) and positive predictivity (PP) [22,27],

$$Se = \frac{TP}{TP + FN} \quad (1)$$

$$PP = \frac{TP}{TP + FP} \quad (2)$$

where TP is the number of true positive detections, FN the number of false negatives, and FP the number of false positives. A third metric, the detection accuracy, can also be used to combine the sensitivity and positive predictivity of the module. A minimal accuracy of 95% would be considered acceptable in our case.

$$Acc = \frac{TP}{TP + FN + FP} \quad (3)$$

3. Pan–Tompkins Algorithm and Proposed Architecture

This section focuses on the system-level architecture with, first, a description of the standard Pan–Tompkins algorithm and, second, an overview of all proposed modifications.

3.1. Standard Pan–Tompkins Algorithm

The Pan–Tompkins algorithm is named after its inventors who first introduced it in 1985 in [14]. It is composed of a series of filters that highlight the frequency components of the ventricular depolarization and remove background noise, followed by a derivation stage, a squaring stage, and a moving average filter. A decision stage then comes with peak detection logic after the pre-processing to output the heart rate (see Figure 4a).

- The first stage consists of a band-pass filter to acquire, isolate, and amplify the frequency band of the R-peak.
- The derivative stage is used to highlight the steep slope of the R-peak, which is a unique characteristic among the P-to-T waves of the ECG signal, and is therefore a useful step towards identification of these peaks.
- After the differentiation, the observed peaks are successively positive (rising edge of the R-peak) and negative (falling edge of the R-peak). The squaring stage transposes all the signals in the positive domain and amplifies the dominant peaks so as not to confuse R-peaks with abnormally steep P-or-T waves.

- A moving average filter is then used to smoothen the peaks and give an indication about their duration.

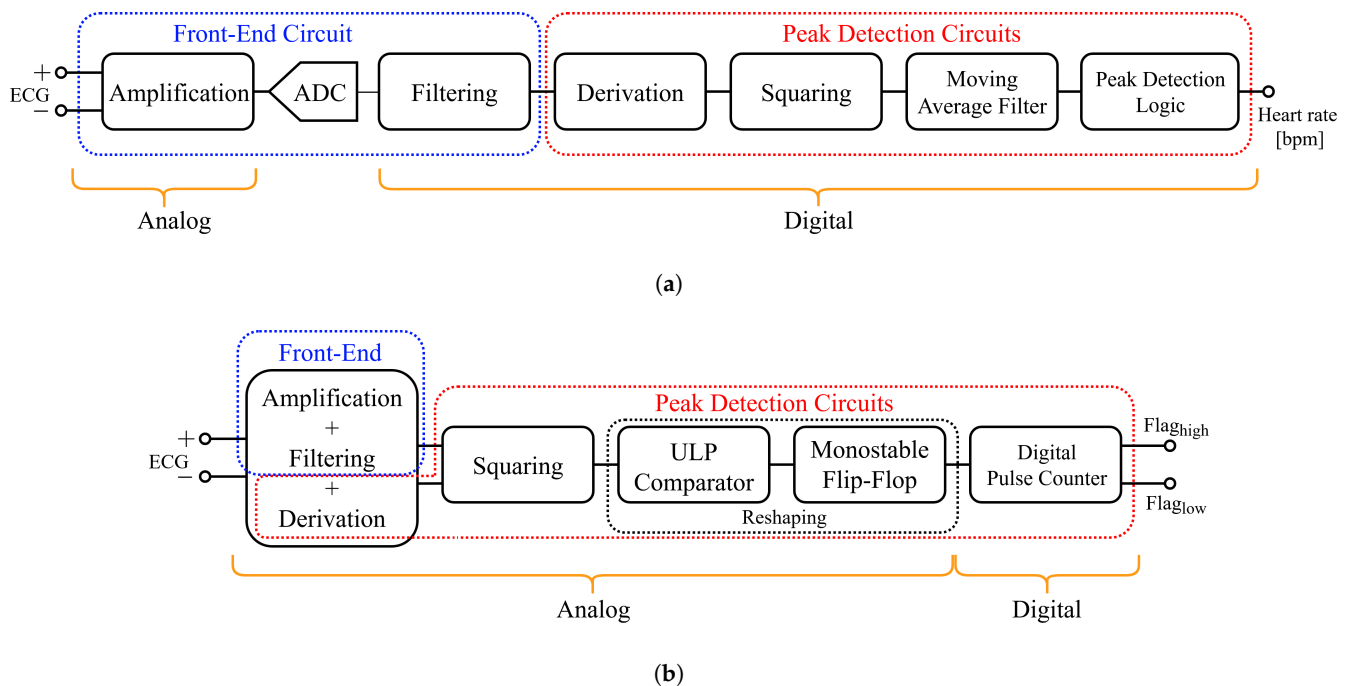


Figure 4. (a) Typical processing chain for the Pan-Tompkins algorithm. (b) Proposed adaptation of the Pan-Tompkins algorithm.

The peak detection logic is then based on adaptive thresholding to discriminate proper QRS complexes from noise peaks.

This algorithm is very promising as it is suitable for an analog implementation. It should still be noted that its later processing steps include a moving average filter and detection logic that are more suitable for digital designs that can allow themselves to have higher power consumption and chip area [28]. In order to strive towards an ultra-low-power fully analog implementation, some modifications to the original Pan-Tompkins algorithm are necessary.

3.2. Proposed Implementation of the Pan-Tompkins Algorithm

The modified processing chain of the designed circuit is shown in Figure 4b. To reduce the power consumption, the proposed modified Pan-Tompkins architecture combines the amplification, noise filtering, and differentiation of the signal into a unique front-end block. Pan-Tompkins band-pass front-ends are typically centered around the frequency band of the QRS complex, between 4 and 25 Hz [15,22]. In our case, the center frequency of the band-pass filter is voluntarily shifted to the right, which allows us to place the QRS frequency band in the domain where the filter acts as a high-pass differentiator. Shifting the center frequency to the right also helps compensate the fact that the observed baseline wandering frequency for rats is higher than for humans. The filtering of the 50 Hz power line disturbance will be less satisfactory but a narrow enough band width should still allow it to be filtered out.

Combining the amplification, the noise filtering, and the differentiation into a single block with a single operational transconductance amplifier (OTA) enables us to limit the die area dedicated to these parts of the circuit compared to solutions implementing them separately [29]. This is also true in terms of power consumption because the OTA is the most power-hungry component in our design excluding reference generators.

In the proposed chain, the implementation of the squaring takes place in the analog domain rather than in the digital domain. Keeping the signal analog allows us to replace the typically digital moving average filter with a simple low-power analog solution. The selected topology is a reshaping circuit made up of an ultra-low-power PMOS comparator and a monostable flip-flop. Under nominal conditions, the comparator is triggered twice per heart beat and produces exactly two rail-to-rail impulses, corresponding, respectively, to the rising and falling edges of the R-peaks. A potential third or fourth impulse can also appear right before or right after in case of a particularly steep P-or-T wave. Therefore, this signal is fed to a monostable flip-flop. It is dimensioned to only generate a single impulse covering the whole duration of the heart beat. These single rail-to-rail impulses are then suitable as inputs for a digital pulse counter that counts all those impulses over a defined time period and raises a flag if the cardiac frequency is too high or too low compared to the targeted one. In a full pacemaker device, this information would then be fed back to the stimulation circuit [7] in order to accordingly modulate the pacing automatically.

This solution enables us to not only replace the potentially large and consuming moving average filter but also get rid of the adaptive thresholding circuit that can account for up to two thirds of the circuit's die area in some cases [19].

4. Circuit Design and Dimensioning

The selected technology for the design is X-FAB's xh018 CMOS process, which is a mature technology that is suited for a 1.8 V power supply, is certified by ISO 13485 [30] for commercial medical devices, and proposes insulated well transistors. Insulated wells allow us to bias the substrate of the transistors independently from each other, thus keeping the voltage difference between sources and bulks under control and preventing threshold voltage discrepancies between transistors, which is especially useful when designing differential pairs. All NMOS transistors described below are 0.35 V threshold voltage neli transistors, and all PMOS transistors are -0.35 V threshold voltage peli transistors. Because the system should ultimately be implantable, all simulations were carried out with a temperature set to 37.3 °C, corresponding to a standard murine internal temperature [31].

An overview of the whole design is shown in Figure 5. Unless otherwise stated, all CMOS circuits are operated in the sub-threshold region [32]. Sub-threshold design has led to tremendous progress in low-power analog sensing for biomedical applications, notably for electrocardiograms [21] and electroencephalograms [33]. Sub-threshold design guidelines, presented in [33,34], were used when designing the circuit:

- Biasing: at very low currents ($V_{GS} \leq 0$ V, $I_d \leq 10^{-11}$ A), the current leakage limits the measurable current. Therefore biasing currents lower than 10 pA should be avoided [35].
- Matching: sub-threshold operated circuits are more sensible to mismatch. When it comes to the sizing of the transistors, there is a direct trade-off between mismatch and bandwidth as larger transistors have better matching but larger parasitic capacitances and a narrower bandwidth, which is not a problem when working below 100 Hz. Larger transistors will therefore lead to more robust designs, and minimum-sized transistors should be avoided to prevent mismatches.
- Noise immunity: When working at low frequencies, circuits are more sensible to $1/f$ flicker noise. This is another reason to favour larger widths W and lengths L for our transistors as the power spectral density of flicker noise is inversely proportional to WL [34]. Moreover, it has been shown that PMOS transistors present about one order of magnitude lower $1/f$ noise than NMOS transistors, especially in weak inversion [36]. PMOS should therefore be prioritized over NMOS.

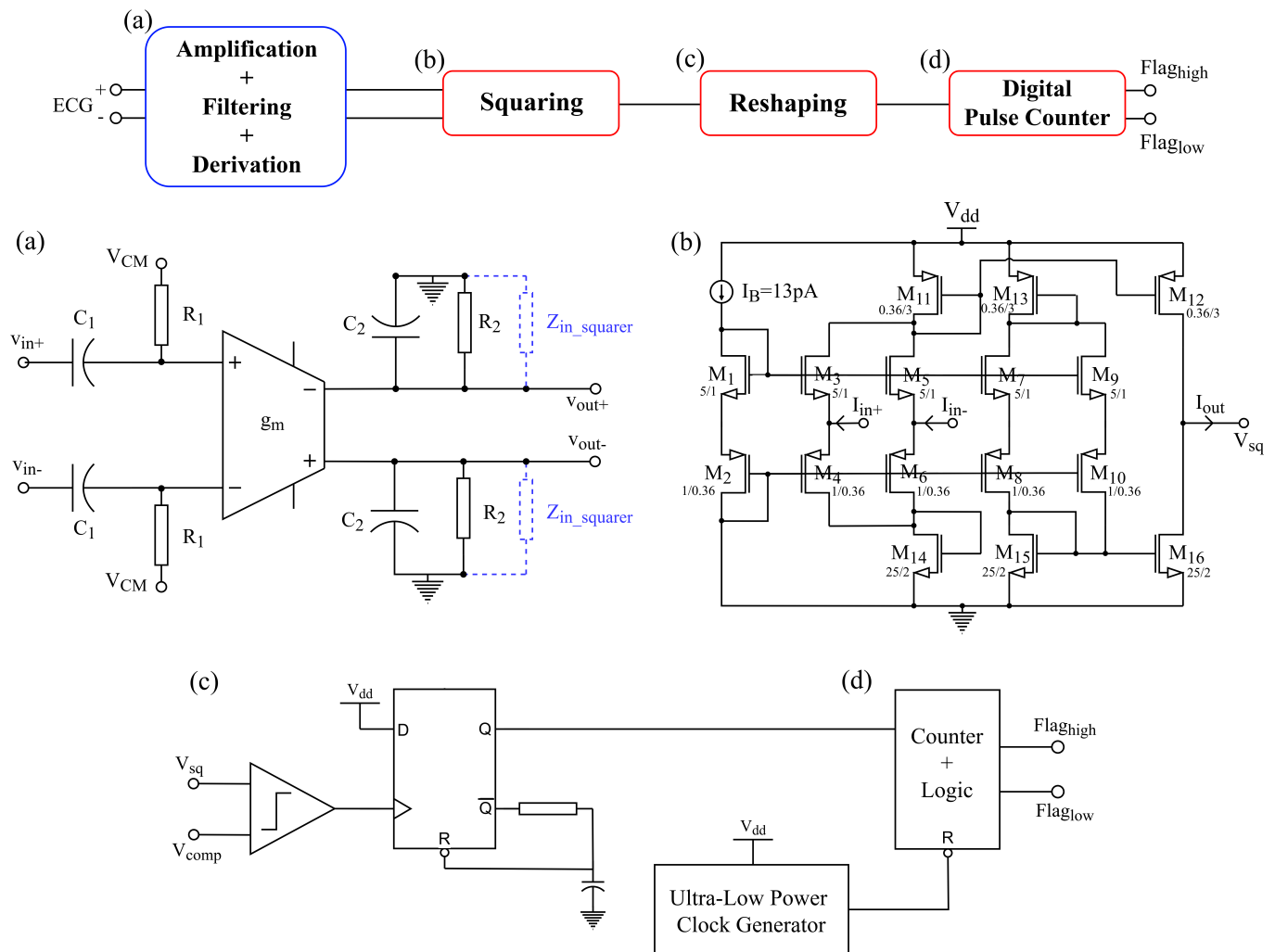


Figure 5. Proposed adaptation of the Pan–Tompkins algorithm—circuit view. (a) All-in-One Front-End. (b) Squaring Circuit. (c) Reshaping Circuit. (d) Digital Pulse Counter.

4.1. All-in-One Pan–Tompkins Analog Front-End

The analog front-end is the first block of the signal processing chain for an ECG. The features of the signal sent to the rest of the circuit have to be as well-defined as possible, thus making the front-end a pivotal block in the chain. The main particularity of a front-end designed for RR-interval detection is to include a band-pass topology to specifically amplify R-peaks. The relevant frequency band for QRS complexes is considered to be between 4 and 25 Hz [15,22]; however, as explained in Section 3.2, the aim here is also to specifically differentiate the ~ 20 Hz R-peak by shifting the center frequency to the right towards frequencies higher than 20 Hz. The front-end also needs to effectively filter the power line disturbance and the baseline wandering, and would ideally also filter the P-and-T waves or at least amplify them less than the R-peak. Typical frequencies for P-and-T waves are considered to range from 5 to 10 Hz [37], which makes their filtering difficult. Therefore, the bandwidth has to be rather narrow, which is achieved by setting high-pass and low-pass filters at cutoff frequencies close to each other. Having both cutoff frequencies so close to each other will significantly damage the gain of the band-pass filter but will ensure a narrow enough bandwidth. Finally, by shifting the bandwidth to the right, we not only filter out the low-frequency baseline wandering well but also eliminate the P-and-T waves more efficiently than with a bandwidth centered around the frequency of the QRS complex.

4.1.1. Global Architecture

Our fully differential band-pass front-end is presented in Figure 5a. It consists of a high-pass filter achieved with components R_1 and C_1 and a low-pass filter achieved with g_m , R_2 , and C_2 . The high-pass filter is placed first in the processing chain because the low-frequency baseline wandering could cause saturation in the following blocks if it is left untouched; its amplitude can indeed reach values up to a few volts for humans, as can be seen in the database presented in [16].

It should be noted also that in Figure 5a, the impedance $Z_{in_squarer}$ has been added to model the input impedance of the squaring circuit, which is the following stage in the proposed Pan–Tompkins implementation. The transfer function can be expressed in the following way:

$$H(s) = \frac{(v_{out+} - v_{out-})}{(v_{in+} - v_{in-})} = -\frac{2Z_{eq}g_mR_1C_1s}{(Z_{eq}C_2s + 1)(R_1C_1s + 1)} \quad (4)$$

where Z_{eq} is R_2 in shunt with the input impedance of the squarer:

$$Z_{eq} = \frac{R_2Z_{in_squarer}}{R_2 + Z_{in_squarer}} \quad (5)$$

Based on the transfer function, it is possible to detail the frequency response of the filter. Figure 6a shows a simplified representation of the different contributions to the amplitude Bode diagram; this simplified diagram overestimates the gain as it ignores the attenuation occurring around both cutoff frequencies. As can be seen, it is necessary to dimension R_2 in the presence of $Z_{in_squarer}$ to obtain the desired frequency for the low-pass filter because the input impedance of the squarer will tend to shift the filter towards higher frequencies. The targeted center frequency of the band-pass filter has been chosen to be 25 Hz because it will at the same time filter out the 50 Hz power line disturbance and any high-frequency artifact. Consequently, the values of the components have been chosen to obtain

$$\frac{1}{2\pi R_1 C_1} = \frac{1}{2\pi Z_{eq} C_2} = 25 \text{ Hz} \quad (6)$$

Obtaining a high-pass cutoff frequency as low as 25 Hz raises integration issues. Indeed, passive filters cannot be reasonably implemented on a chip with a corner frequency this low as the required resistance and capacitance values would be too large. Integration of high-value on-chip capacitors is possible but leads to very large chip areas [38]; it would not be reasonable with our selected technology to integrate capacitors larger than 100 pF. There exist solutions in the literature consisting of building a passive filter outside the chip on a printed circuit, but this results in a system too voluminous for our study [39]. We therefore had to resort to designing pseudo-resistors made of transistors like those introduced in [40] to achieve high equivalent resistance values; the sizing of these pseudo-resistors is detailed in Section 4.6.

Ultimately, the selected components values are pseudo-resistor $R_1 = 400 \text{ M}\Omega$, $C_1 = 15 \text{ pF}$, and pseudo-resistor $R_2 = 720 \text{ M}\Omega$, $C_2 = 15 \text{ pF}$.

Figure 6b provides the Bode diagram obtained by AC simulation with this dimensioning when the front-end is loaded by the following squaring circuit, in typical process variation conditions as well as all possible worst cases.

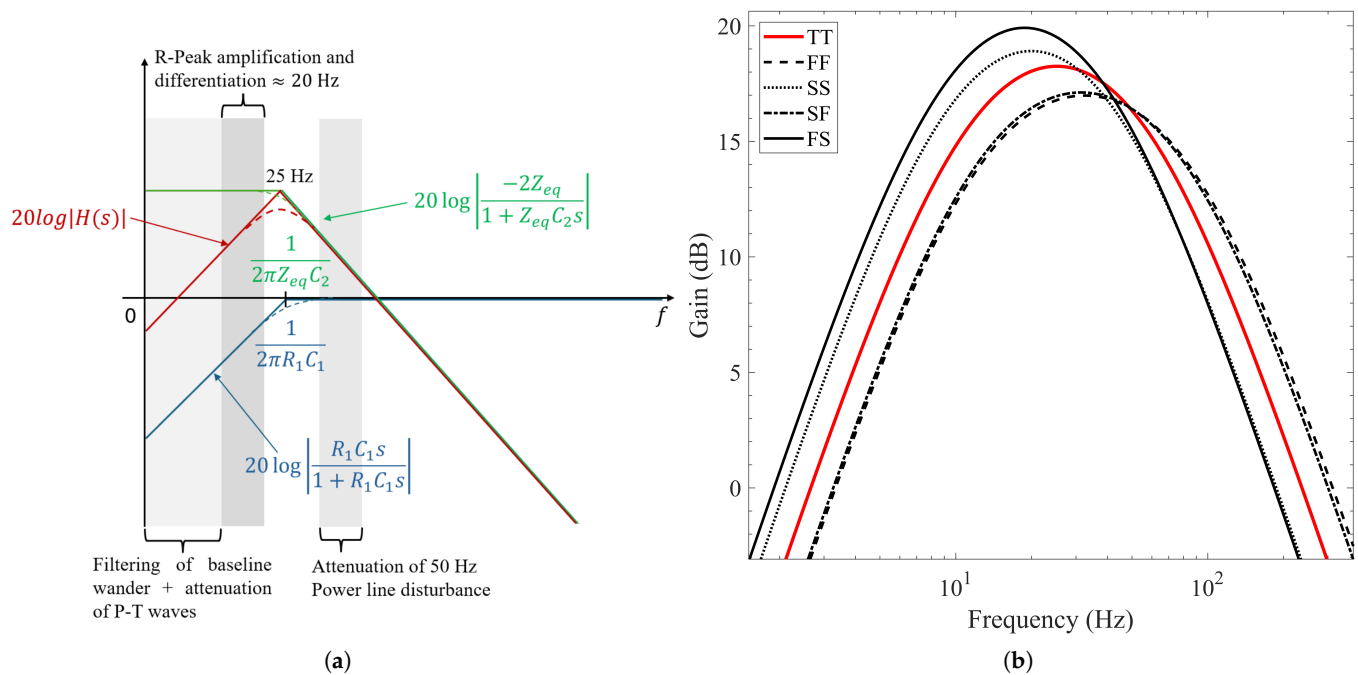


Figure 6. (a) Simplified amplitude Bode diagram of the band-pass front-end. (b) Bode diagram of the band-pass front-end under nominal conditions and all process variations corner cases, obtained by AC simulation.

The Bode diagram shows a 25 Hz center frequency and a -3 dB bandwidth ranging from 10.9 to 57.2 Hz in nominal conditions. The frequency response of the front-end is also depicted in four process variation worst cases. These corner cases (FF, SS, SF, and FS) are what the manufacturer is able to guarantee when it comes to process variations; the first letter corresponds to the toggling speed of the N-type transistors (F is fastest, S is slowest, and T is typical), whereas the second letter corresponds to the toggling speed of the P-type transistors.

For typical process variations, the center frequency gain of the filter is 18.4 dB for a 25 Hz frequency so that the R-peak is both amplified and derivated. Indeed, this placing of the center frequency combined with a narrow bandwidth places the ~ 20 Hz R-wave in the region where the Bode diagram of the filter presents a $+20$ dB/decade slope corresponding to a differentiation, while also maintaining an acceptable 17 dB amplification. This narrow bandwidth also leads to a very efficient filtering of the 1–2 Hz baseline wandering. The filtering of the 50 Hz power line disturbance is not as efficient but still acceptable as the 15 dB gain at 50 Hz keeps it 2.4 dB below the R-peak. It should also be noted that process variations may cause fluctuations in gain from 17 to 20 dB and in center frequency from 20 to 32 Hz.

The resulting transient signal for a typical ECG input, like the one shown in Figure 7a, is shown in Figure 7b. The derivating effect on the signal can be observed with a positive peak followed by a negative peak corresponding to the rising and falling slopes of the R-peak.

The design of the OTA, the most central part of the band-pass front-end, is detailed in what follows.

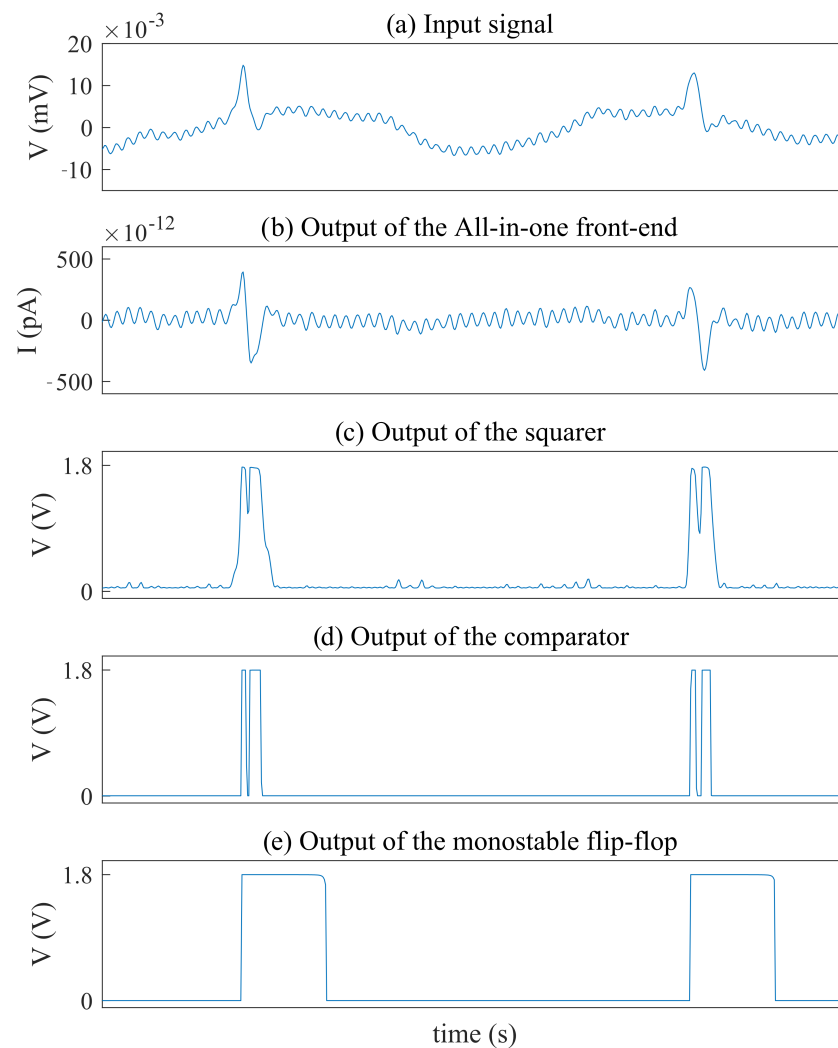


Figure 7. Outputs of the successive processing blocks: (a) Raw input. (b) All-in-one front-end. (c) Squarer. (d) ULP comparator. (e) Monostable flip-flop.

4.1.2. Sub-Threshold Operational Transconductance Amplifier (OTA) and Common-Mode Feedback

The most critical part of the front-end is its OTA. An operational amplifier not robust enough, with an unbalanced differential pair or an unstable common-mode voltage, would possibly render the whole circuit inoperable in the worst cases of manufacturing process variations. It should therefore be very carefully designed. Our OTA is a one-stage fully differential PMOS OTA with 34 nS transconductance, the dimensions of which are detailed in Figure 8a in the format W/L in μm . With all transistors operating in sub-threshold mode, the transconductance is given by

$$g_m = \frac{I_{B_OTA}}{2nV_t} = 34 \text{ nS} \quad (7)$$

Ref. [33] with $I_{B_OTA} = 2.1 \text{ nA}$ the bias current in the OTA, $n \approx 1.2$ the sub-threshold slope factor in the used process, and $V_t = \frac{kT}{q} \approx 25.9 \text{ mV}$ the thermal voltage. While a maximum transconductance $g_m = 34 \text{ nS}$ is observed when both inputs are equal, it is not constant in this topology and depends on the input differential voltage. Figure 9 shows the evolution of g_m versus the input differential voltage.

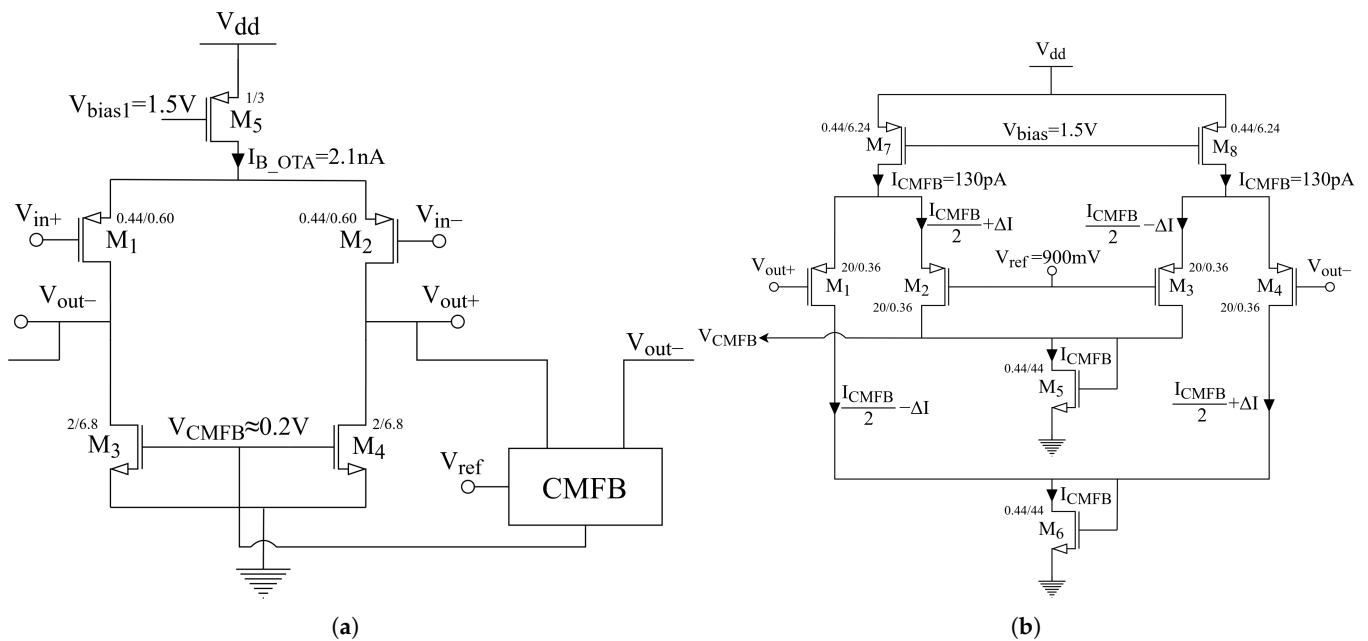


Figure 8. (a) Structure of the designed OTA. (b) Structure of the designed Common-Mode Feedback (CMFB) circuit.

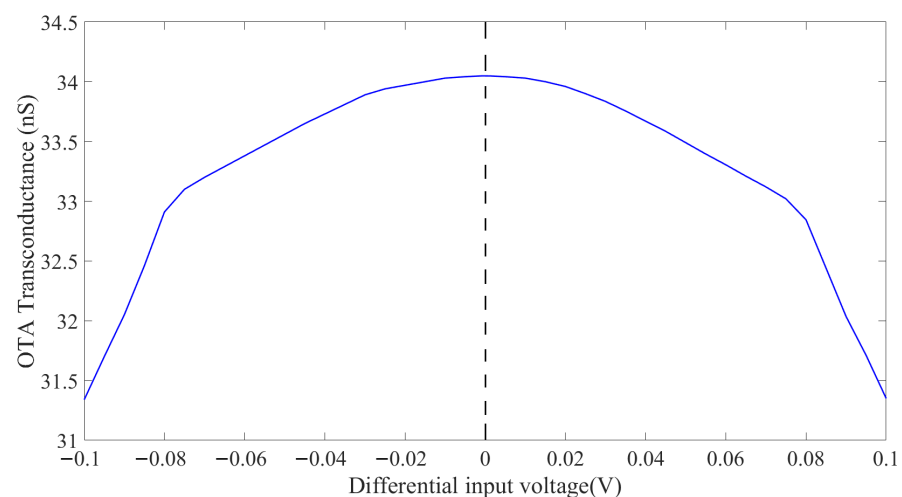


Figure 9. Evolution of the OTA Transconductance depending on the input differential voltage.

As a fully differential circuit, it has several advantages compared to single-ended ones: First, it offers an output swing twice as large as it makes full use of the swing available at two circuit nodes, while the power consumption stays similar [41] (Chapter 6, p. 281). Another major benefit is the cancellation of the common-mode noise, which is considered to be the main source of noise due to the fluctuations in power supply and bias voltages. As common-mode noise is identical on both sides, it will not appear on the differential output. More generally, all even-order distortions will be cancelled thanks to their symmetry around the common-mode voltage $V_{CM} = 900$ mV. This contributes to providing a “clean” undistorted signal for the rest of the chain. However, a known issue with fully differential circuits like the front-end we designed is that the common-mode (CM) component of the signal is not processed like the differential-mode component. The CM path has to be designed in a way that clearly defines the CM output level; otherwise, the smallest of CM drifts with no corresponding variation in the currents could drive the amplifier out of its high-gain operating region and slowly drive all nodes of the circuit to the ground [42]. Thus, a Common-Mode Feedback (CMFB) circuit (see Figure 8b) is used to

provide negative feedback in the CM path, and define and stabilize the CM output voltage to make the whole circuit more robust regarding process variations and sensitivity.

The chosen CMFB architecture is a Continuous-Time CMFB; it was introduced by Whatley in [43]. The working principle is to measure the error between the common mode of V_{out} and the desired common-mode level V_{ref} and to then generate a proportional bias voltage for the amplifier to set the output common mode back to the desired level.

Our OTA has one pair of high impedance output nodes needing CM stabilization. Therefore, only one CMFB circuit is needed.

To very grossly explain the working principle, let us assume that

- V_{bias} is chosen so that M7-8 act as current sources generating a constant bias current I_{CMFB} .
- V_{out+} and V_{out-} have their differential mode equal in magnitude but opposite in sign.
- The CMFB differential pairs have an infinite CMRR, meaning that the large signal output only depends on the input differential voltage [41] (Chapter 6, p. 288).

With both input pairs receiving the same differential voltage, the currents flowing through M1 and M3 are the same. We can chose to express it as $\frac{I_{CMFB}}{2} - \Delta I$, with ΔI the large-signal current change. Same goes for the current through M2 and M4 being equal to $\frac{I_{CMFB}}{2} + \Delta I$. This symmetry ensures that the current I_5 flowing through the diode-connected M5 remains stable and equal to I_{CMFB} even if the differential voltage takes very high values. I_5 sets the voltage V_{CMFB} across M5 that is used to control the bias voltage of the output transistors of the OTA.

Let us now assume that the common-mode of V_{out} drifts and becomes greater than the reference voltage V_{ref} . This imbalance will cause I_2 and I_3 to increase; as a result $I_5 = I_2 + I_3$ will increase, as well as V_{CMFB} . V_{CMFB} biases transistors M3-4 in Figure 8a. A direct consequence of its increase is higher currents pulling down to the ground through these two transistors, thus pulling $V_{out,CM}$ back to V_{ref} .

4.1.3. Comprehensive Characterization of the OTA

An AC simulation of the designed OTA together with its Common-Mode Feedback circuit has been performed, the resulting gain and phase Bode diagram is shown in Figure 10. As it appears, the block can be approximated by a second-order transfer function for frequencies below 10 MHz:

$$H_{OTA}(s) = \frac{K}{(1 + \frac{s}{\omega_0})(1 + \frac{s}{\omega_1})} \quad (8)$$

with $K = 55.6$ (or 34.9 dB) the DC gain, and $\omega_0 = 25.1 \text{ krad}\cdot\text{s}^{-1}$ resulting in a cutoff frequency at $f_0 = \frac{\omega_0}{2\pi} = 4 \text{ kHz}$. A non-dominant pole can be noticed at $f_1 = 2.5 \text{ MHz}$ with $\omega_1 = 15.7 \text{ Mrad}\cdot\text{s}^{-1}$.

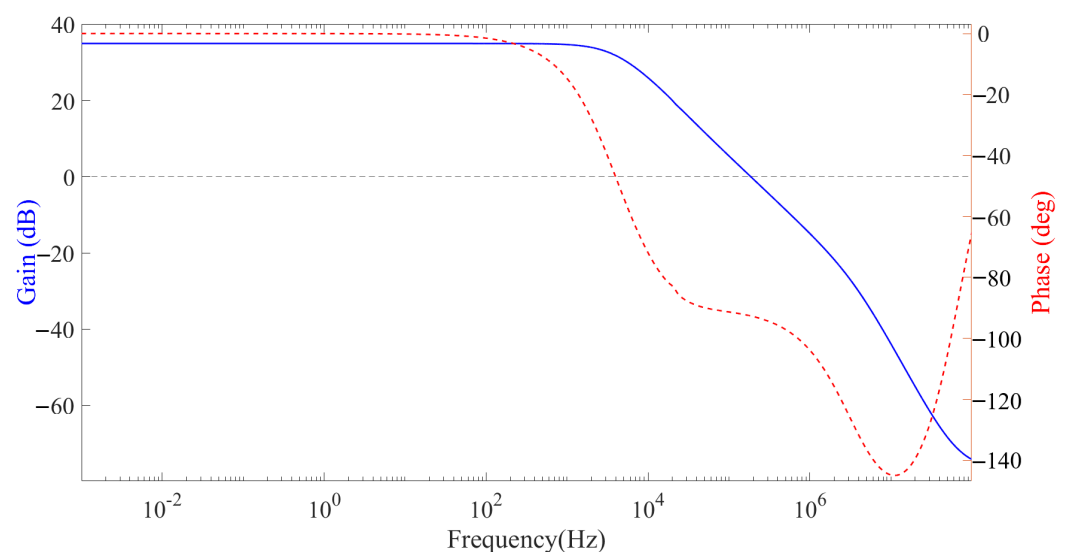
The performance of the OTA is summarized in Table 1. It shows a satisfying stability with a 87.4° phase margin. It should also be noted that the input linear range is limited to around 19 mV due to all transistors operating in the weak inversion region.

Table 1. Post-layout characteristics and performance of the designed OTA with its CMFB.

Parameter	Value
DC Gain	34.9 dB
Bandwidth	0–4 kHz
Gain-Bandwidth Product	223 kHz

Table 1. *Cont.*

Parameter	Value
Phase Margin	87.4°
Gain Margin	undefined (phase does not cross −180°)
Output impedance	1.6 GΩ
Input referred offset	7.0 μV
Input linear range	[−11.4 mV; 7.5 mV]
Output linear range	[−747 mV; 741 mV]
THD	0.75% (−42.5 dB) @10mV _{P-P} input 6.8% (−23.4 dB) @100mV _{P-P} input
Input referred noise	58 μV/√Hz @100mHz 3.89 μV/√Hz @20Hz

**Figure 10.** Bode diagram of the designed OTA with its CMFB circuit.

4.2. Squaring Circuit

After amplification, noise filtering, and derivation, the signal needs to be squared in a squaring circuit. Its purpose is to further enhance the R-peaks compared to the rest of the signal. Contrary to all others parts of the circuit, the input translinear loops (transistors M1-to-6 in Figure 5b) of the squarer are operated in the strong inversion region but with a very moderate current of 13 pA coming from a sub-threshold current source. While sub-threshold squarers are realizable and exist in the literature, their very low gain makes the use of large external components such as capacitors or inductors unavoidable [44]. With external components come larger chip areas and power consumptions actually similar to or higher than those of saturation squarers [45,46] while also being more sensible.

Saturation squarers take advantage of the voltage–current characteristic of MOS transistors in strong inversion to achieve the squaring of the input:

$$I_d \approx \frac{\mu C_{ox}}{2} \frac{W}{L} (V_{GS} - V_{th})^2 \quad (9)$$

The designed squaring circuit can be seen in Figure 5b and was inspired by [46]. It is a differential-input single-ended-output circuit with two translinear loops (made up of

transistors M1,2,3,4 and M1,2,5,6). Assuming that those 6 MOS are operated in saturation mode, using Kirchhoff's current law on those two loops gives us:

$$I_{d3} = \frac{(4I_B - I_{in+})^2}{16I_B} \quad (10a)$$

$$I_{d4} = \frac{(4I_B + I_{in+})^2}{16I_B} \quad (10b)$$

$$I_{d5} = \frac{(4I_B - I_{in-})^2}{16I_B} \quad (10c)$$

$$I_{d6} = \frac{(4I_B + I_{in-})^2}{16I_B} \quad (10d)$$

Transistors M7,9 and M8,10 are sized identically to M1,3,5 and M2,4,6, respectively, so that $I_{d8} = I_{d10} = I_B$. Unity-gain current mirrors M11,12 and M15,16 are then added to get, respectively, $I_{d12} = I_{d3} + I_{d5}$ and $I_{d16} = I_{d8} + I_{d10} = 2I_B$. If we assume that the positive and negative input currents are equal in magnitude and opposite in sign, we obtain

$$I_{out} = I_{d12} - I_{d16} = \frac{I_{in}^2}{8I_B} \quad (11)$$

Figure 11 plots the voltage output against the intensity of the differential input currents, for a given bias current $I_B = 13$ pA in all process variation corner cases. As it appears, the squarer behaves as a squarer in a different operating range of the current for each corner case and reaches saturation for high-input currents. The operating range of the circuit depends directly on I_B , which was kept as low as possible to ensure a low power consumption. The circuit was designed in such a way that we can take advantage of the saturation phenomenon to identify the R-peaks on the ECG. Indeed, if the filtering and differentiation are properly performed, the R-peaks are enhanced and prominent enough compared to the other features of the ECG, thus making it possible to choose a front-end gain that allows us to have amplitudes of the R-peaks above the ± 240 pA (under nominal conditions) saturation threshold while maintaining all other features well below it, preferably under ± 50 pA so that they are barely, if at all visible, after the squaring. This explains the 18.4 dB gain and the 34 nS transconductance chosen, respectively, for the front-end and its OTA. The most critical worst cases are SS, SF, and FS, with the squarer saturating at ± 115 pA in the SS/SF cases and saturating at ± 470 pA in the FS case. The current–voltage conversion at play is related to the very high output impedance of the squaring circuit, which explains that a voltage saturation can be reached even with an output current limited to a few hundred pA. The equivalent resistance of MOS transistors can be expressed as [41] (Chapter 1, p. 28 and p. 53)

$$r_{ds} = \frac{L}{\lambda_L I_D} \quad (12)$$

with L the length of the transistor, λ_L a technology dependant constant around $0.08 \mu\text{m} \cdot \text{V}^{-1}$ in our case ([41], Chapter 1, p. 53), and I_D the drain current. Thus, in sub-threshold operation, very high output impedance values can be reached due to the low currents involved.

An example of the aspect of the signal after the squarer is shown in Figure 7c.

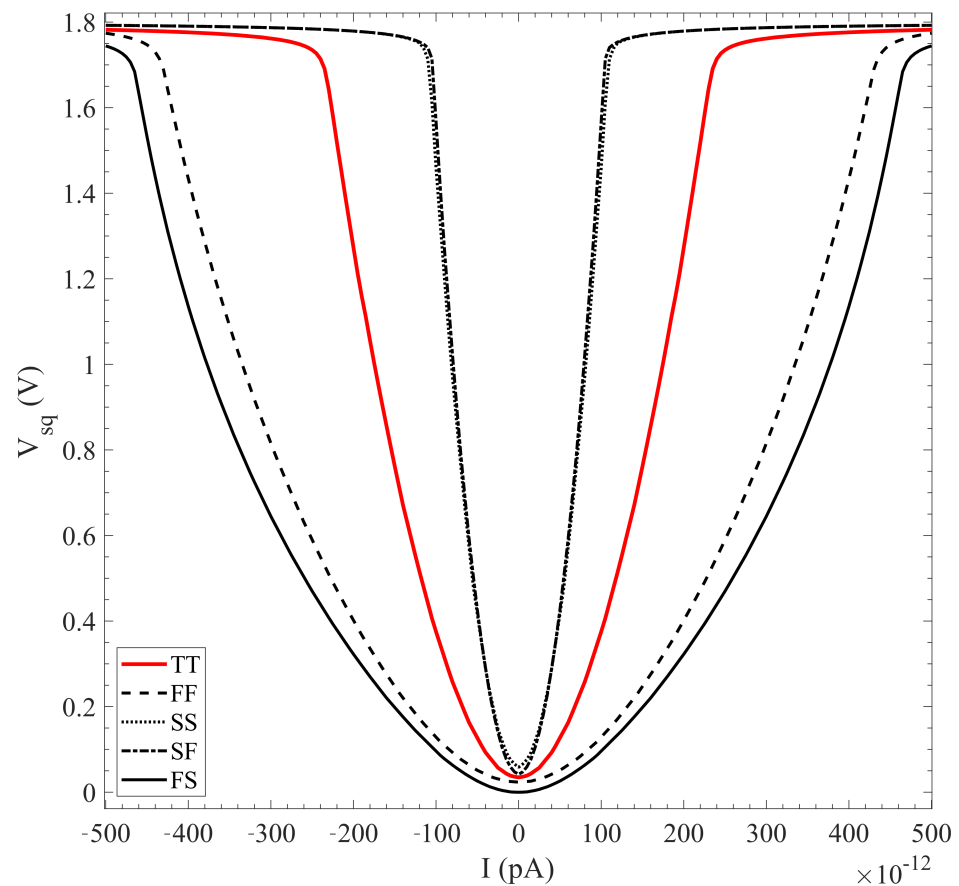


Figure 11. Output of the squarer circuit with a 13 pA bias current against its differential input current in the typical case and all process variation corner cases.

4.3. Reshaping Circuit and Pulse Counter

The reshaping circuit is illustrated in Figure 5c and detailed in Figure 12. Its purpose is to uniformize the signal but also to remove potential inconsistencies regarding the amount of peaks per heart beat. As explained in Section 3.2, two peaks should be observed, corresponding, respectively, to the rising and falling slopes of the R-peak. However, the circuit is more sensible in the FF and FS worst cases, which may lead to some abnormally steep P-or-T waves being amplified by the squarer, thus showing three or four peaks. And, it is less sensible in the SS and SF worst cases, making it possible to only observe one single peak. To reshape the multiple-peak signal at the output of the squarer into a one-peak rail-to-rail signal suitable for simple low-power counting, a two-step circuit is implemented. It consists of a comparator followed by a monostable circuit. The output of the monostable is then applied to a digital counter (see Figure 5d).

The comparator is an ultra-low-power comparator, taken from [7], that provides a proper rail-to-rail signal by comparing the squarer's output to a 1.5 V threshold provided by the autopolarized voltage source detailed in Section 4.5. It is composed of a sub-threshold OTA followed by a dynamic leakage suppression logic [47] inverter (see Figure 12a) and thus does not work properly at frequencies higher than 100 Hz, which is not a problem in our case as murine hearts do not beat faster than around 600 bpm, i.e., 10 Hz. Its effect on the signal can be seen in Figure 7d. The 1.5 V value was chosen for two reasons:

- It guarantees that the PMOS M_5 , acting as a bias current source in Figure 12a, is biased in sub-threshold mode. It is indeed a peli transistor with an estimated threshold voltage $V_{th} = -0.35$ V; having $V_{comp} = 1.5$ V ensures a gate-source voltage $V_{GS} = -0.3$ V $>$ V_{th} .

- The output of the squarer has been observed to reach at least 1.5 V for every healthy ECG recording from the database introduced in [16] in all of the process variation worst cases. $V_{comp} = 1.5$ V therefore ensures that the comparator triggers at least once per healthy heart beat in all of these worst cases.

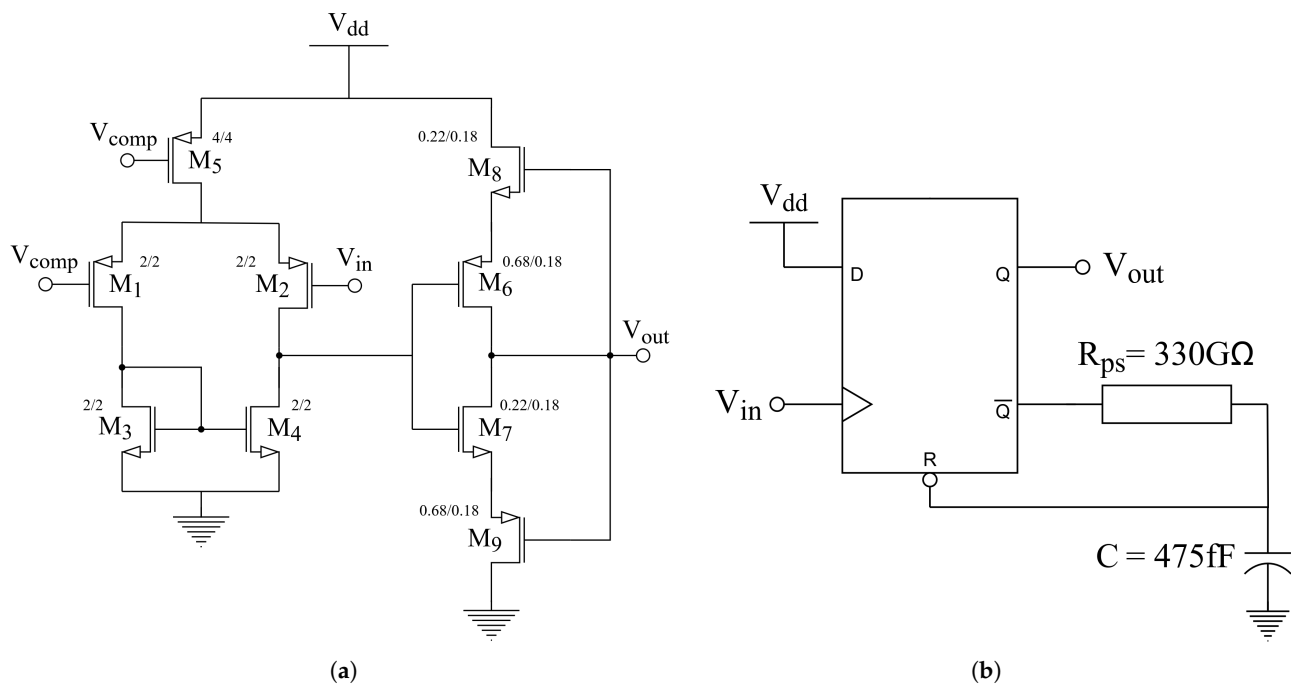


Figure 12. (a) Structure of the dynamic leakage suppression comparator. (b) Structure of the monostable flip-flop.

The monostable flip-flop then consists of a low-leakage D-type flip-flop, an output of which loops on its reset pin (see Figure 12b). When the comparator is triggered, the rising edge at its output causes the flip-flop to copy V_{dd} at its output Q . This pulls $\bar{Q}$ to the ground, thus triggering the reset of the flip-flop when it reaches values below 0.9 V, making Q switch back to 0. The circuit is called monostable because the only stable state of its outputs is $Q = 0$ and $\bar{Q} = V_{dd}$.

On the reset loop, a custom-made 330 G Ω pseudo-resistor and a 475 fF capacitor are added so as not to trigger the reset immediately. Indeed, if the generated impulse is shorter than the peaks from the QRS complex, then V_{in} will still be at a high level after the reset and cause a second impulse. The pseudo-resistor and the capacitor were dimensioned so that the duration of the generated impulse, which depends on the time needed for the partial discharge of the capacitor down to 0.9 V, is at least 60 ms in all corner cases. This corresponds to three times the duration of a typical 20 ms QRS complex for our Sprague Dawley rats and also covers the P-wave as it occurs typically 50 ms before the QRS-Complex. The 330 G Ω pseudo-resistor used in this block is the same as the 720 M Ω one used in the band-pass front-end in Section 4.1, but the widely different polarization makes for a much higher equivalent resistance (see Section 4.6). Thus, with a time constant $RC = 157$ ms, the width of the monostable impulses is approximately 110 ms in the process variation typical case TT, the width goes down to 60 ms in the worst case FS. The aspects of the signal at the output of all aforementioned blocks under nominal conditions are shown in Figure 7.

The pulse counter finally counts the number of impulses over a fixed 2 s duration and compares it with the expected cardiac frequency. The counter is incremented for each rising edge at the output of the monostable flip-flop and is reset every 2 s. A flag is raised

if the observed frequency is too far removed from the expected one ($Flag_{high}$ or $Flag_{low}$ accordingly in Figure 5d).

4.4. Ultra-Low-Power Clock Generation

A time reference is necessary to define a fixed observation window for the pulse counter. The selected reference is the low-power low-frequency relaxation oscillator described in [7]; it is used to regularly reset the pulse counter. The observation duration needs to be as reliable as possible for the measurements to be exploitable. Our oscillator presents a frequency that can vary by up to 17% due to process variations [7], which is problematic in our use case.

The oscillator is, however, tunable, as it presents a switched-capacitor bank controlled by three control signals; this allows for a calibration of the time reference. When driven by a 14.5 M Ω resistor, the typical resulting frequency is 2 Hz. A clock divider is then used to bring the reset frequency down to 0.5 Hz. A Monte-Carlo analysis was conducted with 1000 seeds of process variations to verify the reliability of our time reference. In 97.2% of seeds, a control sequence allowed us to reach a variation from the 2 Hz reference of less than 5%. Table 2 summarizes the proportion of seeds with 5%, 3%, and 1% precision regarding the 2 Hz reference. As it appears, the robustness of our time reference to supply voltage variations is satisfactory; 93.1% of chips would indeed still guarantee staying within 5% of 2 Hz, even for a unrealistically drastic 10% voltage drop.

Table 2. Proportion of seeds in which the oscillator is capable of delivering a reference within 5%, 3%, or 1% of 2 Hz.

Supply Voltage	Proportion of Circuits		
	2 Hz $\pm$ 5%	2 Hz $\pm$ 3%	2 Hz $\pm$ 1%
1.8 V (V_{dd})	97.2%	87.3%	55.4%
1.98 V ($V_{dd}+10\%$)	96.0%	82.3%	35.7%
1.62 V ($V_{dd}-10\%$)	93.1%	78.6%	33.0%
1.89 V ($V_{dd}+5\%$)	96.9%	88.6%	39.4%
1.71 V ($V_{dd}-5\%$)	95.4%	85.9%	38.8%

The tunability thus enables us to considerably reduce the uncertainty of the time reference compared to the initial 17%, which makes the cardiac frequency measurement all the more reliable. As the device is intended to be implantable, the robustness to fluctuations in internal body temperature of the rat has been estimated and is satisfactory, with a typical 1.99 Hz frequency at 35 °C and a 2.03 Hz frequency at 39 °C. The body temperature of a rat should indeed stay in the [35 °C–39 °C] range during its life outside of extreme physical exercise or emotional distress [31].

4.5. Generating the Voltage and Current References

Several voltage and current references are needed throughout the circuit. A 900 mV voltage reference is needed to define the front-end and CMFB common mode. A 1.5 V voltage reference is needed to bias the current sources of the OTA, of its CMFB, and of the PMOS comparator. A 13 pA current reference is needed to bias the squaring circuit.

The 900 mV source consists of simply stacking an even number of diode-connected PMOS transistors between V_{dd} and ground and taking the 900 mV in the middle node of this symmetrical structure. There is a trade-off between the die area and the power consumption as stacking more transistors means a larger area and a smaller consumption, a compromise was found with twelve 20 μ m/20 μ m PMOS and a 700 pA consumption.

The 13 pA and 1.5 V sources are robust low-power autopolarized sources [48] that can be seen, respectively, in Figure 13a and Figure 13b. The output currents/voltages depend on the sizes of the transistors as well as on the value of the bottom resistor. For our 13 pA current source, two current mirrors with very low W/L ratios, M7,8 and M9,10, were added as active loads in order to decrease the output currents $I_{bias\pm}$ down to 13 pA.

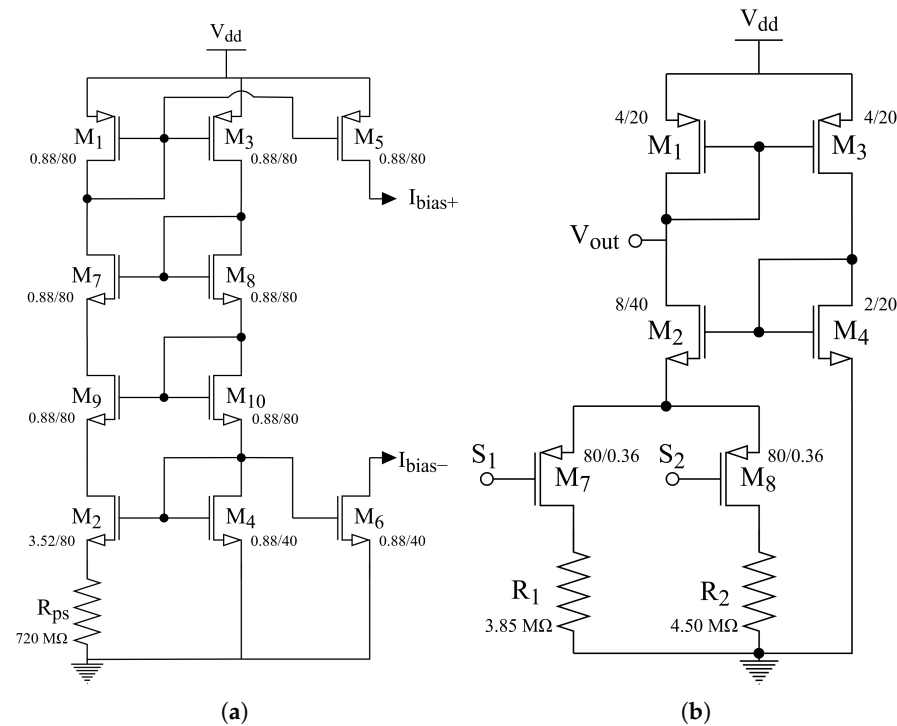


Figure 13. (a) Structure of our 13 pA autopolarized current reference. (b) Structure of our 1.5 V autopolarized voltage reference.

In the case of our 1.5 V voltage source, the output currents are not needed and transistors M5,6 are removed. Moreover, this voltage source is tunable as the single resistance in Figure 13a has been replaced by a switched-resistors bank with two resistors $R_1 = 3.85$ M Ω and $R_2 = 4.50$ M Ω in Figure 13b. Two PMOS are used as switches controlled by the control signals S_1 and S_2 . This tunability allows us to cover all worst cases of process variation when it comes to the gain and bandwidth of our analog front-end. Those front-end characteristics are pivotal as they are responsible for the signal sent to the squaring circuit and therefore condition if the R-peaks will be easily identifiable. Both the gain and the bandwidth depend on the bias current $I_{B_OTA} = 2.1$ nA of the OTA and thus on our 1.5 V reference, which is responsible for the biasing of the OTA. While the front-end is designed to work under nominal conditions with a bias voltage of 1.5 V, it should be noted that the critical FS and SF worst cases indeed show a typical correct operating for bias voltages of, respectively, 1.47 V and 1.55 V.

R_1 covers the cases TT, FF, SS and SF. R_2 covers the cases TT, FF, SS and FS. PMOS transistors M7-and-8 are used as switches to select either R_1 or R_2 ; they were sized with a very large W/L ratio so that their “on resistance” stays small compared to the resistors.

The performance of the voltage and current sources are summarized in Tables 3 and 4. Robustness to process variations is satisfactory as they can only lead at worst to a 6.0% drift in the current reference (case FS in Table 3) and a 1.8% drift in the voltage reference (case SF with resistor R_1 selected in Table 4). Large $\pm 10\%$ supply voltage fluctuations lead to 12.5% variations in the current reference. When it comes to the voltage reference, the difference between the supply voltage and the typical reference stays roughly the same

even with $\pm 10\%$ supply voltage fluctuations (at 295 mV with R_1 selected, and 270 mV with R_2 selected). Thus, the V_{GS} of the PMOS bias current source in the OTA should remain the same and I_{B_OTA} should remain unaffected by such fluctuations.

Table 3. PMOS output current of the 13 pA autopolarized source against supply voltage fluctuations from -10% to $+10\%$ and process variation worst cases. Nominal supply voltage is highlighted.

Supply Voltage	TT	FF	SS	SF	FS
1.62 V ($V_{dd}-10\%$)	11.60 pA	12.38 pA	10.93 pA	10.98 pA	12.46 pA
1.71 V ($V_{dd}-5\%$)	12.43 pA	13.21 pA	11.74 pA	11.70 pA	13.27 pA
1.8 V (V_{dd})	13.25 pA	13.72 pA	12.55 pA	12.53 pA	14.10 pA
1.89 V ($V_{dd}+5\%$)	14.09 pA	14.87 pA	13.39 pA	13.35 pA	14.93 pA
1.98 V ($V_{dd}+10\%$)	14.92 pA	15.73 pA	14.23 pA	14.19 pA	15.77 pA

Table 4. Output voltage of the 1.5 V autopolarized source against supply voltage fluctuations from -10% to $+10\%$ and process variation worst cases in both possible resistor configurations. Nominal supply voltage is highlighted.

V_{dd}	TT		FF		SS		SF		FS	
	w/ R_1	w/ R_2	w/ R_1	w/ R_2	w/ R_1	w/ R_2	w/ R_1	w/ R_2	w/ R_1	w/ R_2
1.62 V	1.326 V	1.352 V	1.341 V	1.369 V	1.309 V	1.333 V	1.319 V	1.342 V	1.343 V	1.371 V
1.71 V	1.415 V	1.441 V	1.431 V	1.459 V	1.399 V	1.423 V	1.400 V	1.431 V	1.433 V	1.461 V
1.8 V (V_{dd})	1.505 V	1.531 V	1.520 V	1.549 V	1.488 V	1.512 V	1.478 V	1.491 V	1.522 V	1.550 V
1.89 V	1.595 V	1.620 V	1.610 V	1.638 V	1.578 V	1.602 V	1.577 V	1.610 V	1.612 V	1.640 V
1.98 V	1.684 V	1.710 V	1.699 V	1.728 V	1.677 V	1.691 V	1.675 V	1.700 V	1.702 V	1.729 V

Finally, fluctuations in a rat's internal body temperature between $35\text{ }^{\circ}\text{C}$ and $39\text{ }^{\circ}\text{C}$ should only have a very minor impact on references with the output values only shifting by less than 0.5% between the nominal $37.3\text{ }^{\circ}\text{C}$ and those temperatures.

4.6. Pseudo-Resistors

Two different pseudo-resistors were designed and used in the circuit:

- A $400\text{ M}\Omega$ 6-PMOS pseudo-resistor used in the front-end high-pass;
- A $720\text{ M}\Omega$ 6-PMOS pseudo-resistor used in the front-end low-pass, the 13 pA reference, and in the monostable flip-flop.

Those equivalent resistance values were estimated for an applied voltage difference around 0.9 V .

Their structure is shown in Figure 14. Both outer PMOS transistors are diode-connected to induce a voltage drop on both sides. The rest of the structure consists of two source-bulk connected pairs in series [40]. The main advantage of this structure is that our pseudo-resistors do not need any biasing circuits like those presented in [49] because the gate voltage of the four centre-most transistors is controlled by the drain voltage of the opposite outer transistor. This is particularly interesting as our biasing references are our most power-hungry components. Resistance values up to a few teraohms can be obtained with such architectures. If smaller pseudo-resistances are needed, 4 PMOS architectures can also be implemented with both outer transistors removed. After parametric dimensioning, the sizes of the transistors making up the pseudo-resistors, shown in Table 5, were chosen. For a given length, wider transistors let more current flow and therefore lead to smaller resistance values, as plotted in Figure 15a.

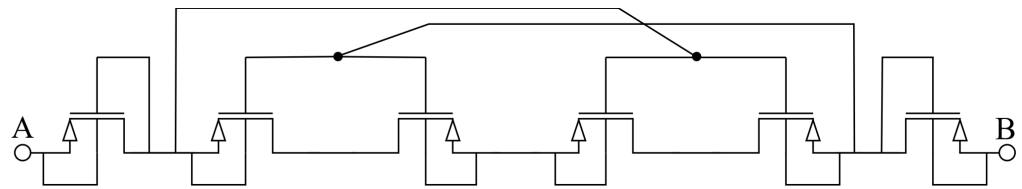


Figure 14. Structure of the designed 6 PMOS pseudo-resistors.

Table 5. Sizing of all designed pseudo-resistors.

Equivalent Resistance R_{eq}	Number of PMOS	PMOS Width (μm)	PMOS Length (μm)
400 M Ω	6	3.5	10
720 M Ω	6	1.85	10

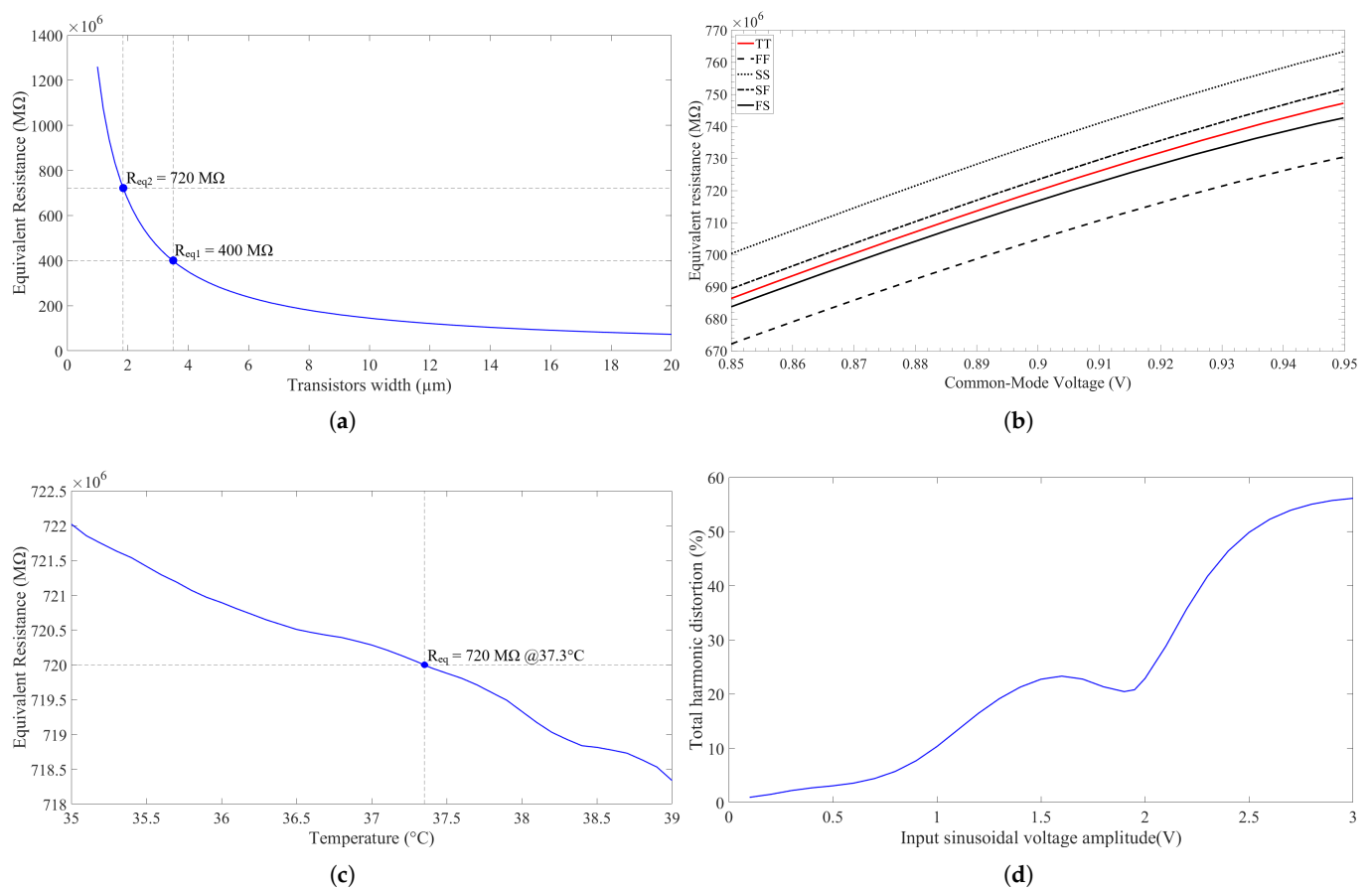


Figure 15. (a) Equivalent resistance for a 0.9 V polarization depending on the width W of used transistors for a given $L = 10 \mu\text{m}$. (b) Comparison of the equivalent resistance for a [0.85–0.95 V] voltage sweep at both terminals of a 720 M Ω pseudo-resistor in all process variation worst cases. (c) Equivalent resistance of a 720 M Ω pseudo-resistor for a 0.9 V polarization in the range of admissible internal temperature in rats. (d) Total harmonic distortion of the designed 720 M Ω pseudo-resistor for input sinusoidal voltage in [0–3 V].

These pseudo-resistors should be robust to common-mode fluctuations and PVT variations. A [0.85–0.95 V] sweep was conducted at the terminals of our pseudo-resistors; the results of the sweep in all four worst cases for an equivalent resistance of 720 M Ω is shown in Figure 15b. As it appears, even extreme 5% common-mode fluctuations from 900 mV to 850 mV (or 950 mV) only decrease (respectively increase) the equivalent resistance at worst by 5%; this remains true for other equivalent resistances.

Process variations (see Table 6) only lead at worst to a 2.2% variation in the equivalent resistance for a given 0.9 V polarization. While a variation in the value of our pseudo-resistors may slightly shift the cutoff frequency of our band-pass filter or vary the duration of the monostables's impulse by a 2 to 3% margin, the robustness of the pseudo-resistors is satisfying enough and will not prevent any element of the circuit from working as intended as long as the common-mode voltage remains stable around 0.9 V. Robustness to temperature variations was also assessed via DC Simulation inside the internal [35 °C–39 °C] temperature range of rats; the effect of the temperature on the equivalent resistance for a 0.9 V polarization is shown in Figure 15c, as it appears the robustness to internal body temperature fluctuations is satisfactory, with a 0.28% drift reached at 35 °C. The total harmonic distortion (THD) of our pseudo-resistors was also investigated and plotted against the input sinusoidal voltage amplitude in Figure 15d. While it remains low for limited amplitudes with a THD remaining below 1% (−40 dB) for amplitudes below 100 mV_{P-P}, it can reach relatively high values for a 1.8V full swing (21.35% or −13.4 dB @1.8 V_{P-P}) or higher amplitudes.

Table 6. Value of the designed pseudo-resistors in all process variation worst cases, with a 0.9 V applied voltage.

Case	R_{eq1} (M Ω)	R_{eq2} (M Ω)
TT	400	720
FF	392	705
SS	409	735
FS	402	723
SF	398	717
Max deviation from TT	2.2%	2.1%

Finally, it should be highlighted that the voltage applied at the terminals of the pseudo-resistors has a very strong impact on the resulting equivalent resistance. While the equivalent resistance is relatively stable around the common-mode voltage 0.9 V (see Figure 15b), very large resistance values above 100 G Ω are obtained for voltage differences above 1.5 V. The evolution of the equivalent resistance of our pseudo-resistor presenting 720 M Ω at 0.9 V is plotted in Figure 16.

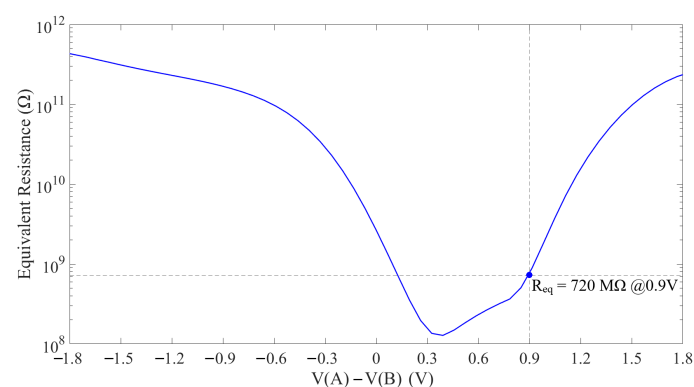


Figure 16. Evolution of the equivalent pseudo-resistance of our 720 M Ω pseudo-resistor depending on the applied voltage difference at its terminals.

5. Results and Discussion

5.1. Post-Layout Simulation Results

The layout view of the whole ECG circuit is presented in Figure 17; it spans over an area of 450 μ m by 270 μ m. Typical resulting waveforms are shown in Figure 7. Those waveforms

correspond to internal circuit nodes; it should therefore be noted that additional output buffers would be required for them to be observed on a physical chip implementation.

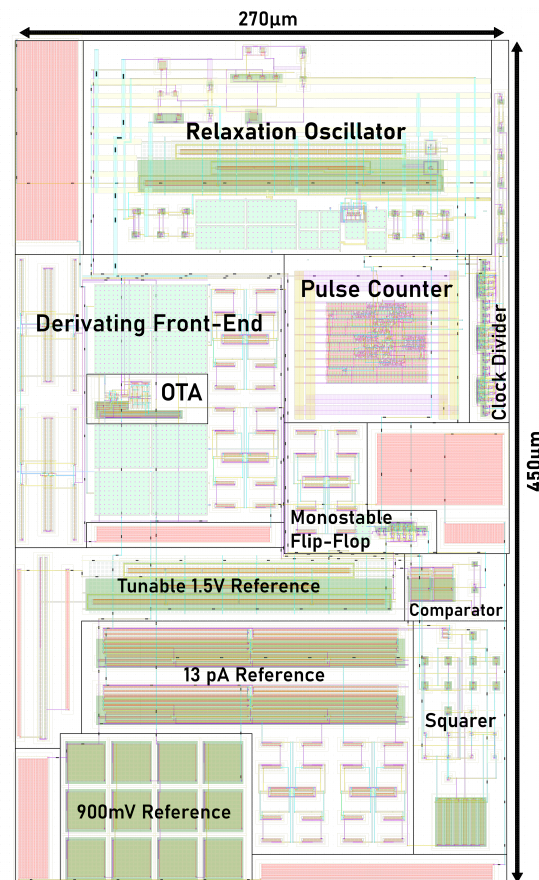


Figure 17. Layout view of the ECG circuit.

To estimate the power consumption, the average current of each block was calculated and multiplied by the supply voltage $V_{dd} = 1.8$ V. The total power consumption of the circuit is 28.5 nW. The analog processing chain has a power consumption of 5.9 nW, of which 4.4 nW are consumed in the all-in-one front-end, 160 pW in the squaring circuit, 230 pW in the comparator, and 1.2 nW in the monostable flip-flop. The three different voltage/current references consume a total of 7.0 nW, while the relaxation oscillator providing the time reference has a power consumption of 14.7 nW. The pulse counter finally accounts for 900 pW of the total.

Our circuit was tested at the layout level on our own rat recordings as well as on the healthy sinus rhythm ECG database of the PhysioNet/-Computing in Cardiology Challenge 2020 [16] and on the MIT-BIH arrhythmia database [50] that were artificially altered to match murine intracardiac physiology. All human signals were sped up by a factor 5 and their amplitude was increased by a factor 5 to fit rat-like intracardiac physiology.

In our own recordings, the detection rate is 100%. On the normal sinus rhythm electrocardiograms from [16], the results are also very satisfying, with 99.88% sensitivity and 99.97% positive predictivity, accounting for 99.85% accuracy.

The results on all 48 30-min tapings from MIT-BIH are summarized in Table 7; records with a perfect accuracy are highlighted in green, and those with an accuracy below 95% in red. The global accuracy on those ECGs is 98.57%, with 99.14% sensitivity and 99.43% positive predictivity. While low-amplitude ECGs (e.g., record 222) caused our system to

miss some heart beats and noisy recordings (e.g., record 108) tended to cause false positives, this demonstrates the efficiency of our circuit for detecting the heart rate of small mammals.

Table 7. Results of heart beat detection on the MIT-BIH arrhythmia database [50], artificially altered to match murine cardiophysiology. Records with a perfect accuracy are highlighted in green. Records with an accuracy below 95% are highlighted in red.

#	Se	PP	Acc	#	Se	PP	Acc
100	100	99.96	99.96	201	95.87	100	95.87
101	100	98.78	98.78	202	98.92	100	98.92
102	99.95	100	99.95	203	96.21	97.19	93.60
103	100	99.95	99.95	205	99.66	100	99.66
104	98.20	97.81	96.09	207	97.15	95.81	93.19
105	99.81	97.64	97.46	208	99.29	99.53	98.82
106	98.96	99.90	98.87	209	100	99.60	99.60
107	99.95	99.81	99.77	210	96.74	99.61	96.38
108	94.09	96.53	91.50	212	100	99.67	99.67
109	99.92	99.65	99.57	213	100	99.75	99.75
111	99.81	100	99.81	214	99.74	99.69	99.43
112	100	99.96	99.96	215	100	99.56	99.56
113	100	100	100	217	99.82	99.55	99.37
114	99.79	99.68	99.47	219	100	99.95	99.95
115	100	100	100	220	100	100	100
116	98.93	99.67	98.60	221	99.42	99.92	99.34
117	100	100	100	222	93.84	100	93.84
118	100	99.57	99.57	223	99.92	99.89	99.81
119	100	100	100	228	94.74	98.03	92.97
121	98.18	99.89	98.07	230	100	99.21	99.21
122	100	100	100	231	99.87	100	99.87
123	100	99.80	99.80	232	99.61	100	99.61
124	100	99.82	99.82	233	99.94	99.71	99.64
200	99.92	98.78	98.71	234	99.86	100	99.86
Total: Sensitivity = 99.14% Positive Predictability = 99.43% Accuracy = 98.57%							

5.2. Comparison to the State of the Art

The evaluation of this circuit's relevancy was done through comparison with other integrated cardiac frequency detection modules found in the literature. Table 8 summarizes key performance indicators of this circuit and seven other ones. Particular attention is given to power consumption and circuit area as these are the two main factors when it comes to implantability of a battery-powered system. Other parameters include the CMOS process, the supply voltage, the detection method, and the QRS-detection accuracy.

A first observation makes clear that digital computation-heavy methods present much larger sizes and consumptions than analog circuits. Neural Network-based solutions [10] show themselves as the most power- and area-hungry solutions, with consumptions in the hundreds of μW and areas over 1 mm^2 , even if implemented with advanced 55 nm technology and relatively low 1.2 V supply voltage. Less consuming digital methods exist, such as sparse Hilbert transforms [8] or wavelet transform singularity detection algorithms [9]; they present interesting advantages such as a better noise immunity that contributes to making it the most accurate detection methods, but they still cannot compare to their analog counterparts when it comes to area and especially consumption.

Table 8. Comparison with the state of the art.

	Güngör, 2019 [19]	Karimlou, 2024 [12]	Silva, 2021 [11]	Morshedlou, 2021 [51]	Xie, 2023 [10]	Zhang, 2026 [8]	Chen, 2022 [9]	This Work
Process	65 nm	180 nm	180 nm	130 nm	55 nm	55 nm	180 nm	180 nm
VDD	1 V	0.8 V	1.8 V	1.2 V	1.2 V	0.75 V	1.8 V	1.8 V
Circuit Area	0.093 mm ²	0.026 mm ²	0.011 mm ²	0.097 mm ²	1.95 mm ²	0.044 mm ²	0.83 mm ²	0.122 mm ²
Power Cons.	0.5 nW [★]	39.8 nW	0.79 µW	31.5 nW	192 µW	4.8 µW	4.7 µW	28.5 nW
Algorithm	P-T based	Time-	Energy-	Energy-	Neural Network	Hilbert	Wavelet	P-T based
Functions	QRS- Detection	Derivative QRS- Detection	Derivative QRS- Detection	Derivative QRS- Detection	QRS- Detection & Freq. Detection	Transform QRS- Detection	Transform QRS- Detection	QRS- Detection & Freq. Detection
Accuracy (MIT-BIH)	97.91%	98.51%	97.52%	98.53%	98.70%	98.89%	99.16%	98.57%
Domain	Analog (Sim.)	Analog (Sim.)	Analog (Meas.)	Analog (Sim.)	Digital (Meas.)	Digital (Meas.)	Digital (Meas.)	Mixed (Sim.)

[★]: This power consumption does not include the consumption of the voltage and current references (OTA biases, comparison thresholds, etc.). P-T: Pan-Tompkins.

Derivative-based analog solutions [11,12,51] are the most promising ones regarding the size of the circuit as they require less computation and thus have less components in their processing chain. Silva et al. [11] even reached a really low 0.011 mm² total area despite using a relatively large 180 nm technology. The most similar approach to ours presented in this table is Güngör and Töreyn's fully analog Pan-Tompkins-based circuit [19], it manages to reach an extremely low power consumption by implementing 10 pA-biased OTAs operated in the deep sub-threshold region. Their low power consumption can also be explained by the use of an advanced 65 nm CMOS process and a low 1 V supply voltage. While these results are impressive, it should be pointed out that all of their bias voltages (OTA biases, comparison thresholds, etc.) are provided by external sources, the consumptions of which are not included in their total. The circuit presented in this article proves its worth by achieving a very low 28.5 nW consumption, while maintaining a satisfying 0.122 mm² area despite using a relatively large 180 nm CMOS process and a 1.8 V supply voltage, and including a digital post-processing step. These performances do not come at the price of a lack of robustness as it shows a reliable 99.88% sensitivity and 99.97% positive predictivity on healthy sinus rhythm murine ECGs, as well as a 99.14% sensitivity and 99.43% positive predictivity on the MIT-BIH Arrhythmia database artificially altered to match murine physiology. This all makes it suitable for usage on small mammals such as rats in the context of the study of pulmonary arterial hypertension, with its low power consumption allowing long-term hospital experiments to take place without needing to change the battery. A limitation to those results would be a conscious and unrestrained animal causing medium-frequency high-amplitude motion artifacts. While most artifacts below 10 Hz (caused for example by respiration or small head movements) and above 60 Hz (due to chewing or fast muscle activation) [52] are efficiently filtered, medium-frequency motion artifacts could cause large voltage spikes, driving the front-end amplifier into temporary saturation. This would lead to missed heartbeats during the saturation, surrounded by two false positives at the beginning and the end of the saturation. The recovery time then corresponds to one cycle of the monostable flip-flop.

Finally, it should also be noted that this circuit, as well as [12,19,51], has been simulated post-layout after parasitic extraction and has not yet been manufactured and measured. Manufacturing the circuit would come with an increased power consumption due to the I/O pads and packaging effects. Tape-out yield is also left unverified. Slightly worse results in terms of power consumption and accuracy should thus be expected. Benchtop validation would include manufacturing of a physical chip containing the whole ECG circuit as well

as every sub-block singled out with their own voltage supply to enable every necessary unit test.

6. Conclusions

This work describes a new ultra-low-power 28.5 nW cardiac frequency detection circuit suited to rat-like cardiophysiology (heart rates up to 600 bpm and baseline wandering up to 1.7 Hz). It comprises a derivating analog front-end, an analog squarer, an analog reshaping circuit, and a digital pulse counter. Low power consumption is achieved by operating the vast majority of transistors at sub-threshold and by modifying the Pan–Tompkins algorithm to remove power- and area-hungry elements such as the moving average filter and the adaptive thresholding, while also combining the filtering and derivative stages. Post-layout simulations have demonstrated its efficiency and robustness on intracardiac murine ECGs and on a database of human ECGs, that were sped up and amplified to match rat-like intracardiac signals.

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Data Availability Statement: The circuit was validated on two publicly available electrocardiograms databases: the MIT-BIH Arrhythmia Database available at <https://www.physionet.org/content/mitdb/1.0.0/> and the PhysioNet/Computing in Cardiology Challenge 2020 Database available at <https://physionet.org/content/challenge-2020/1.0.2/>. Both links last accessed on 15 September 2026.

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Abbreviations

The following abbreviations are used in this manuscript:

Acc	Accuracy
ADC	Analog–Digital Converter
bpm	Beat Per Minute
CM	Common-Mode
CMFB	Common-Mode Feedback
CMRR	Common-Mode Rejection Rate
CMOS	Complementary Metal–Oxide Semiconductor
ECG	Electrocardiogram
iECG	Intracardiac Electrocardiogram
INSERM	French National Institute of Health and Medical Research
MIT-BIH	Massachusetts Institute of Technology—Beth Israel Hospital
OTA	Operational Transconductance Amplifier
PAH	Pulmonary Arterial Hypertension

PP	Positive Predictivity
P-T	Pan–Tompkins
PVT	Process, Voltage, and Temperature
Se	Sensitivity
THD	Total Harmonic Distortion
ULP	Ultra-Low Power

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