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Adaptive Hybrid Switched-Capacitor Cell Balancing for 4-Cell Li-Ion Battery Pack with a Study of Pulse-Frequency Modulation Control

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Abstract

Battery cell balancing is crucial in series-connected lithium-ion packs to maximize usable capacity, ensure safe operation, and prolong cycle life. This paper presents a comprehensive study and a novel adaptive duty-cycled hybrid balancing system that combines passive bleed resistors and an active switched-capacitor (SC) balancer, specifically designed for a 4-cell series-connected battery pack. This work also explored open circuit voltage (OCV)-driven adaptive pulse-frequency modulation (PFM) active balancing to achieve higher efficiency and better balancing speed based on different system requirements. Finally, this paper compares passive, active (SC-based), and adaptive duty-cycled hybrid balancing strategies in detail, including theoretical modeling of energy transfer and efficiency for each method. Simulation showed that the adaptive hybrid balancer speeds state-of-charge (SoC) equalization by 16.24% compared to active-only balancing while maintaining an efficiency of 97.71% with minimal thermal stress. The simulation result also showed that adaptive active balancing was able to achieve a high efficiency of 99.86% and provided an additional design degree of freedom for different applications. The results indicate that the adaptive hybrid balancer offered an excellent trade-off between balancing speed, efficiency, and implementation simplicity for 4-cell Li-ion packs, making it highly suitable for applications such as high-voltage portable chargers.

Keywords: battery management systems (BMS); cell balancing; switched-capacitor; passive balancing; hybrid balancing; lithium-ion; portable charger; pulse-frequency modulation

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1. Introduction

Series-connected lithium-ion battery packs require cell balancing to prevent capacity degradation due to cell mismatches. Even a small state-of-charge (SoC) or voltage imbalance can limit the pack's usable capacity by the weakest cell and accelerate cell aging. Therefore, an effective balancing system is crucial for maintaining optimal battery performance and safety. In energy storage applications ranging from electric vehicles to portable electronics, two broad balancing approaches exist: passive and active balancing. Passive balancing uses resistors to bleed excess energy from higher-charge cells as heat, offering simplicity and low cost, but wasting energy and potentially causing thermal issues [1]. Such dissipative methods are commonly employed in cost-sensitive or scenarios where the energy loss is acceptable [2]. In contrast, active balancing methods redistribute energy between cells. For example, by using capacitors or inductive converters, so that surplus energy from

higher-voltage cells is transferred to lower-voltage cells instead of being dissipated [3]. Active cell balancing thus can achieve higher efficiency and preserve more of the pack's energy, at the expense of increased circuit complexity and cost.

Switched-capacitor (SC) balancers have attracted attention for their compactness and low component count among active balancing techniques. An SC balancer typically uses one or more capacitors that are periodically switched across pairs of cells to shuttle charge. This approach avoids bulky inductors and can be integrated with small solid-state switches, which is ideal for space-constrained applications. However, conventional SC balancing suffers from slow convergence when many cells are in series, as the charge transfer between distant cells must propagate cell-by-cell over many cycles [4]. Kim et al. noted that while SC circuits are promising for their low cost and size, their balancing speed decreases as the string length increases [4]. Various improved SC topologies have been proposed to alleviate this issue, such as chain structures as shown in Figure 1, which provide additional charge transfer paths among non-adjacent cells to accelerate the balancing of outer cells [5,6]. Still, these enhancements involve more capacitors or switching elements, which can be considered an auxiliary improvement that can be implemented later in the system design phase.

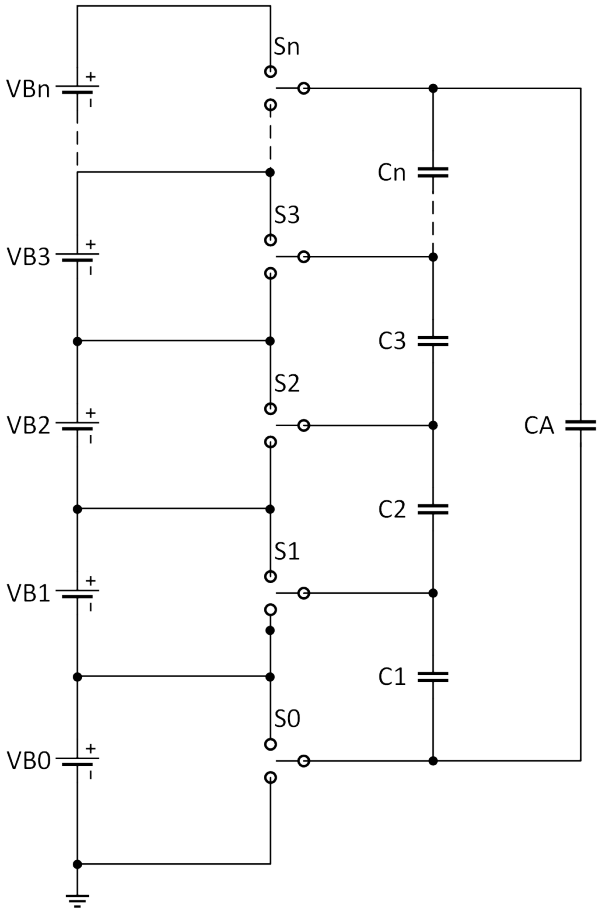


Figure 1. Switched-capacitor balancer with chained structure.

For applications such as a 4-series-cell portable charger (approximately 4 × 3.7 V lithium-ion cells, as found in high-capacity portable chargers), the balancing system must be compact and low-cost, yet effective at equalizing cells during charge/discharge cycles and storage. Many commercial portable 4-cell packs forego active balancing due to cost, or use only simple passive bleeding at end-of-charge [7–9]. This leads to wasted energy (reduced charge delivered to the user) and potential cell stress from thermal runaway if imbalances are large and unchecked. A solution that can be integrated into such portable

devices to improve energy utilization and longevity without significantly increasing cost or size is highly preferable. Switched-capacitor balancing is a compelling choice here because it omits heavy magnetics, can be integrated into a single chip, and can provide sufficient balancing currents for moderate-capacity cells (on the order of a few hundred mA) with minimal overhead. A comparison of different types of cell balancing methods is presented in Table 1 for a clearer picture. By focusing on this specific context, this paper presents a balancing strategy that leverages the strengths of SC-based equalization while addressing its limitations through hybridization with passive elements.

Table 1. Typical balancing—current ranges for 4-series-cell packs (∼3.4 Ah).

Balancing Type	Current Range	Reference Sources	Notes/Implications
Passive resistor (bleed)	30–100 mA	DALY 4-S BMS DS [10]; DIY-Solar teardown [11]	Simple, low cost; balancing time often in hours.
SC active (single-cap)	0.2–0.5 A peak (50–150 mA avg)	Endless-Sphere tests [12]; MathWorks example [13]	No magnetics; >90% efficient for ≤4 cells.
SC active (chain/DT)	0.5–1 A peak	Kim et al. [4]; Ye et al. [6]	Faster, but more switches and capacitors.
Inductor/flyback	1–10 A	ADI LTC3300 DS [14]; MPS white paper [15]	Fastest; requires magnetic, costly for small packs.

This study consolidates and extends prior work on passive, active, and hybrid cell balancing strategies for optimal battery performance [16]. A novel hybrid balancing architecture that leverages the open circuit voltage (OCV) of each cell to determine when to switch between active and passive balancing modes was proposed. The architecture integrates a SC-based active balancer with resistive bleeding, thereby combining the high energy efficiency of active charge transfer with the simplicity and reliability of passive bleed resistors.

The hybrid scheme involved an intermittent control strategy: passive balancing intervals are inserted between periods of SC-based active balancing. The duration of each passive interval is adaptively adjusted based on real-time cell voltage conditions to optimize thermal performance and minimize energy loss. Compared to purely passive schemes, the hybrid approach reduces dissipation during large imbalances by engaging active transfer, while accelerating final equalization through resistive bleeding when voltage differences become small.

Additionally, building on our earlier adaptive pulse-width modulation (PWM) work [17], this paper also investigates an adaptive pulse-frequency modulation (PFM) strategy within the SC-based active balancing framework. The system dynamically adjusts the SC switching frequency according to the instantaneous cell voltage mismatch. The largest ΔOCV between each cell OCV to the average voltage of battery pack is used to determine the switching frequency, based on the equation: $f(t) = f_{\min}\,(1 + k_f\,\Delta V_{\max})$. This adaptive-PFM approach ensures efficient operation throughout the entire balancing cycle and provides another perspective for system design to be tailored to different applications.

The contributions of this work are summarized as follows:

- This work presents a unified analysis of passive, active (switched-capacitor-based), and hybrid cell balancing methods applied to a four-cell Li-ion pack.
- This work introduces a novel SC-based hybrid balancing architecture that combines active charge redistribution with passive resistive bleeding. The on-chip digital controller autonomously switches between active and passive modes based on cell OCV thresholds to optimize both speed and efficiency.
- This work studied an adaptive PFM scheme for the SC-based active balancer. The switching frequency is varied between $f_{\max}$ and $f_{\min}$ according to the instantaneous

voltage imbalance, achieving high charge-transfer currents during large imbalances and minimizing switching losses near equilibrium.

- This work presents comprehensive post-layout simulations, with 3.4 Ah battery cells (Panasonic MH12210) modeled by capacitors of 3308 F, comparing passive-only, active-only, hybrid, and adaptive-PFM strategies under identical initial conditions. Based on the simulation results of this work, the hybrid scheme balances in 7.48 h at 97.71% efficiency, while the adaptive-PFM scheme completes in 8.06 h at 99.86% efficiency, outperforming fixed-frequency extremes.
- This work implements the proposed balancers in STMicroelectronics' 180 nm BCD technology and verifies functionality via Cadence Virtuoso post-layout simulations. The chip achieves autonomous mode switching, redistributes over 97.71% of imbalance energy, and occupies a 1730 µm × 1452 µm footprint.

The remainder of this paper is organized as follows: Section 2 provides background on cell balancing methods and reviews related works, particularly SC-based equalizers and hybrid designs. Section 3 provides a detailed description of the proposed hybrid balancing system and adaptive-PFM active balancing switching control, including its circuit topology, control algorithm, and theoretical analysis of balancing dynamics. Section 4 presents post-layout simulation results, along with comparisons between different methods and with prior literature. Finally, Section 5 concludes the paper with key findings and suggestions for future work.

2. Background and Related Work

In this section, the operating principles of passive and active cell balancing will be briefly described, and relevant prior works that have influenced the development of the hybrid approach will be discussed.

2.1. Passive vs. Active Cell Balancing Techniques

In passive balancing, each cell in the series stack is typically shunted by a resistor, often controlled by a switch or transistor, as shown in Figure 2a. When a cell exceeds the pack's minimum cell voltage (or SoC) by a certain threshold, the resistor is activated to bleed off the excess charge until the cell falls in line with the others. This approach equalizes cells by wasting the energy difference as heat. Its main advantages are simplicity and low cost: the circuit can be as basic as a resistor and a transistor per cell, managed by the battery management system (BMS) controller. Passive balancing is inherently safe and requires minimal control effort. However, the apparent downside is energy inefficiency—any corrected imbalance directly translates to lost energy. In high-energy packs, this loss not only reduces overall efficiency but can also cause significant heating in the resistors, which require thermal management. Due to these issues, passive schemes are acceptable primarily for packs that are lightly used or where slight energy loss is tolerable (e.g., small consumer electronics or during the final stage of charging) [8]. In our target 4-cell power bank scenario, a passive balancer would dissipate energy from a whole cell as heat, reducing the charge available to the user and potentially warming the device noticeably.

Active balancing techniques avoided this waste by moving energy from one cell to another. There are numerous active balancing topologies in the literature [18]. Broadly, they can be categorized by the energy transfer element: some use capacitors, others use inductors or transformers (flyback converters, multi-winding transformers, etc.), and some use combinations of both. Inductor-based balancers (such as buck–boost converters or Cuk converters between cells or between cells and a central bus) can transfer energy efficiently and quickly [19]. Still, they usually require magnetic components that are larger and more expensive, which can be a drawback for compact devices. SC-based balancers use one or

more capacitors that are periodically connected across cells to share charge, as illustrated in Figure 2b. They have the advantage of no inductors (hence lower profile and potentially integrated design) and relatively simple control, often just a fixed-frequency clock to cycle the capacitor connections.

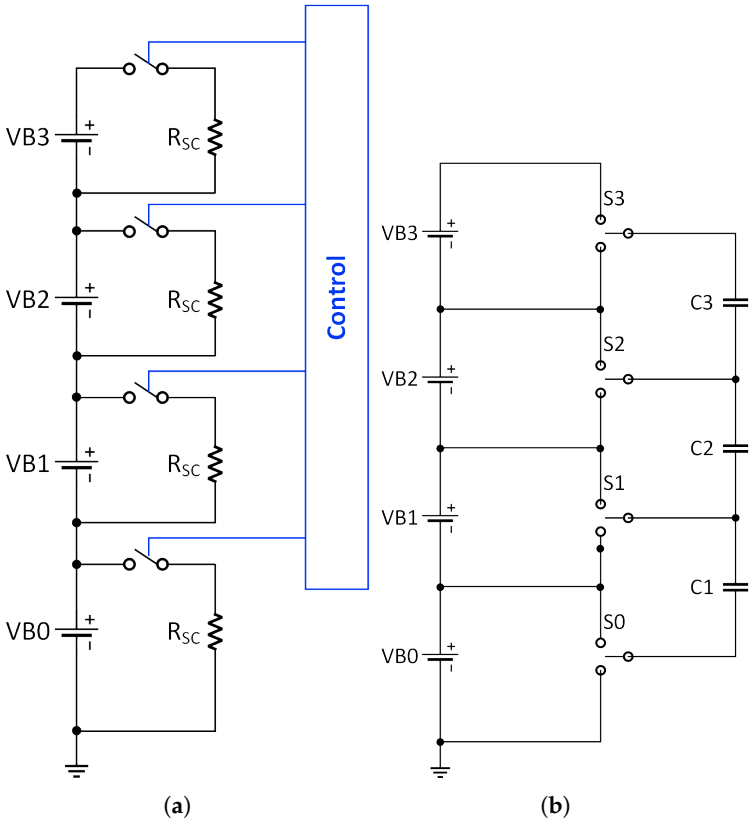


Figure 2. (**a**) Conventional switched-resistor passive converter. (**b**) Conventional switched-capacitor active converter.

A basic SC-based balancer operates by connecting a flying capacitor across adjacent cell pairs in a repeated sequence. In one switching state, the capacitor charges from a higher-voltage (higher SoC) cell; in the next state, it is connected to a lower-voltage (lower SoC) cell to discharge into it. By cycling quickly, charge is redistributed until the cell voltages equalize. This adjacent cell-to-cell transfer eventually equalizes the whole string. The SC approach is easy to implement and scales to any number of cells (just by switching the capacitor sequentially along the string). However, its balancing speed can be modest, especially for longer strings, because the charge must hop through intermediate cells. As noted in the literature, the balancing speed of conventional SC methods tends to deteriorate as the number of series-connected cells increases [4]. Researchers have sought to improve upon this limitation by modifying the circuit topology. For instance, Kim et al. introduced a chain structure of SCs as shown earlier in Figure 1, effectively creating additional capacitive paths among non-neighboring cells to accelerate the equalization of cells positioned farther apart in the stack [4]. Their proposed architecture demonstrated significantly faster balancing performance on a long lithium-ion string compared to the classical pairwise SC configuration. Other variants include double-tier and multi-tier SC designs, where multiple capacitors operate in a layered manner to reduce the required number of switch cycles and enhance balancing speed [6]. An early example of this approach is the double-tier SC technique proposed by Baughman and Ferdowsi, which employed two levels of capacitors to enable charge transfer across two adjacent cell pairs simultaneously, thereby shortening the overall balancing time in large battery packs [5].

Another common strategy is to combine different balancing methods to capitalize on their strengths. For instance, some works merge switched-capacitor networks with converter-based circuits. Liu et al. proposed an integrated balancer that combines a coupled buck–boost converter with a parallel-connected SC network, enabling flexible "any cell-to-any cell" charge redistribution [20]. Their experiments on 4–6 cell modules demonstrated that this combined topology achieved the highest balancing speed and energy efficiency among several configurations tested [20]. Similarly, Jain et al. explored multi-layer balancing architectures that incorporate both inductive and capacitive elements to enable multiple energy transfer pathways and support higher equalization currents [21]. While these hybrid hardware topologies exhibit excellent performance, they often involve increased complexity due to a larger number of components and control loops.

In summary, purely passive balancing offers simplicity but suffers from low energy efficiency. Purely active balancing, whether based on capacitors or inductors, can improve efficiency; however, SC approaches may be limited by slower balancing speed, while inductor-based solutions often involve greater complexity and bulk. Combined or hybrid approaches can enhance overall performance but typically require additional hardware. In the context of a 4-cell portable charger, where constraints on size and cost are critical, the use of large inductors or complex multi-converter topologies is impractical. At the same time, faster and more efficient balancing is desired than what passive or basic SC methods alone can provide. These considerations motivate the development of a *hybrid SC–passive balancing strategy with adaptive control*, as proposed in this work.

2.2. Prior Hybrid Balancing Approaches

The concept of hybrid balancing (using both active and passive elements) is not entirely new. One straightforward hybrid strategy implemented in some BMS is to use active balancing during certain periods (for example, during charging when there is surplus energy to redistribute) and then rely on passive bleeding at other times (such as at the top-of-charge to fine-tune each cell to exactly equal voltage). The architecture of the hybrid balancing is as shown in Figure 3 [16]. This approach can balance cells 41.5% faster than an active-only strategy with simulated results. However, this is done in a fixed, sequential manner and not adaptively duty-cycled, so it could generate more heat and thermal runaway issues [16].

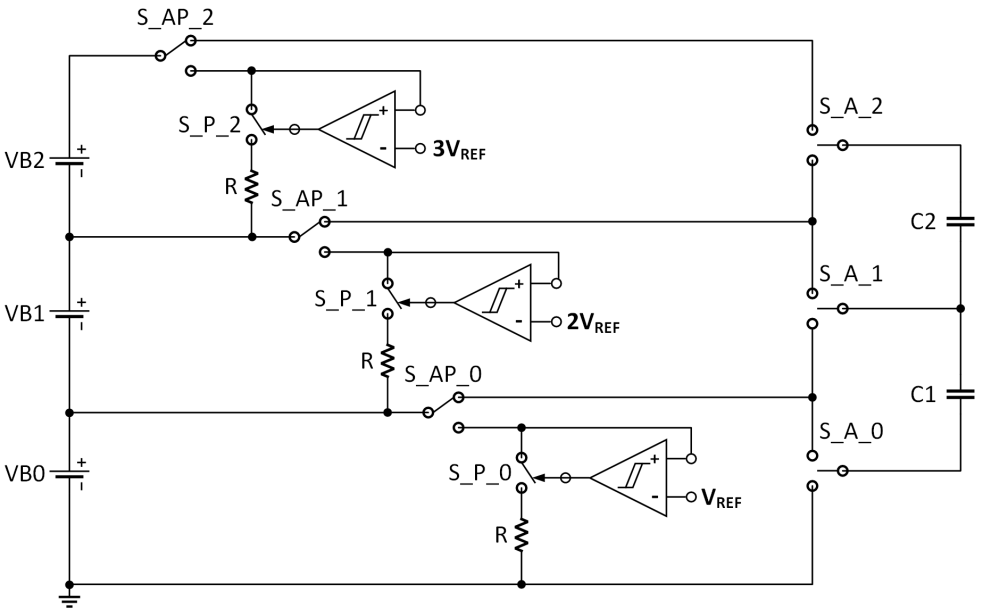


Figure 3. Hybrid balancer system block diagram.

Other studies proposed hybrid approaches that combine multiple techniques or novel control algorithms to improve speed and efficiency. For instance, Guo et al. [22] use a flyback converter-based hybrid method (active + passive) to accelerate balancing in EV packs. Kocyigit et al. [23] introduce a two-level hybrid scheme (module-level switched-capacitor active balancing combined with cell-level passive shunting) for electric vehicles. On the control side, Evangeline et al. [24] explore intelligent algorithms (quantum PSO) to dynamically optimize a mixed SC + transformer balancer dynamically, achieving 99.24% efficiency. Khan et al. [25] likewise propose a duty-cycle-based hybrid active method for EV packs that significantly cuts balancing time. There are also works with hybrid balancing proposed for LEO satellites, Zhu et al. [26] demonstrate a switch–matrix hybrid that uses passive shunts during charge and an active flyback path during discharge to balance reliability and efficiency in a DC-bus architecture.

2.3. Adaptive Pulse-Frequency Modulation for Active Balancing

For adaptive active balancing control, Hua et al. [27] presented a charge equalizer using a modified half-bridge converter that combines aspects of PWM and PFM control. By adjusting both the duty cycle and switching frequency based on the pack's state, their system could effectively balance cells under different load conditions. This indicates that adaptive control can greatly enhance balancing efficiency, an insight that is leveraged in the presented design as well. The difference in the approach presented in this work is that the adaptive frequency control to a switched-capacitor architecture is applied, which is inherently simpler and more compact than a full DC-DC converter-based equalizer.

In summary, prior art indicates the following:

- Switched-capacitor equalizers are well-suited for compact applications but often require enhanced topologies to achieve high balancing speeds [4].
- Combining multiple active balancing methods (e.g., buck–boost converters with SC networks) or sequencing active and passive schemes can yield better performance than any single method alone [20].
- Adaptive control strategies, such as varying switching frequency (PFM) or duty cycle (PWM) based on real-time cell imbalance, can significantly improve balancing efficiency and mitigate issues like excessive current spikes or oscillatory behavior [17,27].

These findings from the literature form the foundation for the hybrid approach. In the next section, the design of the PFM-controlled SC-based hybrid balancer will be discussed in detail, which seeks to incorporate these best practices while maintaining a minimal hardware profile for use in portable electronics.

3. Proposed Duty-Cycled Hybrid Balancing System and Adaptive PFM Active Balancing

This section describes (1) the duty-cycled hybrid balancing system that interleaves SC-based active balancing with passive bleeding, and (2) a standalone adaptive PFM strategy for SC-based active balancing. Each circuit topology and its on-chip implementation will be discussed, then derive equations governing balancing dynamics and efficiency.

3.1. Duty-Cycled Hybrid Balancing System

3.1.1. Circuit Topology and On-Chip Implementation

Figure 4 shows the actual hybrid balancer chip architecture, the architecture is extended from the functional system diagram as shown in Figure 3. Three flying capacitors, each with $C_f = 120\,\mu\text{F}$, are used to shuttle charge between adjacent cells through the switches in block *Active Balancing Control*. Each cell i also has a shunt resistive bleed branch

$R_{\text{bleed}} = 47\,\Omega$ controlled by block *Passive Balancing Control*. All switch-drive level shifters, comparators, and digital logic are integrated in respective two blocks.

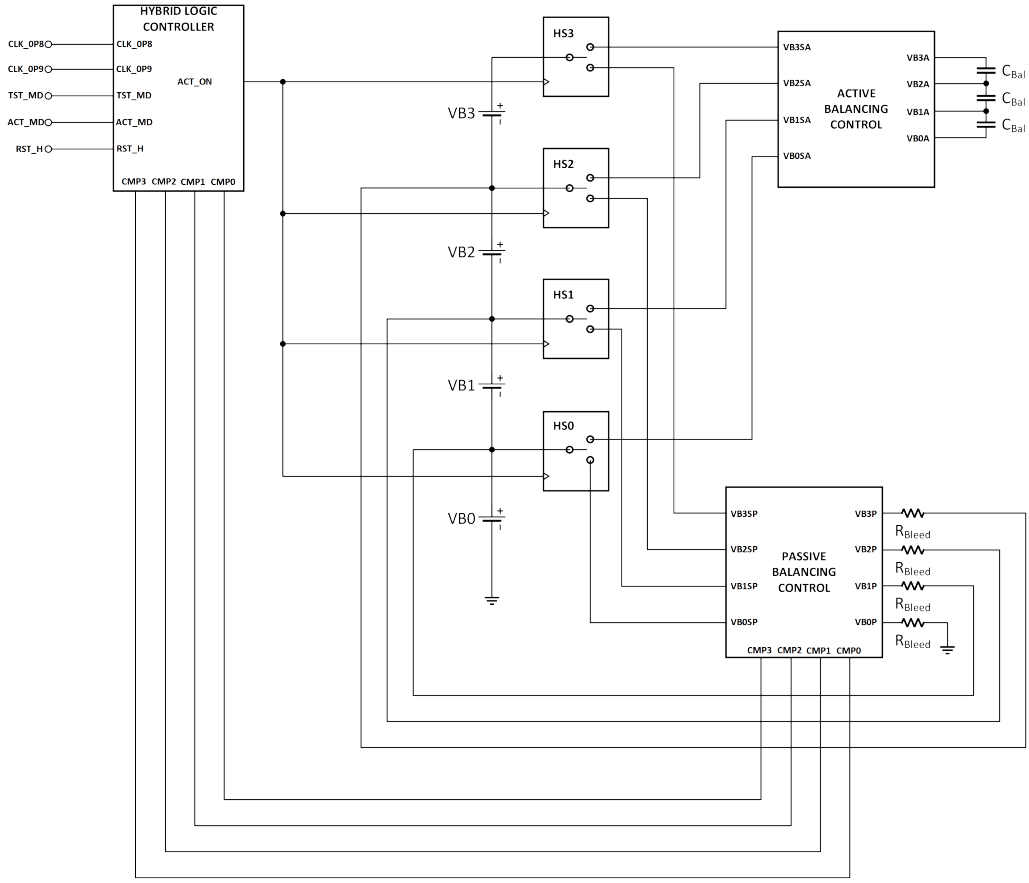


Figure 4. Duty-cycled hybrid balancer architecture

3.1.2. Digital Controller Architecture

The on-chip controller comprises the following:

- An OCV measurement unit that samples each cell voltage V_{B_i} through a comparator.
- A mode logic that computes average voltage with the Equation (1) and number of balanced cell with the logic in (2).

$$V_{\text{avg}} = \frac{1}{4}\sum_{i=0}^{3} V_{B_i} \tag{1}$$

$$N_{\text{Bal}} = \left|\{i : V_{B_i} \geq V_{\text{avg}}\}\right| \tag{2}$$

- A duty-cycle controller passing the gate signals from external clock for the SC network and bleed transistors according to N_{Bal}.

3.1.3. Control Algorithm and Threshold Selection

At each 100 ms cycle, the scheduler sets the SC-active fraction:

$$\begin{cases} 90\%\text{ active, }10\%\text{ passive,} & N_{\text{Bal}} \geq 2, \\ 80\%\text{ active, }20\%\text{ passive,} & N_{\text{Bal}} \geq 3, \\ 100\%\text{ active, }0\%\text{ passive,} & \text{otherwise.} \end{cases}$$

The passive branch trims residuals but dissipates heat; the SC path performs active balancing, largely lossless redistribution (switch and ESR losses only). For the 47 Ω resistor, the instantaneous dissipation during passive balancing is as shown in (3).

$$P_{\text{on}} = \frac{V^2}{R} \approx \frac{(4.2\,\text{V})^2}{47\,\Omega} \approx 0.38\,\text{W} \tag{3}$$

The average passive power over a control period is as shown in (4).

$$\bar{P} = D_{\text{passive}} \frac{V^2}{R} \approx \begin{cases} 38\,\text{mW}, & D_{\text{passive}} = 10\%, \\ 75\,\text{mW}, & D_{\text{passive}} = 20\%, \end{cases} \tag{4}$$

As calculated in (4), the power dissipated through the resistor is far below the resistor's 7 W power rating and keeps the steady temperature rise small. Through–hole resistors have thermal time constants on the order of seconds; with a 100 ms cycle, the per-cycle temperature ripple is small and the steady rise is set by $\bar{P}$. A typical heat rise chart for the through-hole resistor implies a practical $\theta_{JA} \sim 35$ K/W, so $\bar{P} = 38$–75 mW corresponds to ∼1.3–2.6°C rise. These fractions are implementation-dependent and can be re-tuned to a different thermal budget.

3.2. Adaptive Pulse-Frequency Modulation Active Balancing

3.2.1. Circuit Topology

The SC network and flying capacitor are identical to the hybrid system, but no bleed resistors are used. The controller only adjusts the switching frequency.

3.2.2. Frequency Scaling Law

The adaptive PFM control law maps the instantaneous maximum cell-to-cell voltage difference $\Delta V_{\max}(t)$ to the SC switching frequency via simple linear scaling. To characterize the switching frequency evolution under adaptive PFM, we ran a time-domain simulation; the setup is described in Section 4. As balancing progresses, the controller updates the switching frequency according to the scaling law, producing the trajectory shown in Figure 5. Equation (5) is used to define the frequency.

$$f(t) \;=\; f_{\min}\left(1 + k_f\,\Delta V_{\max}(t)\right) \tag{5}$$

where k_f, as shown in Equation (6), is a designer-defined gain with a unit of V^{-1} and $f_{\min}$ sets the lower frequency bound.

$$k_f = \left(f_{\max}/f_{\min} - 1\right)/\Delta V_{\max} \tag{6}$$

In our implementation, the parameter was chosen to be 3.5, so the frequency range can cover up to 3048 Hz. In this chip, k_f was set by an empirical post-layout sweep to confine the switching frequency to 956.24–3048 Hz; because the optimum depends on device parasitics, and cell ESR/capacity, other implementations should re-tune k_f for their specific hardware. Our system has the following parameters as a result.

$$\begin{cases} f_{\min} = 956.24\ \text{Hz}, \\ f_{\max} = 3048\ \text{Hz}, \\ \Delta V_{\max} = 1.40\ \text{V}. \end{cases}$$

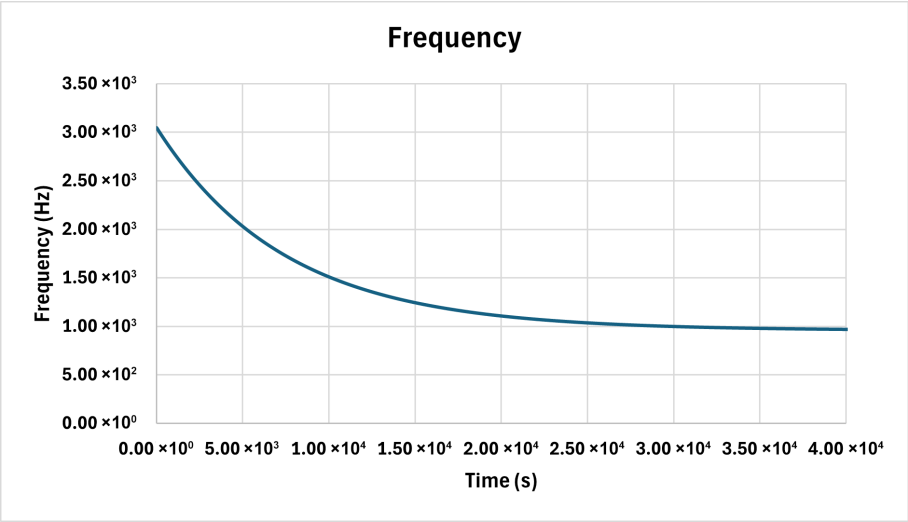


Figure 5. Adaptive PFM switching-frequency profile vs. time (s).

3.3. Layout Implementation and Parasitic Extraction

The hybrid balancer was laid out in Cadence Virtuoso with floorplan partitioning: SC-switch banks adjacent to cell pads, transistor switches for bleed-resistor were symmetrically placed, and digital logic was centralized as shown in Figure 6, which corresponded to the device under test (DUT), "NTUBMSTOP", as shown in Figure 7. The die measures 1730 µm × 1452 µm. The switches are designed to have a on-resistance of 2 Ω. As the SC only redistributes charge within the stack and average branch currents taper as ΔV decreases, conduction loss in the 2 Ω path remains a small fraction of the imbalance energy; measured redistribution efficiencies of hybrid balancing scheme in Section 4 remain 97.71%.

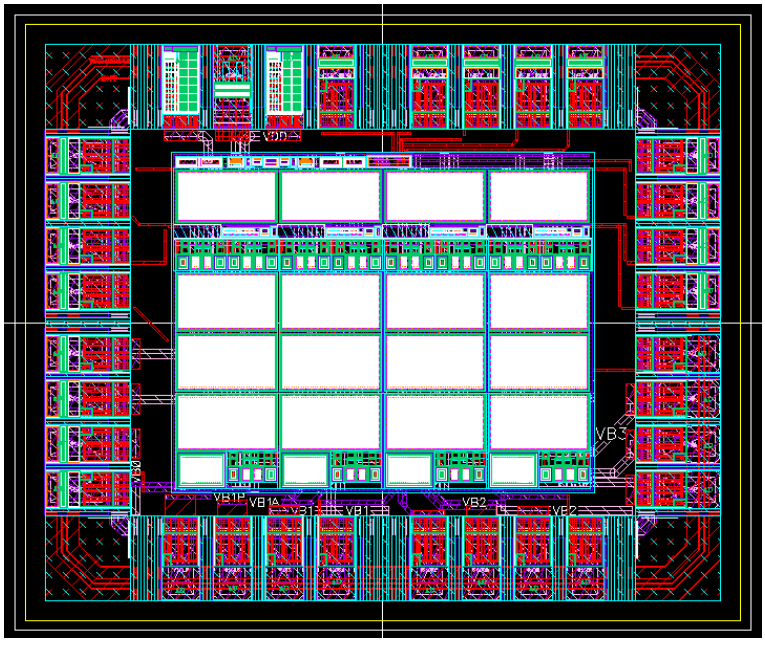


Figure 6. Layout of the hybrid balancer IC.

3.4. Test-Bench Set-Up for Post-Layout Simulation

The evaluation testbench included ESD diodes and decoupling capacitors (Figure 7), with all level shifting and gate driving performed on-chip. On the testbench, four subtractors provide individual cell voltage monitoring, two 10 Hz hybrid control clocks with 80% and 90% duty cycle, and a clock for active cell balancing switching control.

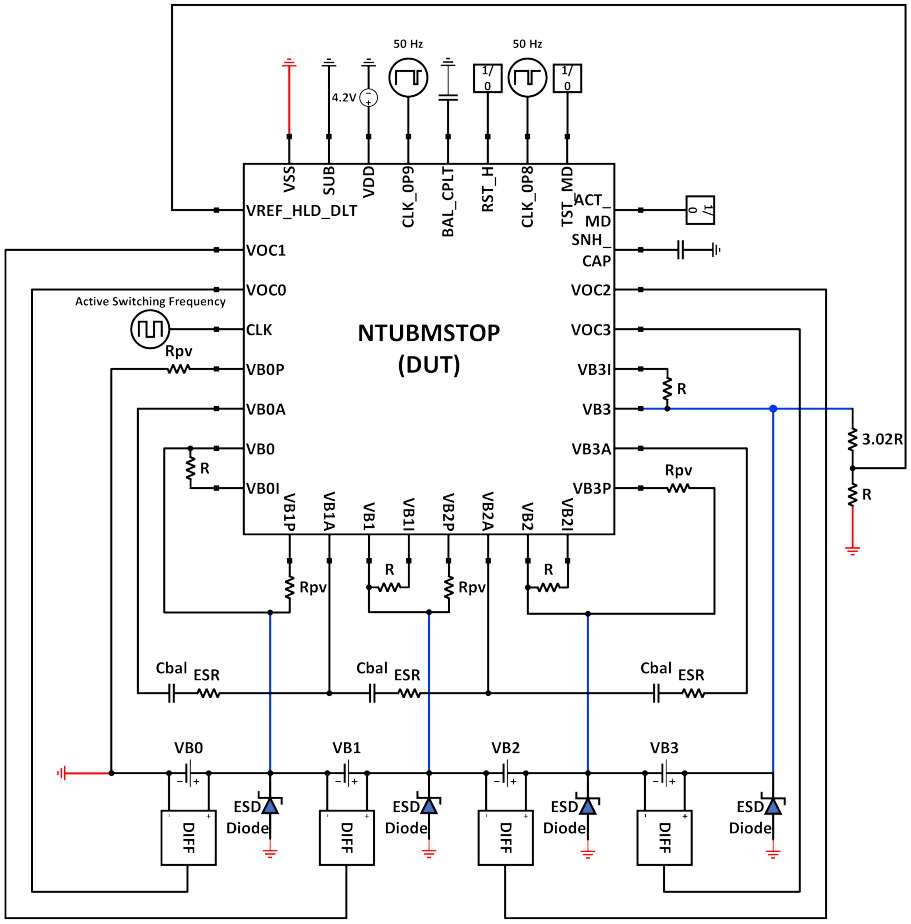


Figure 7. Test-bench with hybrid balancer chip (NTUBMSTOP).

4. Simulation Results and Discussion

Simulations use ideal 3.4 Ah cell models ($C_{\text{cell}} = 3.4$ Ah, $R_{ESR} = 50$ mΩ). Initial OCVs are listed in Table 2.

Table 2. Initial cell open-circuit voltages.

Cell Index	Cell's OCV (V)
V_{B3}	3.3
V_{B2}	4.2
V_{B1}	4.0
V_{B0}	2.8

Figure 8 shows the cell-voltage convergence under each scheme. The hybrid approach rapidly equalizes bulk imbalance via SC transfer, then fine-tunes it via bleeding, thereby avoiding the slow tail balancing seen in fixed-frequency active schemes. The switching between active and passive balancing is interleaved to improve thermal control.

The trajectories in Figure 8 show two phases. (i) Active cell balancing (initial steep slopes): the SC network dominates and rapidly collapses the OCV spread. (ii) Late-stage trimming (as highlighted in the magnified inset of Figure 8): brief passive balancing to remove small residual offsets that are inefficient to be balanced with SC-based active balancing alone. The hybrid schedule interleaves short passive intervals (10–20% of each 100 ms cycle) with predominantly active transfer and maintains the average bleed power to ∼38–75 mW over each resistor, keeping the resistor temperature rise small.

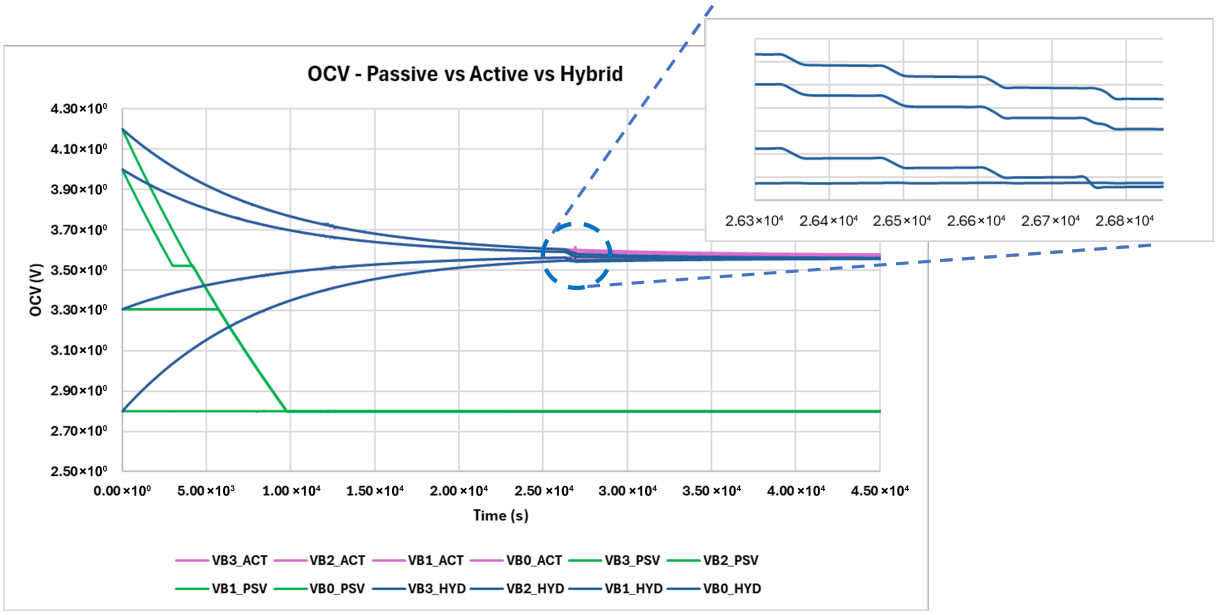


Figure 8. Cell voltage convergence for passive, active, and hybrid schemes.

Table 3 reports total balancing time and energy efficiency computed via Equations (7) and (8).

$$E_{\text{bled}} = E_{\text{start}} - E_{\text{end}} \tag{7}$$

$$\eta = \frac{E_{\text{start}} - E_{\text{end}}}{E_{\text{start}}} \times 100\%. \tag{8}$$

Passive yields $\eta \approx 0\%$, active 99.89%, hybrid 97.71%, and adaptive PFM 99.86%.

Table 3. Post-layout balancing performance for 4-cell stack.

Scheme	Time (h)	Efficiency (%)
Passive	2.72	0.00
Active	8.93	99.89
Hybrid	7.48	97.71
Adaptive PFM	8.06	99.86
Fixed Low (956 Hz)	8.30	99.91
Fixed High (3048 Hz)	7.87	99.70

Table 4 summarizes the performance and hardware trade-offs of passive, SC-based active, and the proposed hybrid approach.

Table 4. Qualitative comparison of balancing methods for a 4-cell pack.

Aspect	Passive	Active (SC)	Hybrid (Proposed)
Balancing Time	Hours	Minutes–hours	7.48 h
Energy Efficiency	0%	$>99\%$	97.71%
Thermal Behavior	High heat	Low heat	Low heat
Circuit Complexity	Very low	Low–Medium	Medium
Overall Utilization	Reduced	Near-maximal	Near-maximal

5. Discussion and Comparison

With the simulation results presented in a previous section, a comparison between this work and other works is as summarized in Table 5.

Table 5. Performance comparison with recent works.

Method	Cells	Time (h)	Eff. (%)	Notes
Adaptive Hybrid (SC + Resistor)—This Work	4	7.48	97.71	Minimal magnetics; details is summarized in Table 3.
Adaptive PFM Active (SC-only)—This Work	4	8.06	99.86	Details is summarized in Table 3.
Buck-Boost Active [28]	6	≈0.37	≈97.05	22 V pack; centralized DC-DC converter achieves very fast balancing via high transfer currents; added complexity.
H-DCB Hybrid [25]	96	6.0	-	Uses H-bridge + DC-DC pack bypass; ∼35% faster vs. passive/DCB.

The efficiencies reported here used (8), defined as the fraction of imbalance energy redistributed rather than bled energy only. The proposed methods achieve a high redistribution efficiency (97.71–99.86%), on par with the active-only systems (e.g., 97–99% in [28]) while using simpler, inductor-less, and essential hardware with a smaller footprint. By contrast, despite the balancing time of this work seems to be longer than cited references [25,28], absolute "balancing time" is not an invariant metric: it depends strongly on the cell chemistry and capacity (C_{cell}), internal resistance/ESR, the initial OCV spread ΔV_{max} and SoC distribution, ambient temperature, as well as the controller's termination threshold and sampling period. Consequently, times reported across different studies are not strictly comparable. Thus, for balancing time comparison, it is better to be compared within the same test set-up. As such, the comparison in Table 3 can better conclude the balancing time improvement across different methodologies.

6. Conclusions

This work introduced two on-chip balancing strategies for four-cell Li-ion packs:

- An OCV-driven, duty-cycled hybrid balancer completing in 7.48 h at 97.71% efficiency with minimal external components.
- A standalone adaptive PFM SC balancer completing in 8.06 h at 99.86% efficiency by dynamically tuning switching frequency.

The hybrid method offers a 16.24% speed-up over active-only with minor efficiency loss, while adaptive PFM delivers near-maximal efficiency with competitive speed. Both outperform pure passive and fixed-frequency active methods in speed–efficiency trade-offs, validating their practicality for integration into compact BMS ICs. Future work could explore dynamic threshold adaptation, layout optimization for larger cell counts, and implementation of on-chip monitoring for predictive thermal management.

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Abbreviations

The following abbreviations are used in this manuscript:

BMS	Battery Management System.
DUT	Device Under Test.
SoC	State-of-Charge (percentage of full charge).
OCV	Open Circuit Voltage.
SC	Switched Capacitor.
PFM	Pulse-Frequency Modulation.
PWM	Pulse-Width Modulation.

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