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Review

Wake-Up Receivers: A Review of Architectures Analysis, Design Techniques, Theories and Frontiers

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Abstract

The rapid growth of the Internet of Things (IoT) has driven the need for ultra-low-power wireless communication systems. Wake-up receivers (WuRXs) have emerged as a key technology to enable energy-efficient, near-always-on operation for IoT devices. This review explores the state of the art in WuRXs design, focusing on low-power architectures, key trade-offs, and recent advancements. We discuss the challenges in achieving low power consumption while maintaining sensitivity, power consumption, and interference resilience. The review highlights the evolution from radio frequency (RF) envelope detection architectures to more complex heterodyne and subthreshold designs and concludes with future directions for WuRXs research.

Keywords: wake-up receiver; wake-up radios; low-power radio; ultra-low power; energy efficiency; wireless sensor nodes (WSNs); internet of things (IoT)

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1. Introduction

As wireless sensor networks and Internet of Things (IoT) systems become increasingly pervasive, the demand for energy-efficient always-on connectivity has intensified [1,2]. In such applications, most sensor nodes remain idle for extended periods, only needing to transmit or receive data occasionally. However, the power consumed by the radio front end, even when idle, can dominate the total energy budget and severely limit battery life or hinder energy harvesting capabilities [3]. To address this bottleneck, the wake-up receiver (WuRX) has emerged as a promising architectural solution [1–8].

A WuRX is a small, ultra-low-power receiver designed to continuously monitor the wireless channel for a specific wake-up signal or identifier. Rather than replacing the main receiver, it serves as an auxiliary always-listening front end. When a wake-up event is detected, the WuRX activates the main radio or processing core, allowing the system to transition from sleep to active mode. The fundamental idea is to offload the idle listening functionality from the power-hungry primary transceiver to an always-on sub-system, thereby significantly reducing standby power consumption. In many reported implementations, WuRXs operate with power budgets in the nanowatt or even picowatt range, enabling battery-less operation through energy harvesting or multi-year lifetimes from small batteries.

On the physical layer, a WuRX can be modeled as a minimal receiver chain comprising a matching network, an optional LNA or passive gain stage, a frequency downconversion

mechanism (e.g., envelope detection or mixer-based heterodyning), a baseband amplifier (BBA), and some form of wake-up logic, typically a digital or analog correlator. Unlike conventional radios, WuRXs often adopt non-coherent architectures without high-precision oscillators, mixers, and analog-to-digital converters (ADC), replacing them with square-law detectors and 1-bit digitizers to minimize power.

Beyond the physical layer, WuRXs play a vital role in system-level performance. By reducing the idle-listening power from milliwatts to nanowatts, they enable aggressive duty cycling, enhance network scalability, and extend the lifespan of battery-powered or energy-harvesting devices. Moreover, WuRXs allow asynchronous communication without pre-negotiated schedules, simplifying MAC-layer design and reducing latency in event-driven sensing systems. In some scenarios, such as implantable medical devices or massive-scale environmental monitoring, WuRXs are not just desirable but essential for practical system deployment. WuRX can also be integrated with backscatter modulation techniques to build ultra-low-power IoT nodes. In such architectures, the WuRX monitors wireless signals and triggers the backscatter transmitter upon detecting a specific wake-up packet. Unlike active radios, backscatter communication reflects and modulates incident RF signals by dynamically adjusting the antenna impedance, eliminating the need for power-hungry RF transmission. This architecture presents a promising pathway for future energy-constrained wireless systems.

Despite their appeal, WuRX design faces a unique set of challenges that differ from those in traditional radio frequency (RF) transceivers. First, achieving adequate sensitivity at such low power budgets is fundamentally difficult, as thermal noise, flicker noise, and limited gain must be managed without resorting to power-intensive circuitry. Second, WuRXs must operate reliably in the presence of strong in-band interference, especially in license-free ISM bands. Given their typically wide input bandwidth and lack of sharp filtering, interference resilience becomes a key bottleneck. Third, achieving accurate synchronization and robust wake-up detection often requires high timing resolution or complex correlation logic, which conflicts with the strict power constraints [6]. Lastly, integration with existing communication protocols such as BLE or Wi-Fi remains nontrivial, particularly when deterministic wake-up or security features are needed [7].

These challenges motivate ongoing research into new WuRX architectures, including passive and mixer-first topologies, digitally assisted baseband processing, ultra-low-power clock generation. As the field matures, balancing trade-offs among power, sensitivity, latency, complexity, robustness, and standard compatibility becomes central to enabling practical WuRX deployments [8,9].

In this paper, we present a comprehensive review of recent advancements in WuRX design, focusing on architectural innovations, circuit-level techniques, and system-level considerations. We aim to provide both a high-level overview and technical depth on how WuRXs can be optimized to meet the evolving demands of next-generation wireless systems. Section 2 introduces the key design specifications of WuRX systems. Section 3 reviews mainstream WuRX architectures. Sections 4–6 discuss key techniques used in different architectures, including RF envelope detection, on-chip LO, and transmitted-LO designs. Section 7 presents other supporting circuit techniques applicable across architectures. Section 8 explores emerging trends and frontier research in WuRX design. Section 9 discusses figure-of-merit (FoM) metrics for quantitative comparison. Finally, Section 10 concludes the paper with a summary of key findings.

2. WuRX Design Specifications

Compared to conventional RF receivers, WuRXs are designed for specialized applications, typically operating under much lower power conditions and better suited for

intermittent, event-driven communication tasks. As a result, their design requires careful trade-offs among multiple performance metrics based on practical requirements. Common design specifications include power consumption, sensitivity, data rate, latency, operating frequency, interference tolerance, carrier frequency, robustness, and compatibility with standard communication protocols.

1. Power consumption: Since WuRXs are responsible for maintaining continuous listening while the main receiver is in standby mode, power consumption becomes the most critical design constraint. It must be significantly lower than that of the main receiver. For applications where maintenance is scarce, lower power is better, such as assisting sensor communications in remote areas. For scenarios such as smart homes, power consumption limits can be relaxed. Reported power consumption in the literature ranges from several hundred microwatts down to below 1 nanowatt [7,10–15]. To reduce power, most WuRX designs operate at supply voltages lower than the nominal voltage of the adopted integrated circuit process, allowing MOS transistors to remain in the subthreshold region. Other common low-power techniques include passive demodulation, duty cycling, and simplified signal processing.
2. Sensitivity: Sensitivity determines the minimum signal strength that a WuRX can detect, and thus directly affects its communication range. Ideally, the sensitivity of a WuRX would match that of the main receiver, but due to simplified front end architectures and power constraints, practical WuRX designs typically achieve sensitivities between -60 and -90 dBm [11,14,16–20], with only a few exceptional cases reaching -100 dBm [6,10,21,22]. To improve sensitivity, common techniques include incorporating RF front end gain stages, passive matching networks, and optimized baseband processing circuits.
3. Latency and data rate: The primary function of a WuRX is to detect wake-up commands rather than support continuous data communication. Therefore, its latency requirements are generally relaxed and vary depending on the application. Some use cases, such as applications that periodically report device status, can tolerate delays of several seconds [12,23], while others like scenarios involving health and security require a response within a few microseconds [18,24,25]. WuRX latency is typically tied to the data rate, which, similar to conventional receivers, has a direct impact on the achievable sensitivity.
4. Interference Tolerance: In crowded RF environments, especially in the ISM bands where many IoT devices operate, the ability to reject in-band and adjacent-channel interference is critical. WuRXs based on non-linear demodulation like envelope detection (ED) are more susceptible to noise and nonlinear distortion [12,13]. In contrast, WuRXs that utilize high-precision local oscillators tend to exhibit stronger interference rejection at the cost of power consumption [10,11]. Another effective approach is using filtering modules, such as high-Q input matching networks or Micro-Electro-Mechanical-Systems (MEMS)-based filters.
5. Carrier frequency: The carrier frequency of WuRXs is typically in the sub-GHz range, such as 433 MHz or 915 MHz [1,6,13,14,26], which are commonly used in IoT applications. Some designs also target higher frequencies, such as 2.4 GHz, to leverage existing communication protocols like Wi-Fi, Bluetooth and Zigbee [11,16]. Higher carrier frequencies offer larger effective RF bandwidth, smaller antenna and circuit dimensions, and improved integration density [4]. However, these benefits come at the cost of increased power consumption in gain and filtering circuits, reduced communication range, and lower passive gain due to low-Q inductors typically available at higher frequencies.

6. Robustness: Many WuRX circuits operate in the subthreshold region to achieve ultra-low power consumption. However, this operating mode makes them inherently more vulnerable to process, voltage, and temperature (PVT) variations. These issues are particularly critical in applications where the WuRX is expected to function in harsh or maintenance-free environments, requiring robustness against temperature fluctuations. Additionally, for WuRXs powered by energy harvesting systems, supply instability must be carefully considered, as variations in input voltage can further degrade circuit stability and sensitivity.
7. Compatibility: Ensuring that the WuRX is compatible with existing communication protocols such as Wi-Fi, Bluetooth, and Zigbee can significantly expand its range of practical applications [11,16]. However, this compatibility often requires additional complexity in the design, such as implementing specific modulation schemes or protocols.

When designing a WuRX, the power consumption requirements of the target application should be considered first, as power directly constrains the achievable sensitivity and latency. Other performance metrics such as interference tolerance and robustness can then be optimized accordingly. Section 3 will provide a detailed discussion of various WuRX architectures suited for different application scenarios.

3. Current Mainstream Wake-Up Receiver Architectures

The three predominant WuRX architectures are as follows:

1. RF envelope detection architecture;
2. On-chip LO architecture;
3. Transmitted-LO architecture.

RF envelope detection architecture achieves the lowest power consumption but suffers from limited interference rejection and sensitivity. The on-chip LO architecture improves interference immunity by downconverting RF signals to an intermediate frequency (IF) using an on-chip generated LO, although at the cost of higher power consumption from clock generation circuits. The transmitted-LO architecture eliminates high-power LO circuits by embedding LO information within transmitted signals but introduces system complexity and protocol compatibility challenges.

3.1. RF Envelope Detection Architectures

The RF envelope detection WuRX is the simplest and most power-efficient architecture, serving as the foundation for other designs. It directly demodulates incoming RF signals to baseband by an envelope detector (ED). The absence of the LO and mixer significantly reduces power consumption, making this architecture suitable for ultra-low-power applications [19,27,28]. However, the limitation on power consumption also limits the sensitivity and data rate upper limit of WuRX.

The Figure 1 shows the conventional architectures of RF envelope detection WuRXs. The ED's nonlinear characteristics enable self-mixing of incoming RF signals, directly generating baseband signals without requiring power-hungry RF modules such as low noise amplifies (LNAs) or phase-locked loops (PLLs). This architecture achieves ultra-low power consumption by eliminating complex circuits and leveraging relaxed data rate requirements (typically 10 bps–10 kbps) through reduced baseband processing frequencies. However, as shown in (1), the self-mixing process inherently discards frequency and phase information while lacking quadrature (I/Q) signal separation, limiting compatibility to On–Off Keying (OOK) modulation and resulting in poor interference rejection. Additionally, direct

downconversion to the BBA is more susceptible to DC offset and 1/f noise, necessitating advanced calibration techniques for practical implementations [5,8,15,19].

$$V_{out} = \frac{k}{2}A^2(t) \quad (1)$$

where $A(t)$ is the modulating signal, normally OOK signal, and k is the scaling factor of the ED.

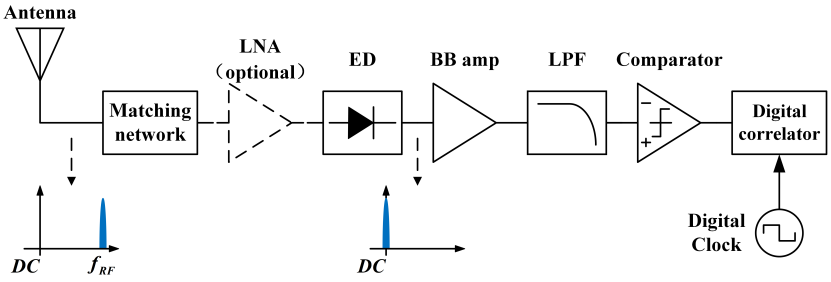


Figure 1. The conventional RF envelope detection architecture with signal spectrum.

The matching network between the RF signal source and the ED is critical, providing dual functionality: passive voltage gain and interference filtering. As derived in (1), the ED's square-law operation causes passive gain (measured in dB) to manifest as quadratic improvement in output power. Simultaneously, the passive network suppresses out-of-band noise and interference, thereby enhancing both sensitivity and interference immunity. This dual benefit makes impedance matching optimization essential for balancing performance metrics in WuRX designs.

The low-pass filter (LPF) and BBA further process the output from the ED. By operating at extremely low frequencies due to the low data rate, these modules significantly reduce overall system power consumption. The filtered and amplified signal is then analyzed through a comparator and digital correlator to detect valid wake-up beacons.

This cascaded approach maintains <100 nW total power while achieving <0.1% missed detection rate (MDR) for input levels ranging from −70 to −60 dBm [15,29–31].

3.2. On-Chip LO Architecture

The RF envelope detection architecture prioritizes power efficiency over-sensitivity in this fundamental trade-off. However, for IoT applications demanding higher sensitivity like long-range environmental sensors, the on-chip LO architecture becomes preferable. As depicted in Figure 2, this architecture downconverts RF signals to baseband/IF through mixing with a LO, followed by envelope detection and baseband processing stages similar to the RF envelope detection architectures (ED, BBA, etc.). While integrated LO circuitry can improve sensitivity, its clock generation circuits, particularly those operating above 1 GHz, significantly increase power consumption, often exceeding sub-µW thresholds [11,32]. Depending on the accuracy of the LO frequency, this architecture can also provide improved interference rejection [10,26].

Similar to conventional receivers, the on-chip LO architecture can employ both zero-IF and low-IF configurations. For OOK modulated signals, the zero-IF approach enables direct demodulation after envelope detection but remains susceptible to 1/f noise in ultra-low data-rate applications. While the low-IF architecture mitigates 1/f noise through dual downconversion stages and filtering, achieving low-power image rejection presents significant implementation challenges.

Notably, as shown in (1), the ED inherently discards frequency information, eliminating the need for precise IF frequency control—the core principle of uncertain-IF

architectures [20,33]. Replacing PLLs with voltage-controlled oscillators (VCOs) reduces power consumption at the cost of wider IF bandwidths and elevated intermediate-frequency noise. This design compromise makes uncertain-IF systems suitable for applications requiring sensitivity marginally beyond the limits of RF envelope detection architectures.

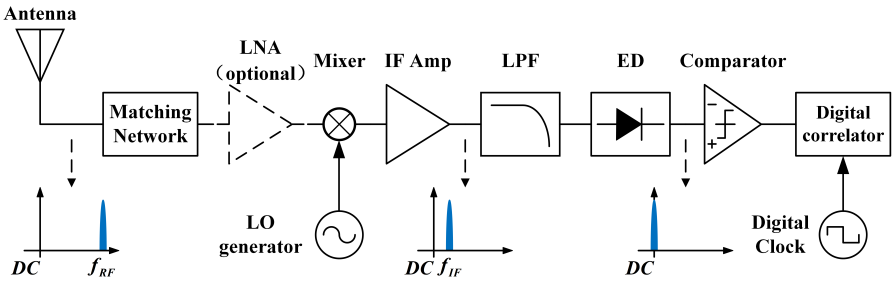


Figure 2. The conventional on-chip LO architecture with signal spectrum.

The on-chip LO architecture closely resembles that of conventional RF receivers. It downconverts the incoming RF signal to an intermediate or baseband frequency using a mixer, enabling precise frequency control and compatibility with existing communication protocols. Some WuRX designs adopt a zero-IF architecture, omitting the LNA and directly mixing the RF signal, followed by digital baseband processing to extract the wake-up signal. Such implementations can achieve sub-mW power consumption and sensitivity better than -90 dBm [16,34]. Other designs employ low-IF architectures to shift the signal away from the $1/f$ noise corner, thereby improving both sensitivity and robustness. These systems can also support techniques such as I/Q mixing and dual-mode operation for BLE and Wi-Fi, offering a balanced trade-off between multi-protocol compatibility, low power consumption, and high performance [7,26,35].

3.3. Transmitted-LO Architectures

The transmitted-LO architecture eliminates integrated clock circuits by externally supplying LO signals for frequency downconversion. As depicted in Figure 3, the classic two-tone implementation utilizes the ED's self-mixing property: simultaneous injection of RF and LO signals generates IF signal components through mutual mixing. This enables IF bandpass filtering to enhance interference rejection.

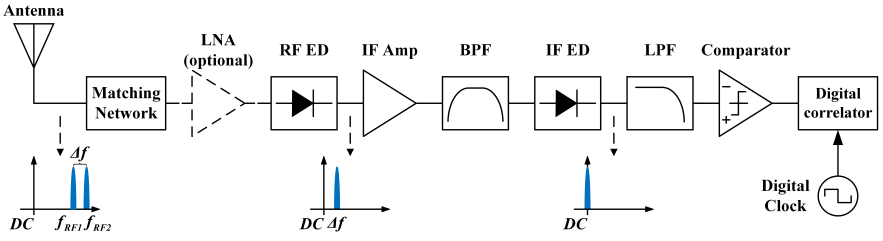


Figure 3. The conventional transmitted-LO architecture with signal spectrum.

Further optimization of two-tone signals, via channel-embedded on–off keying (CE-OOK) or spread spectrum techniques, can improve sensitivity and noise immunity. CE-OOK technique modulates the RF carrier using OOK by a BFSK-pre-modulated IF signal. CE-OOK is more compatible with communication protocols, while also improving the sensitivity and interference injection of the receiver, but it also increases the complexity of the receiver [20,22]. Spread spectrum technique modulates the RF carrier using a pseudo-random sequence, which can improve the robustness of the receiver against interference, but it also reduces compatibility [24,36,37].

Transmitted-LO architectures without on-chip LO cannot fully comply with the requirements of standardized communication protocols. However, they can still leverage existing transmitters to send wake-up signals. For instance, multi-carrier on–off Keying (MC-OOK) modulation can be implemented by selectively enabling or disabling specific subcarriers within a Wi-Fi orthogonal frequency division multiplexing (OFDM) transmitter to represent binary "1" and "0" [11].

4. Key Techniques in RF Envelope Detection Architecture

4.1. Envelope Detector

The ED serves as the most critical module in WuRXs, being universally adopted across nearly all architectural implementations. Its primary function relies on the nonlinear characteristics of semiconductor devices such as MOSFET, diodes, and bipolar junction transistors (BJTs) to enable self-mixing of input signals, thereby allowing OOK demodulation

$$V_{ED,in} = A(t)\cos(2\pi f_c t) \tag{2}$$

$$V_{ED,out} = kV_{ED,in}^2 = kA^2(t)\cos^2(2\pi f_c t) = \frac{k}{2}A^2(t)(1+\cos(2\pi\cdot 2f_c t)) \tag{3}$$

where k is the scaling factor of the ED, and f_c is the carrier frequency. Therefore, the input signal is shifted to the DC component and the double frequency $2f_c$ component. After passing through the LPF, the output signal as shown in (1) retains only the DC component $kA^2(t)/2$.

As demonstrated by [5], the RF noise undergoes two distinct transformations after passing through the ED: the self mixing of noise in (4) and the mixing between the signal and noise in (5).

$$\sigma_{ED,out,N^2}^2 = k^2\sigma_{ED,in}^4 \tag{4}$$

$$\sigma_{ED,out,SN}^2 = 2k^2\sigma_{ED,in}^2 P_{in}A_v^2 \tag{5}$$

$$\sigma_{ED,out}^2 = \sigma_{ED,out,N^2}^2 + \sigma_{ED,out,SN}^2 \tag{6}$$

where A_V is the voltage gain of the matching network, LNA and other circuits before the ED, P_{in} is the power of input RF signal, and $\sigma_{ED,in}^2$ is the total noise power at the ED input. Figure 4 illustrates the spectral transformation of RF-stage noise and signals after passing through the ED [5].

The system sensitivity is formally expressed in (7),

$$\begin{aligned} P_{MDS} = {} & 4SNR_{MIN}BW_{BB}F_{FE}K_BT + \\ & 2F_{FE}K_BT\sqrt{4BW_{BB}^2SNR_{MIN}^2 + BW_{RF}BW_{BB}SNR_{MIN}} \end{aligned} \tag{7}$$

where F_{FE} is the noise factor of the front end, K_BT is the thermal noise floor, K_B is the Boltzmann's constant, T is the absolute temperature, BW_{RF} is the RF bandwidth, BW_{BB} is the baseband bandwidth, and SNR_{MIN} is the minimum SNR which is determined by the modulation method and specific application requirements.

The system sensitivity exhibits distinct dependence on RF bandwidth characteristics: when operating with wide RF bandwidth, sensitivity is predominantly governed by noise self-mixing as shown in (8), whereas under narrow RF bandwidth conditions, the signal-noise cross-mixing becomes the limiting factor as shown in (9).

$$P_{MDS,N^2} = 2F_{FE}K_BT\sqrt{BW_{RF}BW_{BB}SNR_{MIN}} \tag{8}$$

$$P_{MDS,SN} = 8SNR_{MIN}BW_{BB}F_{FE}K_BT \tag{9}$$

The upper bound of sensitivity is linked to both RF and baseband bandwidth characteristics. Figure 5 demonstrates this relationship by plotting sensitivity against RF bandwidth and front end noise figure (NF) under a fixed baseband bandwidth of 10 kHz.

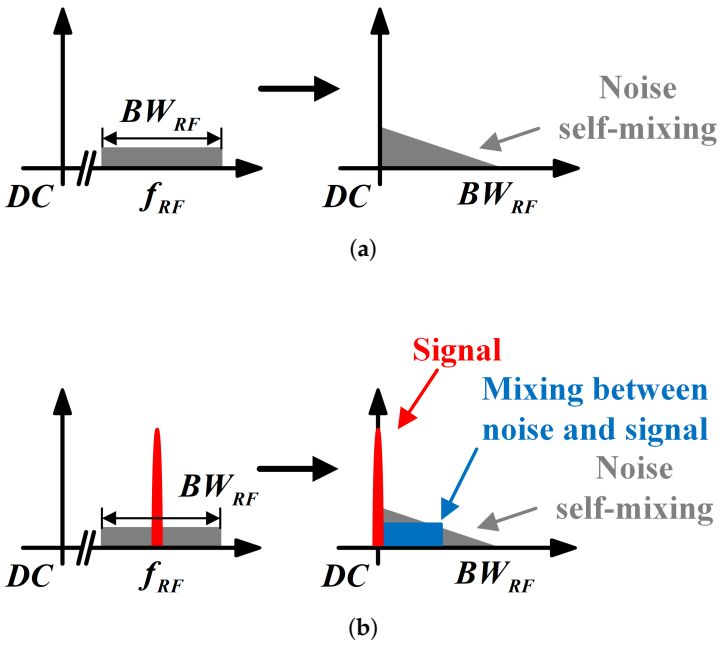


Figure 4. Power spectrum density versus frequency for (**a**) noise self-mixing and (**b**) mixing between noise and signal.

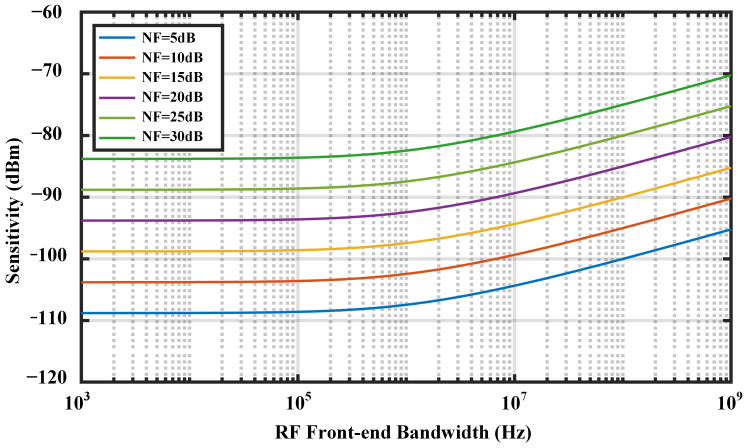


Figure 5. RX sensitivity at 10 kHz BW_{BB} with different NF and RF bandwidths when limited by RF stage noise.

EDs can be categorized into passive and active architectures. Passive EDs, characterized by the absence of DC bias currents, eliminate 1/f noise and additional power consumption, making them the predominant choice in WuRXs. While passive structures inherently lack gain and support only low data rates, (7) reveals that their sensitivity remains unaffected by RF-stage amplification. Crucially, the low-data-rate limitation aligns well with the operational requirements of most WuRX applications, where infrequent wake-up events prioritize ultra-low standby power over high throughput.

Beyond radio-frequency noise, baseband noise constitutes another critical limiting factor for achievable receiver sensitivity [5].

$$P_{MDS,BB} = \frac{20\sqrt{\overline{v_{n,eq}^2} SNR_{MIN}}}{kA_v^2} \tag{10}$$

where $\overline{v_{n,eq}^2}$ is the input-referred BB noise power in the form of voltage square, which should also include the noise of the ED generated after squaring. Neglecting 1/f noise, the total thermal noise power is

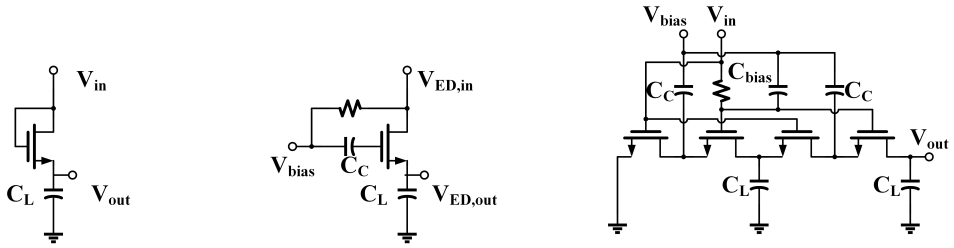
$$\overline{v_{n,eq}^2} = K_B T \cdot BW_{BB} \tag{11}$$

Equation (10) can be rewritten as

$$P_{MDS,BB} = \frac{20\sqrt{K_B T \cdot BW_{BB} SNR_{MIN}}}{kA_v^2} \tag{12}$$

4.1.1. Passive ED

Figure 6 illustrates the typical configuration of a passive ED. In its simplest form, the RF signal is simultaneously applied to the gate and drain terminals of a MOSFET, enabling self-mixing through the device's nonlinear transconductance characteristics. A DC bias voltage at the gate terminal optimizes input impedance matching, thereby maximizing passive voltage gain. However, the limited conversion gain of single-stage implementations amplifies baseband noise challenges.



(**a**) (**b**) (**c**)

Figure 6. (**a**) Conventional ED. (**b**) One-stage self-mixer. (**c**) Four-stage self-mixer circuit.

To address this limitation, recent studies [15,30,38] propose integrating Dickson charge-pump topologies into multi-stage EDs as shown in Figure 6c. This approach achieves progressive voltage doubling through cascaded stages, with the output voltage expressed as

$$V_{ED,N,out} = N\frac{V_{ED,in}^2}{2nV_t} \tag{13}$$

where N is the stage count, n is the coefficient for the subthreshold slope and $V_t = K_B T/q$.

As noted in [15], the relationship between the output resistance and the input resistance of this structure is given by

$$R_{out} = N^2 R_{in} \tag{14}$$

Therefore, the thermal noise of the ED is expressed as follows:

$$PSD_{ED,N,out} = 4K_B T N^2 R_{in} \tag{15}$$

When considering only the thermal noise of the ED, the output signal-to-noise ratio (SNR) derived from (13) and (15) is expressed as

$$SNR_{ED,N} = \frac{V_{ED,N,out,RMS}}{PSD_{ED,N,out} f_s} = \frac{1}{K_B T f_s}\frac{1}{4n^2}\frac{A_V^2 P_{in}^2 R_s^2}{R_{in} V_t^2} \tag{16}$$

While (16) indicates no direct dependence of SNR on the stage count N, increasing the number of stages enhances voltage gain, facilitating subsequent noise suppression and reducing baseband current consumption. This approach is highly efficient because passive EDs use almost no power. However, excessive stage counts degrade the ED's input impedance, thereby compromising passive voltage gain from the matching network. This issue will be further discussed in subsequent sections.

Traditional differential implementations require off-chip baluns (balanced-unbalanced transformers), but their limited Q-factor reduces passive gain. The structure in Figure 7 addresses this by generating opposite-polarity voltages through directional adjustments, creating a pseudo-differential ED. Compared to single-ended designs, this approach achieves double the conversion gain and 1.5 dB sensitivity improvement while eliminating bulky baluns.

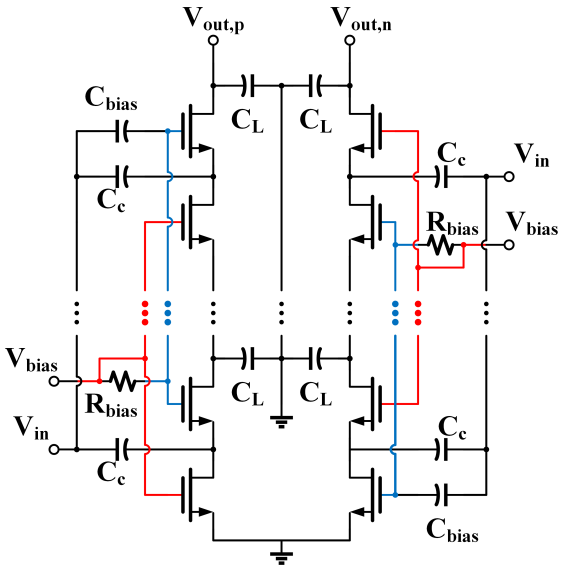


Figure 7. Differential passive ED structure.

4.1.2. Active ED

Active EDs can provide higher input impedance and faster data speeds. They remain important in specific applications such as high-speed medical monitoring for tracking heart signals, and wideband sensing used in factory equipment monitoring. In these applications, delays of seconds may cause security issues.

Figure 8 shows a basic active ED design. By performing Taylor expansion on the MOSFET's subthreshold voltage-current characteristics and retaining the second-order term, the quadratic dependence of output current on input RF voltage is derived:

$$i_d = I_s \cdot \frac{v_{GS}^2}{2n^2 V_t^2} \tag{17}$$

This intrinsic square-law behavior enables direct amplitude demodulation through self-mixing. The demodulated signal is subsequently converted to an output voltage through either resistive loads or MOS-based active loads. This conversion stage impact the ED's voltage gain and output noise characteristics.

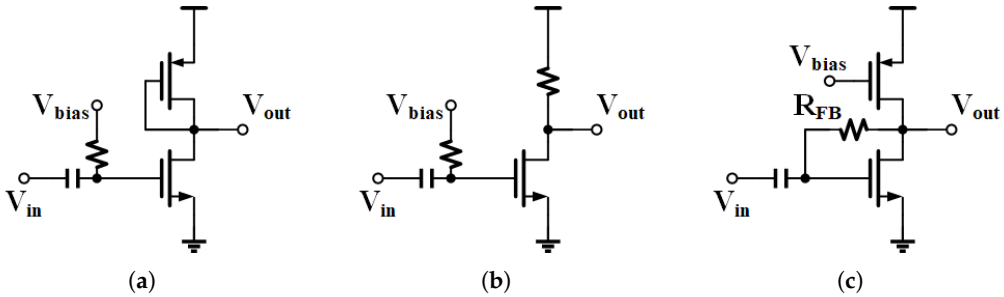


Figure 8. Active ED structures (**a**) with active diode loading, (**b**) with resistor loading, (**c**) with active-L biased ED and equivalent output impedance.

Similar to passive architectures, active EDs can utilize current-reuse pseudo-differential structures as shown in Figure 9. Operating in the subthreshold region, this design maintains sufficient voltage headroom even under a 0.5 V supply. However, inherent mismatches between PMOS/NMOS transistors and load variations lead to output voltage asymmetry.

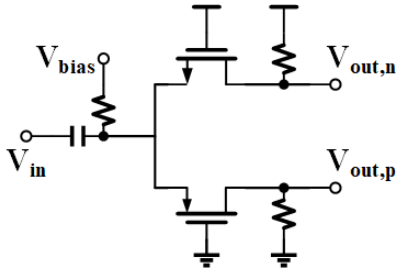


Figure 9. Active differential ED structure.

4.1.3. Matching Network

In RF envelope detection architectures, the limited pre-ED gain makes baseband noise the dominant factor in sensitivity. Therefore, according to (10), any additional (in dB) gain introduced before the ED can ideally double the improvement in system sensitivity (in dB), making the matching network crucial, which can provide passive gain.

Figure 10 illustrates typical L- and π-type matching networks used in RF envelope detection WuRX architectures. The parameter C_{in} represents the equivalent input capacitance of the WuRX, including contributions from bond pads, package, PCB, etc. Similarly, R_{in} denotes the equivalent input resistance of the WuRX.

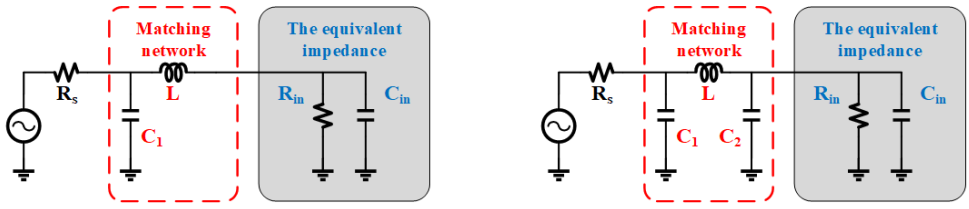


Figure 10. Typical (**a**) L- and (**b**) π-type matching networks.

The gain of the L-type passive matching network can be expressed as [15]

$$A_v = \sqrt{\frac{R_{in}}{R_s}} \Big/ \sqrt{1 + \frac{\omega_{RF} R_{in} C_{in}}{Q_L}} \tag{18}$$

where Q_L is the quality factor of the inductor (assuming the resonant frequency is much higher than $\omega_{RF}/2\pi$), R_s is the antenna source impedance, and ω_{RF} is the angular frequency

of the RF signal. From this equation, the gain is directly proportional to the input resistance R_{in} and inversely proportional to the input capacitance C_{in}.

For the π-type matching network, the voltage gain is given by [8]

$$A_v = \sqrt{\frac{R_{in}}{R_s}} / \sqrt{1 + \frac{\omega_{RF} R_{in} C_{in} L}{Q_L L_p}} \tag{19}$$

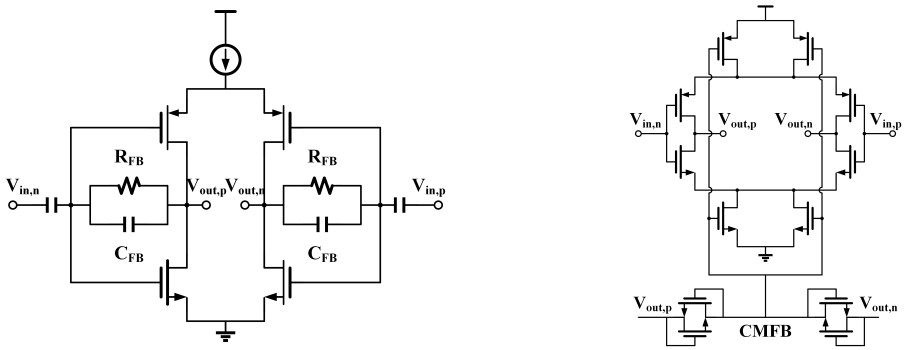
where L_p is part of the L, which is determined by the value of C_1 and C_2, and L.

As shown in (18) and (19), the inductor's quality factor plays an important role in determining gain. For RF envelope detection architectures, most designs operate at relatively low frequencies [9,28,31], with a few near 1 GHz or 2.4 GHz. Because of the simplicity of this architecture, on-chip matching networks would dominate the die area, which contradicts the low-cost objective. In addition, on-chip inductors typically exhibit low Q factors, as indicated by (10), (18) and (19), which can significantly degrade the sensitivity. Therefore, most implementations rely on off-chip inductors, where Q factors can commonly reach 80 or even exceed 100, thereby alleviating the sensitivity loss. In addition, larger R_{in} and smaller C_{in} values can significantly enhance passive voltage gain.

It is worth noting that in the previously discussed passive ED based on a Dickson charge pump, increasing the stage number N can enhance the ED's gain according to (13). However, as each ED stage is connected in parallel at the input port, the resulting decrease in input impedance (with increasing number of stages) reduces the passive gain. Consequently, an optimal stage number must be selected to maximize the overall gain.

4.2. Baseband Amplifier

Baseband noise significantly affects receiver sensitivity in low-power WuRX systems. This issue is particularly critical in ED-first architectures, where the output voltage of the ED is very small. Consequently, a low-power and high-gain BBA is required to amplify the signal for subsequent digital processing. The common-source amplifier, which satisfies these demands, is widely used. Typical gain values range from 30 to 60 dB, with current consumption in the nanoampere to microampere range. Figure 11a illustrates a typical current-reused differential common-source amplifier, where system gain and bandwidth can be tuned by adjusting the bias current [2].



(**a**) (**b**)

Figure 11. (**a**) Current-reuse differential common-source BBA and (**b**) bias-free BBA.

However, DC offsets in the BBA can arise from various sources, including mismatches in transistor parameters, process variations, and temperature fluctuations. These offsets can significantly degrade the performance of the WuRX system by introducing errors in the amplified signal, leading to false wake-up triggers or missed detections. Common-mode feedback (CMFB) circuits are employed to suppress these offsets. The simplest and most

efficient CMFB technique for WuRX systems uses resistor feedback, as shown in Figure 11a. However, due to the Miller effect, the resistance seen at the output is scaled down by a factor of $1/A_v$, where A_v is the open-loop gain of the BBA. If the feedback resistor R_f is too small, the closed-loop gain is significantly reduced. On the other hand, large resistors occupy excessive chip area.

To overcome this trade-off, a bias-free BBA using pseudo-resistors is proposed in [18]. The output common-mode voltage is regulated by a CMFB circuit connected to both PMOS and NMOS tails, ensuring stability over PVT variations without the need for a dedicated bias voltage V_B, as shown in Figure 11b. This design uses a diode-connected pseudo-resistor with an inverse polarity and a (W/L) ratio of 2 µm/100 nm to allow bidirectional conduction between the input and output nodes. This enables accurate voltage sensing for enhanced common-mode feedback. Since the DC offset of the ED is limited, the pseudo-resistor approximates an ideal resistor during normal operation. Compared to traditional approaches, additional PMOS transistors are used in the feedback loop to boost loop gain and improve both the DC operating point. Another advantage of this structure is the ability to use DC coupling, reducing $1/f$ noise and eliminating the need for large coupling capacitors which increase startup time and chip area.

Another approach involves active feedback to amplify and regulate the common-mode voltage, trading additional power consumption for better common-mode rejection, faster response, and improved PVT stability. Due to the low supply voltage, each transistor in the core circuit operates with a very limited drain-source voltage margin. Even when operating in the subthreshold region, this narrow margin makes the circuit sensitive to PVT variations. To address this, the low-voltage fast-response differential amplifier shown in Figure 12 is proposed [8]. It requires only $3 \times V_{DS}$ instead of $4 \times V_{DS}$ in the signal path, providing extra voltage headroom for each transistor to tolerate variations.

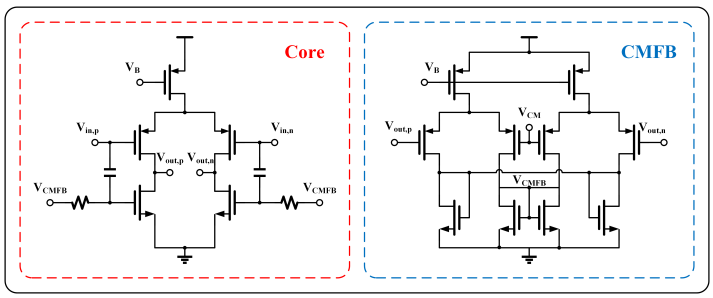


Figure 12. Low-voltage fast-response differential amplifier.

4.3. Correlator

After baseband amplification, the signal is digitized using either an ADC or a comparator. The correlator offers a low-power, low-cost, and easy-to-implement solution for detecting wake-up signal, without requiring a power-hungry PLL.

4.3.1. Digital Correlator

A typical architecture of a digital correlator is shown in Figure 13a [31,39]. An optimized 16-bit code sequence (1110101101100010) is designed such that it has a large Hamming distance from all its cyclic shifts ($D = 9$), as well as from the all-zero sequence ($D = 9$). Longer correlation codes (e.g., 63 bits versus 8 bits) yield higher coding gain, with up to 6 dB improvement in signal-to-noise ratio. The digital correlator samples the digitized input at a 2× oversampling rate and compares it to pre-stored codewords via bit-wise XNOR operations to calculate the Hamming distance. When the calculated Hamming distance falls below a predefined threshold, a wake-up signal is triggered.

To further improve the correlator's accuracy, MOSFETs can be used as loads, with each XNOR gate connected in series with an NMOS, as shown in Figure 13b [18]. The advantage of this structure is that the voltage output reaches a high level only when all XNOR gates output high. If any one of the XNOR outputs goes low, the corresponding MOSFET enters a low-impedance state (gate and drain tied), while the remaining MOSFETs enter a high-impedance state (gate and source tied). As a result, the voltage fed to the comparator is limited to the MOSFET threshold voltage, ensuring that only near-perfect matches produce a wake-up trigger. Compared to conventional correlators that may tolerate Hamming distances close to half the number of code bits [31], this structure significantly reduces the MDR.

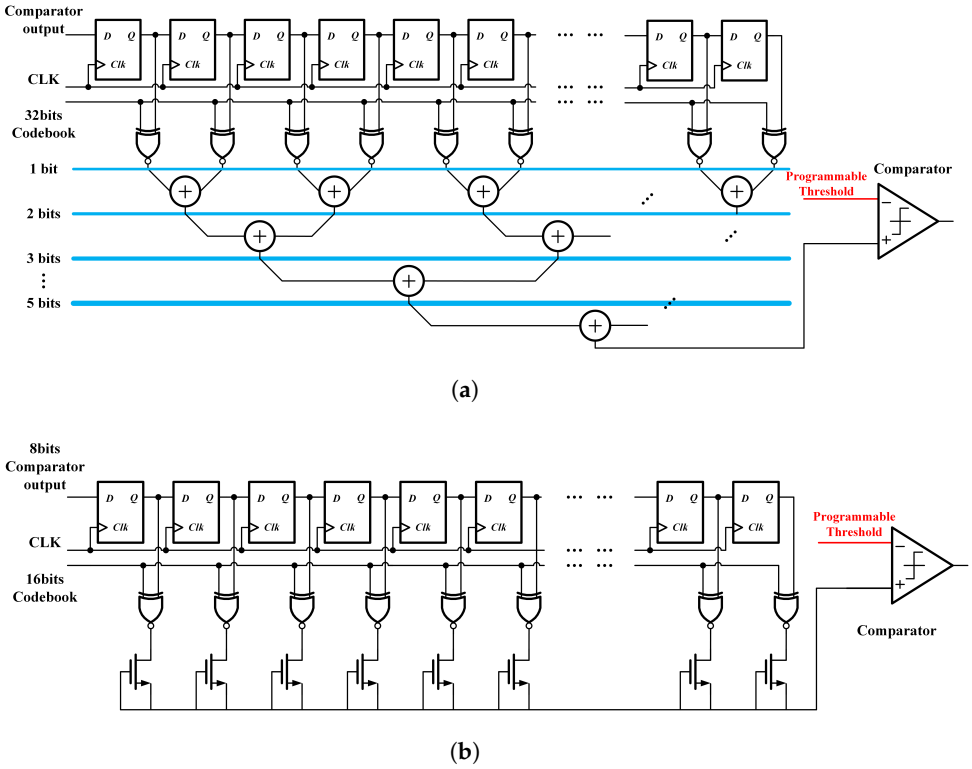


Figure 13. (**a**) Conventional Digital Correlator and (**b**) digital Correlator with MOSFET loads.

However, this design still requires a 2× clock for oversampling. Manchester coding can be employed to recover both data and clock from the same bit-stream, trading off data rate for simplified synchronization with 1× clock [40]. While this slightly increases the complexity of the digital correlator, it simplifies the overall WuRX system architecture.

4.3.2. Analog Correlator

Digital circuits such as correlators and ADCs typically rely on local oscillator such as crystal oscillator or other external references. However, those circuits introduce unnecessary standby power consumption, increases system size and cost, and imposes additional constraints on integration due to the need for an external reference.

To achieve the goal of truly always-on, ultra-low-power listening, analog correlators becomes promising approaches. They inherently suppress undesired AM interference and can support simultaneous wake-up in CDMA-based networks using orthogonal codes. An asynchronous, clockless WuRX architecture based on leakage-powered analog correlation is proposed in [41]. As illustrated in Figure 14, the proposed design eliminates the need for any continuously running clock source by leveraging a passive analog circuit that

performs correlation without time-domain sampling. The input signal is processed through a delay chain, where each stage is tuned to match half of the signal period. The resulting parallel signal stream is then fed into combinational logic that detects a wake-up pattern. Upon a successful match, a wake-up signal is generated.

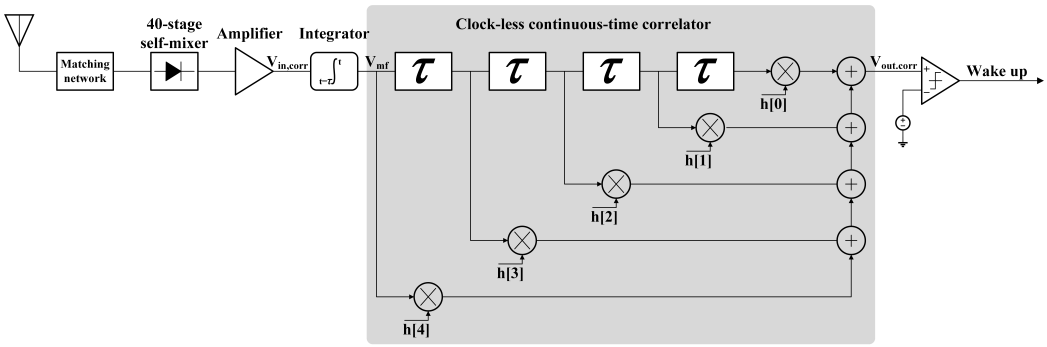


Figure 14. A WuRX architecture with analog correlator.

However, if the delay stages are not precisely calibrated, due to inaccurate tuning of the control voltage V_{tune}, the delay per stage deviate from the ideal value. This mismatch leads to timing skew between delayed signal taps and causes distortion of the expected bit pattern, ultimately degrading detection reliability. A phase detector-based auto-tuning clockless WuRX is shown in Figure 15 [42]. The mechanism continuously monitors the phase difference between the delayed signal Q_3 and the reference input data. Any deviation from the ideal timing results in a control signal that adjusts the bias voltage V_{tune} applied to a current-starved delay cell.

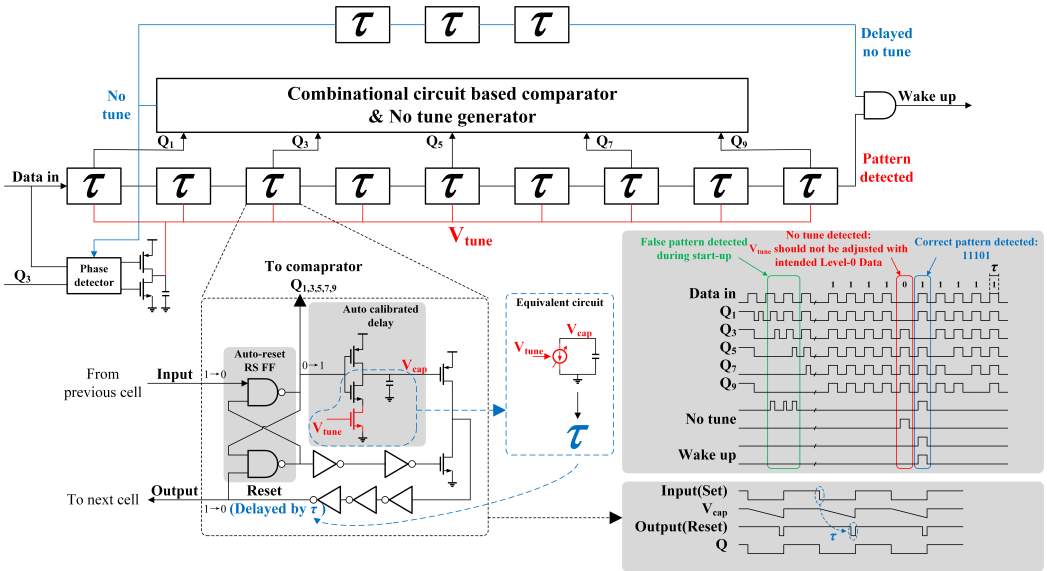


Figure 15. Asynchronous clockless WuRX.

It passively adjusts the signal propagation speed through the delay chain to align with the incoming signal frequency. The result is a self-adaptive delay line that remains synchronized with the data stream over time, without the need for external references or continuous calibration. However, the phase detector falsely trigger even during correct system operation when input data = 0 and Q_3 = 1, despite the correlation sequence being valid. To avoid this, an additional combinational logic block is used to match the expected bit pattern and assert a no-tune signal, which temporarily disables the phase detector under these conditions. The no-tune signal can also serve as a correlation. After appropriate delay alignment, it can be jointly evaluated with the pattern detection to control the final wake-up

signal. This dual use of the signal further reduces the probability of false wake-up events and improves system reliability.

However, analog implementations are more complex than digital ones and exhibit higher timing error rates. Additionally, although analog correlators do not require a clock, their inherent power consumption is often higher than that of digital correlators. (e.g., 11-bit analog correlators may consume up to 37 nW).

5. Key Techniques in On-Chip LO Architectures

On-chip LO WuRXs use a local oscillator to downconvert the RF signal to a baseband or IF frequency. While more power-hungry than RF envelope detection and transmitted-LO architectures, on-chip LO WuRXs offer better sensitivity and interference rejection.

For OOK modulated signals, the ED inherently discards frequency and phase information during demodulation. However, the transmitted data can still be accurately recovered as long as the downconverted signal resides within the ED's IF bandwidth. This tolerance relaxes the precision requirements for the VCO clock frequency, enabling significant power savings compared to PLL-based systems.

5.1. N-Path Mixer

Figure 16 demonstrates a four-phase passive mixer architecture directly interfaced with the antenna. This topology employs four MOS switches controlled by non-overlapping 25% duty-cycle clock signals, sequentially activated with 90° phase offsets. The mixer transistors are characterized as ideal switches incorporating a minimal series resistance R_{SW}. Each switch is loaded with a capacitor, C_L, and a resistive load R_L, forming a first-order RC network. This non-overlapping characteristic ensures singular conduction paths between the antenna port and load network at any instant, enabling equivalent circuit simplification where the four parallel switch resistances coalesce into a single effective resistance [24,43,44].

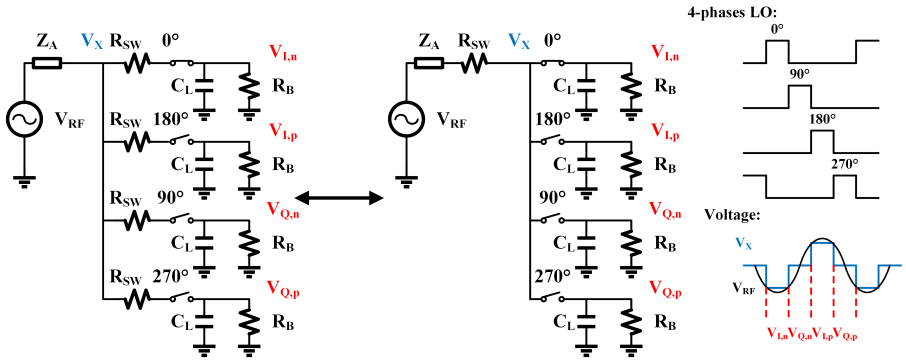


Figure 16. A four-phase passive mixer architecture.

During respective LO activation phases, the RF input voltage V_{rf} is sampled onto each corresponding capacitor, establishing four discrete steady-state voltage levels correspond to differential and down converted baseband signals. If the time constant ($\tau = R_L C_L$) of RC network is much larger than the frequency of *LO* signal, it can be approximately considered that the charge on the capacitor remains unchanged in a switching cycle.

Increasing the number of paths N in an N-path mixer can enhance the frequency selectivity, resulting in a steeper filter response and stronger out-of-band rejection, thereby effectively suppressing adjacent-channel interference. However, a primary limitation arises from the $1/N$ duty cycle requirement for LO signals in N-phase mixers. As N increases,

the reduced duty cycle significantly elevates clock circuitry complexity. Another critical limitation stems from the mixer's input impedance (Z_{in}) which will be discussed later.

The N-path mixer directly interfaces with the antenna, requiring impedance matching to the impedance of antenna Z_a, normally 50 Ω. The equivalent impedance of the structure consists of two parallel components: the harmonics-transformed resistance R_{sh} and the impedance-transformed resistance R_B, as shown in the Figure 17. Therefore, the input impedance is

$$R_{in} = R_{sw} + \gamma R_B || R_{sh} \tag{20}$$

$$R_{sh} = \gamma_{sh}(R_{sw} + Z_a) \tag{21}$$

For N-path mixers, γ and γ_{sh} are

$$\gamma = N\frac{\sin^2(\frac{\pi}{N})}{\pi^2} \tag{22}$$

$$\gamma_{sh} = \frac{N\gamma}{1 - N\gamma} \tag{23}$$

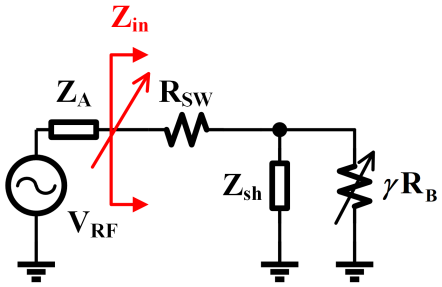


Figure 17. The equivalent impedance of the N path mixer.

According to (20), the input impedance can be tuned by adjusting the switch resistance R_{sw} and load resistance R_B. However, as the N increases, the γ coefficient decreases while the r_{sh} coefficient in Z_{sh} rises rapidly. For $N = 4$, $r = \frac{2}{\pi^2}$, $r_{sh} \approx 4.3$. For $N = 8$, $r = \frac{2-\sqrt{2}}{\pi^2}$, $r_{sh} \approx 18.9$ and Z_{sh} exceeds 945 Ω. Therefore, impedance matching to Z_A (50 Ω) relies on adjusting R_{sw} and R_B, for large N. This constrains R_B to small resistance values. As previously established, the time constant $\tau = R_B C$ must be sufficiently large to maintain nearly constant capacitor voltage during switch-off periods. With small R_B values required for impedance matching, impractically large capacitors C would be needed. This approach presents practical challenges for cost-sensitive, area-constrained WuRX designs, where implementing such large capacitors may not be the most optimal solution. In the "LNA-First" architecture, the LNA's output resistance may exceed the antenna impedance. This characteristic allows for slight relaxation of the mixer stages.

5.2. Clock Generation

In on-chip WuRX architectures, the local oscillator (LO) plays a critical role in enabling frequency downconversion. Since reusing the main receiver's LO would result in excessive power dissipation, WuRX designs typically require a dedicated, ultra-low-power LO for always-on operation. While LC-based VCOs (LC VCOs) in [10] are common in traditional coherent receivers, their high power consumption makes them less suitable for WuRX applications. For systems using low intermediate frequencies (IF) and non-coherent demodulation, the phase noise requirement can be relaxed to around −80 dBc/Hz at 1 MHz offset [45], reducing the need for high-performance oscillators. Therefore, ring oscillators

(ring VCOs) are widely adopted in WuRX designs due to their simple architecture and significantly lower power consumption compared to LC VCOs [26,46]. Figure 18 shows a 3-stage differential ring VCO used for a 6-path mixer mentioned in Section 5.1. The oscillator's coarse and fine-tuning are controlled by 5-bit and 6-bit resistive arrays, respectively, enabling a tuning slope (K_{VCO}) of 320 kHz/mV while maintaining a wide frequency range and strong PVT robustness. Ring VCOs for frequency downconversion in WuRXs typically operate with power consumption ranging from 20 to 80 µW.

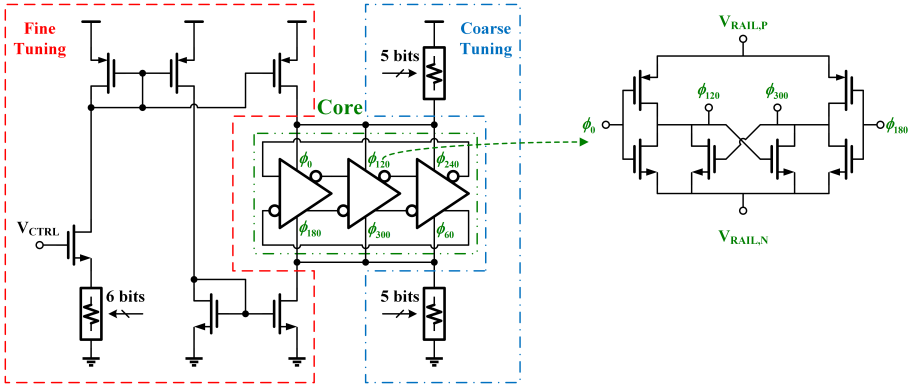


Figure 18. Ring VCO.

For digital baseband timing, particularly in systems with always-on correlators, various ultra-low-power oscillator topologies have been explored. Prior works [7,35] employ a ring oscillator operating between 100 Hz and 10 kHz to clock the digital baseband, consuming only 0.3 nW. In a different approach, a relaxation oscillator is implemented using a comparator with complementary to absolute temperature (CTAT) delay and an RX core with proportional to absolute temperature (PTAT) behavior to achieve temperature compensation [47]. This design achieves 94 ppm/°C frequency stability while operating at 1.22 kHz with a power consumption of just 1.14 nW. A 32-kHz crystal oscillator based on sub-harmonic pulse injection is proposed in [10], consuming only 0.74 nW from a single 0.3 V supply. It employs a slicer, delay-locked loop (DLL), and pulse driver to efficiently inject energy at sub-harmonic intervals, eliminating the need for PLLs or multi-domain biasing circuitry. These designs demonstrate that ultra-low-power clock generation in the sub-kHz to tens-of-kHz range is feasible, making them ideal for clocking WuRX digital correlators and control logic without compromising energy efficiency.

In conventional receivers, a stable LO with low phase noise is essential and typically achieved using a PLL to lock a VCO. However, PLLs are not mandatory in WuRX designs. Since WuRXs often do not adhere to existing communication protocols, requirements on phase noise and signal-to-interference ratio (SIR) are generally relaxed, allowing designers to omit the PLL in favor of simpler solutions. Free-running oscillators eliminate the need for locking circuits, further reducing power consumption. However, they require a wider IF bandwidth to compensate for frequency drift. For example, in systems using frequency multiplication, a 1 MHz frequency offset in the VCO could necessitate an additional 5 MHz or more of IF bandwidth to ensure proper signal reception. This broader bandwidth also increases the noise seen at the input of the ED, potentially degrading overall system sensitivity, mentioned in Section 4.1. Nevertheless, PLLs remain necessary in WuRX systems that require precise frequency tracking across wide temperature or voltage ranges, or in scenarios where synchronization with external devices is required. This includes wake-up schemes based on BLE or Wi-Fi beacons, where and narrowband operation are essential to reject channel interference, which is not suitable for uncertain IF. In such cases, the PLL provides long-term frequency stability and accurate downconversion. Despite

these benefits, PLLs introduce extra power overhead and startup latency, which may conflict with the ultra-low-power budgets of WuRX systems. As a result, PLLs are typically reserved for WuRX architectures that demand strict frequency accuracy, rather than being considered a standard component.

6. Key Techniques in Transmitted-LO Architectures

Transmitted-LO WuRXs use a two-tone signal to downconvert the RF signal to the IF signal using the nonlinearity of the ED. This approach allows for better interference rejection compared to RF envelope detection architectures, as the desired signal can be filtered at the IF.

6.1. Two-Tone Modulation

By converting the RF signal into a two-tone OOK waveform and subsequently demodulating it using an ED, the received signal can be effectively shifted to IF signal [24,25,48]. As shown in Figure 3, an original two-tone WuRX architecture is illustrated alongside its frequency-domain representation. In this structure, the transmitter simultaneously emits both the RF carrier and a local oscillator (LO) tone. The two-tone waveform can be expressed as [48]

$$V_{2\text{-}tone} = \frac{A}{\sqrt{2}}[\cos(2\pi f_c t + \phi_1) + \cos(2\pi(f_c + \Delta f)t + \phi_2)] \tag{24}$$

where A is the peak-to-peak amplitude of the signal, Δf is the frequency spacing of the two tones, $\phi 1$ and $\phi 2$ is the random phase offsets. The ED at the receiver mixes these two signals, producing a beat frequency at the IF. A bandpass filter can then isolate the desired signal while suppressing in-band interference and 1/f noise. According to (3), the output of ED (and BPF) can be written as

$$V_{2\text{-}tone,IF} = \frac{kA^2}{2}[\cos(2\pi\Delta f t + \phi_1 - \phi_2)] \tag{25}$$

This is treated as the desired signal because it preserves the relative frequency information and operates at a frequency well-suited for power-efficient IF circuit stages. A second-stage can then be used to downconvert the signal to baseband for quantization and digital processing. A -90 dBm sensitivity is achieved using this approach with 19 µW power and -46 dB SIR [17].

6.2. CE-OOK

CE-OOK is another variation of the two-tone scheme as shown in Figure 19 [20,21,23]. Unlike the original two-tone structure, CE-OOK applies a BFSK-pre-modulated IF signal to modulate the RF carrier using OOK. The CE-OOK waveform in each channel can be expressed as [4]

$$V_{CE\text{-}OOK} = A\cos(2\pi f_c t)[Sq(t) + 1] \tag{26}$$

where $Sq(t)$ is a square signal with a unity amplitude and frequency of f_Δ. By applying a Fourier series expansion to (26), followed by squaring through the ED and subsequent filtering, the resulting IF signal can be expressed as [4]

$$V_{CE\text{-}OOK,IF} = \frac{4kA^2}{\pi}[\cos(2\pi f_\Delta t)] \tag{27}$$

Mathematically, CE-OOK produces an IF signal that is 2 dB stronger than that of conventional two-tone OOK as shown in (25). This leads to an improved SNR and enables a simpler transmitter implementation due to the use of a single, constant-envelope carrier.

MC-OOK is an extended OOK modulation scheme based on the OFDM structure for low-power wake-up functionality compatible with Wi-Fi systems [11,16]. It represents "1" and "0" bits by selectively activating or deactivating OFDM subcarriers, enabling subcarriers for a "1," and disabling all subcarriers for a "0." With Manchester encoding, MC-OOK improves timing recovery and significantly relaxes LO frequency accuracy requirements. Compared to original CE-OOK, MC-OOK is easier to integrate with Wi-Fi transmitters, offers stronger interference resilience, requires lower SNR (as low as 0 dB), and achieves high sensitivity (−92.6 dBm) under ultra-low-power conditions [16]. It serves as a practical and performance-enhanced extension of CE-OOK for Wi-Fi compatible WuRX systems.

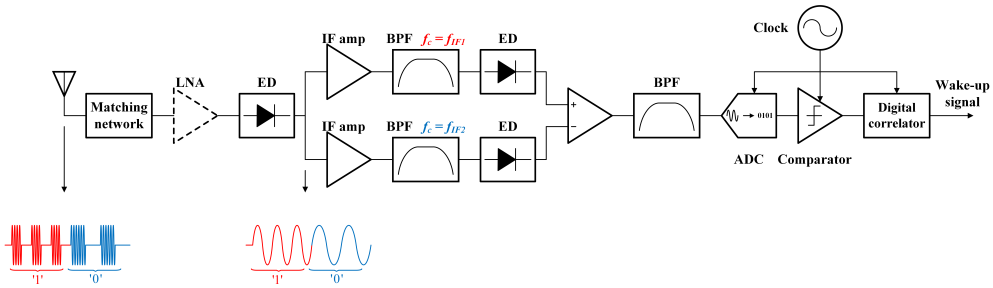


Figure 19. Illustrations of the CE-OOK WuRX.

6.3. Spread-Spectrum

Recent studies [24,36,37] have extended the two-tone architecture by introducing a spread-spectrum transmitted-reference modulation scheme as shown in Figure 20, which improves interference resilience. A spreading sequence is generated, and a frequency-shifted replica modulated with the data is produced. Both the unmodulated and modulated sequences are transmitted simultaneously to RX. Both the original and modulated versions are then transmitted concurrently. After demodulation via the ED, the desired signal is recovered at the IF, while the interferer signals are pushed further away in the frequency domain, resulting in improved signal isolation and enhanced SIR.

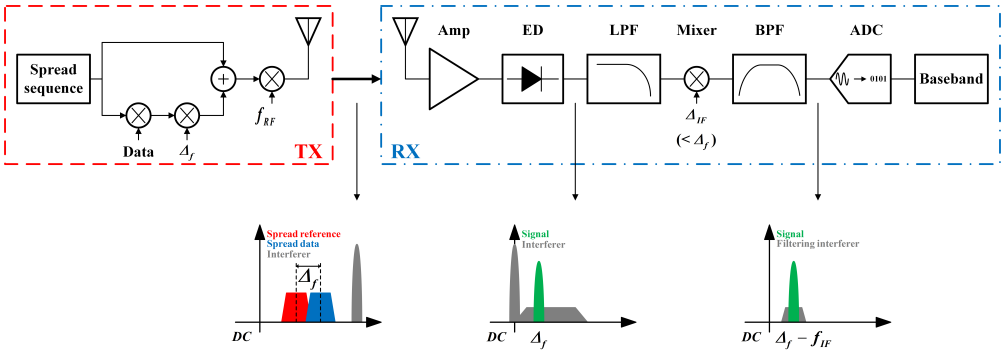


Figure 20. Illustrations of the spread-spectrum transmitted-reference wake-up system with signal spectrum.

The dual-chirp OOK (DC-OOK) as shown in Figure 21 combines the advantages of spread spectrum modulation and dual-tone modulation [37]. This technique employs two linear chirp signals with different starting frequencies and slopes to represent the "1" symbol, which are downconverted to a low-frequency chirp IF signal through self-mixing. The IF signal is then converted into a baseband OOK signal. This design retains the low-power advantages of traditional dual-tone modulation while achieving spread

spectrum processing gain through the wideband spectrum of chirp signals, resulting in excellent anti-interference performance in the 430 MHz ISM band. Experimental results demonstrate that this technology achieves high sensitivity of −103 dBm and can suppress AM interference up to 41 dBc at a 10 MHz frequency offset with consuming 110 µW.

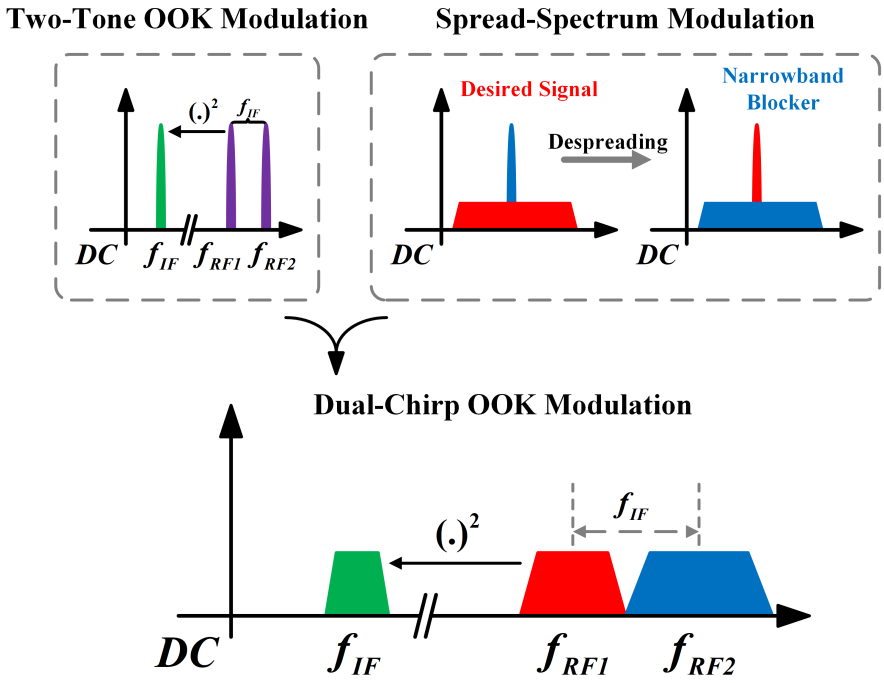


Figure 21. Illustration of the DC-OOK modulation.

7. Other Techniques for Wake-Up Receivers

7.1. Duty Cycling

Duty cycling is a common technique to reduce power consumption in WuRXs. By periodically turning off the receiver, duty cycling can significantly reduce average power consumption. However, this comes at the cost of increased latency, as the receiver may miss wake-up signals during the off periods.

Bit-level duty cycling (BLDC) as shown in Figure 22 involves turning on the receiver for a fraction of each bit period [21,23,32]. This technique reduces power consumption but requires careful synchronization to avoid missing wake-up signals.

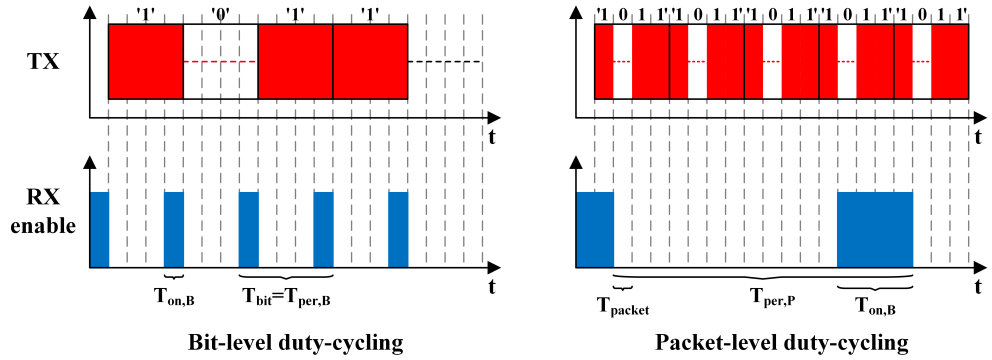


Figure 22. Illustration of bit-level duty cycling (BLDC) and packet-level duty cycling (PLDC).

Packet-level duty cycling (PLDC) as shown in Figure 22 involves turning on the receiver for entire packets, reducing the need for frequent synchronization [22]. This approach is more power-efficient than BLDC but requires longer wake-up times.

According to [4], the minimum BB bandwidth requirements for BLDC and PLDC can be derived as

$$BW_{BLDC} = \frac{0.35}{T_{on,B}} \tag{28}$$

$$BW_{PLDC} = \frac{1}{T_{on,P}} \tag{29}$$

The power dissipation under BLDC and PLDC can be written as follows:

$$P_{BLDC} = P_{inst}\frac{T_{on,B}}{T_{per,B}} \tag{30}$$

$$P_{PLDC} = P_{inst}\frac{T_{on,P}}{T_{per,P}} \tag{31}$$

where P_{inst} is the instantaneous power, and $T_{on,B}/T_{per,B}$ is almost equal to $T_{on,P}/T_{per,P}$.

Therefore, BLDC requires only one-third the bandwidth of PLDC, which gives BLDC the advantages of lower latency and higher sensitivity. However, the narrower sampling window of BLDC also introduces issues such as DC offset and spectral leakage. Moreover, for ultra-narrowband downconversion receivers, employing BLDC demands exceptionally high clock accuracy. This not only increases system complexity but also contradicts the low-power design requirements.

7.2. Chopper

EDs in WuRX architectures are particularly susceptible to 1/f noise, which significantly limits receiver sensitivity. Chopper techniques are widely adopted to mitigate this issue. A synchronized-switching envelope detection receiver is proposed in [49,50] to suppress 1/f noise and enhance sensitivity. This architecture is more accurately associated with chopper stabilization (CHS) rather than correlated double sampling (CDS) as commonly used in analog signal processing.

As illustrated in Figure 23, a chopper is inserted at the input of the ED. In the frequency domain, this chopper shifts the signal to odd harmonics of the switching frequency f_{ss}, creating sidebands centered at f_{ss} and its multiples. Due to the squaring operation inherent in ED, the signal content appears at f_{ss} rather than DC. After amplification, a second chopper modulates the signal back to DC, while flicker noise and DC offsets are now upshifted to f_{ss}, where they can be effectively suppressed by an LPF. This technique thus enhances signal integrity by reducing the impact of low-frequency noise components.

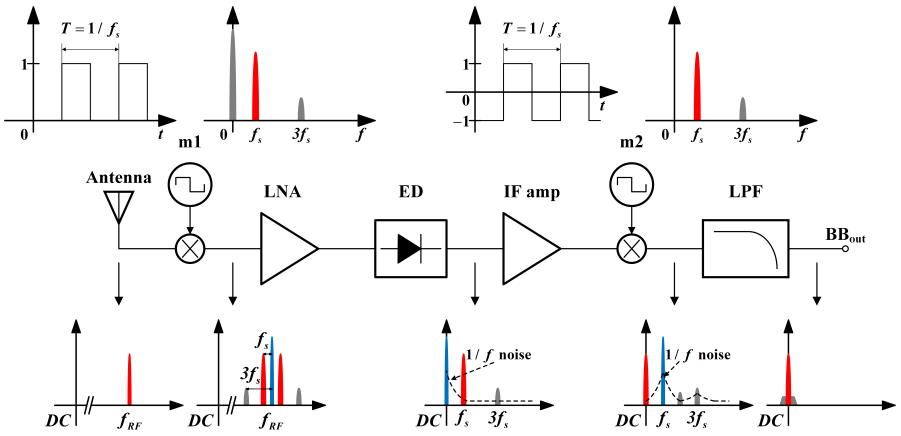


Figure 23. Illustrations of the synchronized-switching envelope detection receiver with signal spectrum.

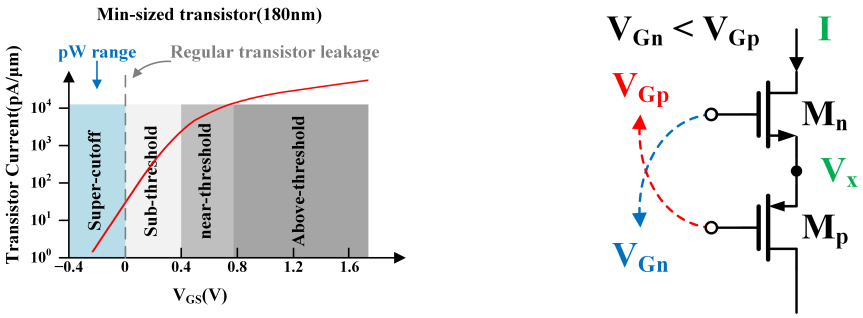
8. Frontiers of Wake-Up Receiver Design

In the previous sections, we presented commonly adopted architectures and design styles for WuRXs, which have been proven sufficient for most application scenarios. However, ongoing research continues to push technological boundaries to address new challenges such as lower power consumption and higher operating frequencies.

8.1. Super-Cutoff Operation

The power consumption of current WuRX designs depends on their intended application and ranges from nanowatts to microwatts, with only a few architectures capable of achieving sub-nW levels, down to a few hundred picowatts. In purely harvested systems, particularly under fluctuating environmental conditions—such as light-harvested power in near-dark conditions (e.g., 100 pW/mm^2 as available from a solar cell at near-dark)—a significantly lower power budget is required to ensure stable operation.

Most mainstream WuRX implementations rely on MOS transistors operating in the subthreshold region. However, as shown in Figure 24a, even when $V_{GS} \approx 0$, individual MOS transistors still exhibit leakage currents close to 10 pA. Although lowering V_{GS} below zero could theoretically yield even smaller currents, this would require negative biasing, which in turn increases circuit complexity.



(**a**) (**b**)

Figure 24. (**a**) Power range explored in [40] lies in the region where transistors operate in the super-cutoff region. (**b**) NMOS-PMOS stack.

An innovative NMOS-PMOS stack structure is proposed to effectively achieve $V_{GS} < 0$ operation without the need for voltages outside the supply rails [40], as illustrated in Figure 24b. The current of this structure is

$$I = I_{0,N} e^{\frac{V_{GN} - V_x - V_{TH,N}}{nkt/q}} = I_{0,P} e^{\frac{V_x - V_{GP} - |V_{TH,P}|}{nkt/q}} \tag{32}$$

where, I_0 is a process-dependent constant depended on the parameters such as the transistor width-to-length ratio (W/L). V_{TH} denotes the threshold voltage, n is the subthreshold slope factor (assumed identical for both NMOS and PMOS transistors), and kT/q is the thermal voltage. The expression for current assumes that the exponential term $1 - e^{-V_{DS}/(kT/q)}$ approaches unity, which holds when $V_{DS} \geq 4kT/q \approx 100$ mV. When the sizes of NMOS and PMOS transistors are selected so that $I_{0,N} = I_{0,P} = I_0$, and assuming the same threshold voltages (i.e., $V_{TH,N} \approx |V_{TH,P}| \approx V_{TH}$), the intermediate node voltage V_x becomes the average of the two gate voltages $\frac{V_{GN}+V_{GP}}{2}$ and (32) can be rewritten as

$$I = I_0 e^{\frac{\frac{V_{GN} - V_{GP}}{2} - V_{TH}}{nkt/q}} \tag{33}$$

As long as $V_{GN} < V_{GP}$, the NMOS-PMOS stack can be equivalently modeled as an NMOS transistor with the $V_{GS} < 0$. By replacing conventional transistors with the proposed

NMOS-PMOS stack structure, Basu et al. [40] reconstructs several standard analog building blocks. Such as super-cutoff current mirror, operational transconductance amplifier (OTA), and comparator are shown in Figure 25.

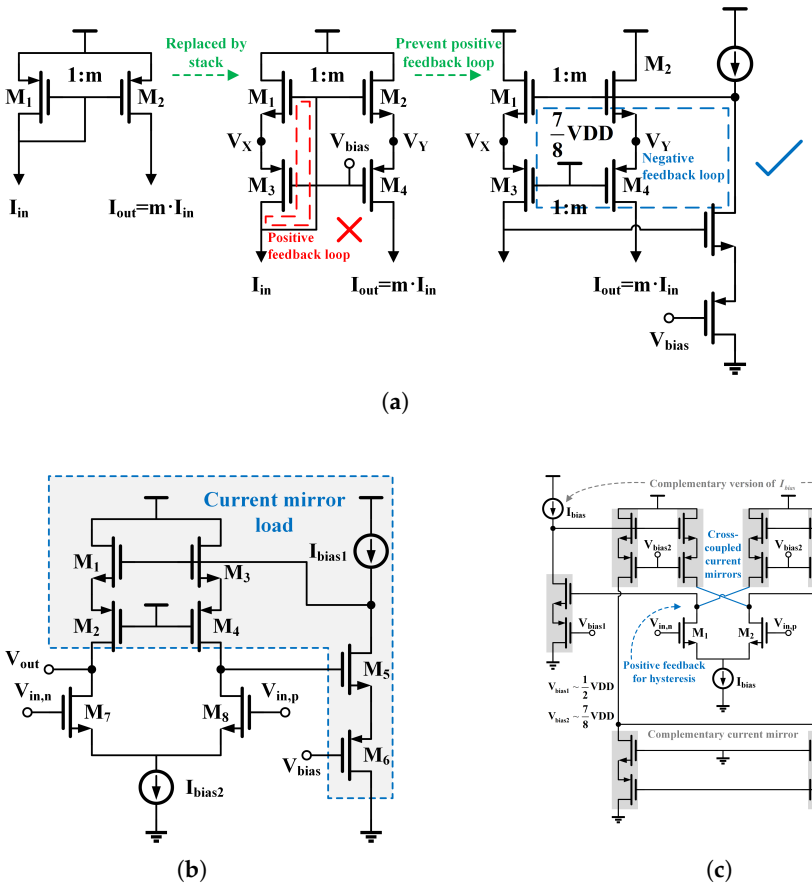


Figure 25. Reconstructed analog building blocks (**a**) super-cutoff current mirror (**b**) super-cutoff OTA (**c**) super-cutoff comparator.

The resulting WuRX as shown in Figure 26, based entirely on super-cutoff transistor stacks, achieves an ultra-low power consumption of just 78 pW at room temperature. Remarkably, this power level can be fully sustained by a 1 mm^2 solar cell even under extremely low illumination levels of 1 lux (i.e., moonlight), enabling nearly 100% uptime without any energy storage. Under indoor lighting conditions of 450 lux, with a 2 W LED source placed 1 m away, the system achieves a bit error rate (BER) better than 10^{-3}. These results demonstrate a promising new class of silicon systems characterized by ultra-low power operation and near-continuous availability, paving the way for battery-less, and environmentally sustainable sensing platforms.

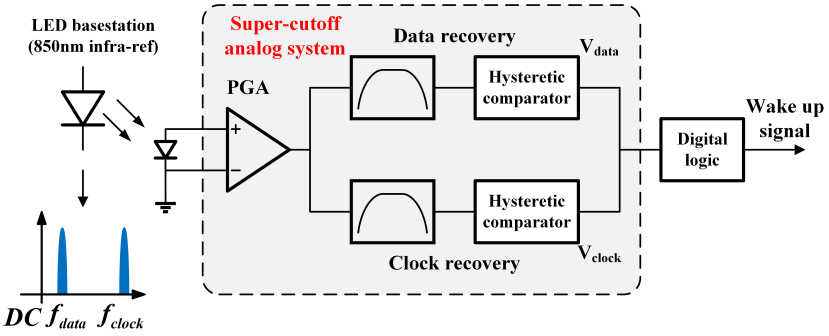


Figure 26. The LiFi optical WuRX system.

8.2. Sub-THz Wake-Up Receiver

Conventional WuRX designs typically operate in the sub-GHz to low-GHz range. While these systems offer notable energy efficiency, their physical size is fundamentally constrained by the antenna dimensions, which scale with wavelength and often reach the cm^2 level. This limitation hinders integration into ultra-miniaturized platforms, especially for applications demanding stealth, mass deploy ability, or implantable form factors. To overcome this bottleneck, the sub-terahertz (sub-THz) spectrum offers several key advantages: its shorter wavelength enables compact on-chip antenna integration, highly directional beams, and enhanced spatial selectivity. These characteristics make sub-THz an ideal candidate for achieving extreme miniaturization in next-generation WuRX systems.

The fully integrated WuRX operating at 264 GHz in the sub-THz band is demonstrated in [51], as illustrated in Figure 27. A key innovation in this work lies in the dual-antenna-driven THz detector architecture, which departs from the conventional single-antenna topologies used in most RF and THz WuRX systems. Traditional designs typically couple both gate and drain terminals of a detector transistor to a single antenna, resulting in limited control over signal amplitude and phase at each terminal. In conventional GHz-band circuits, this structure introduces only minor phase variations. However, in the sub-THz band, the metal trace lengths become comparable to the signal wavelength. As a result, distributed modeling must be employed, leading to significant phase shifts that can critically affect device matching and detection efficiency.

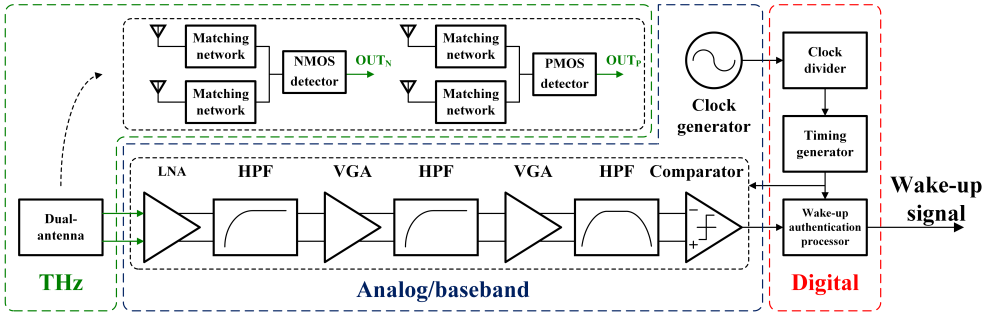


Figure 27. The sub-THz WuRX.

A pseudo-differential dual-antenna detector is employed in this WuRX, as shown in Figure 28, in which two independently sized patch antennas separately drive the gate and drain of a cold-biased FET (cold-FET), allowing fine-tuned control over the power split and relative phase. The optimal rectification occurs when the amplitude ratio $|v_{ds}/v_{gs}| = 4.5$ and the phase difference $\angle(v_{ds}/v_{gs}) = 170°$.

By using antennas with carefully engineered aperture widths W_G and W_D, the power received at the gate P_G and drain P_D terminals achieves the desired ratio, enabling the maximization of voltage responsivity R_v. Matching networks are separately designed for each terminal. This dual-antenna configuration also improves spatial selectivity and reduces vulnerability to ambient interference, as it creates a more directive and precisely aligned electromagnetic field interaction at the transistor terminals. Furthermore, its pseudo-differential nature mitigates comparator kickback noise and enhances common-mode rejection. Overall, this architecture exemplifies a powerful design paradigm for achieving highly efficient, scalable, and miniaturized THz WuRX front ends.

Implemented in 65-nm CMOS, the system occupies only 1.54 mm^2 without antenna. The detector achieves a responsivity of 2.4 kV/W and a minimum noise-equivalent power (NEP) of 10.5 $pW/Hz^{1/2}$. The measured sensitivity of the overall system is -48 dBm at a data rate of 1.02 kb/s while consuming 2.9 µW in continuous operation, achieving a BER of 10^{-3}. Furthermore, the system supports beam-steerable THz communication

using an electrically controlled reflect array. Experimental results demonstrate successful wake-up at 0°, 15°, and 30° with angular radar imaging and spectral verification.

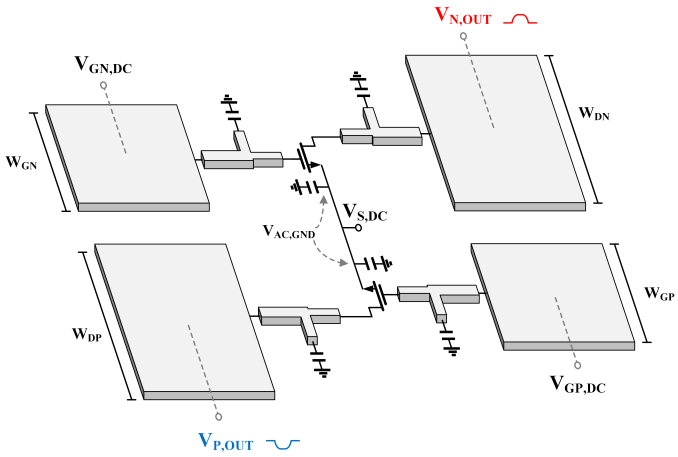


Figure 28. Pseudo-differential dual-antenna.

Overall, this work pushes the frontier of WuRX design by combining extreme miniaturization, high-frequency operation, and integrated hardware security—highlighting the emerging role of sub-THz technologies in battery-less wireless sensing.

8.3. Bi-Directional Communication with Backscatter Modulation

Backscatter modulation enables wireless communication without the need for active RF transmission. By controlling the impedance at the antenna port, it reflects and modulates incoming signals from ambient or dedicated RF sources, thereby drastically reducing power consumption [52,53]. Backscatter techniques have already been widely applied in the past. Figure 29 illustrates the operating principle of a radio frequency identification (RFID) tag, which is a typical backscatter system. Such structures can operate over a frequency range of 0.4 to 2.4 GHz and support communication distances of up to several meters.

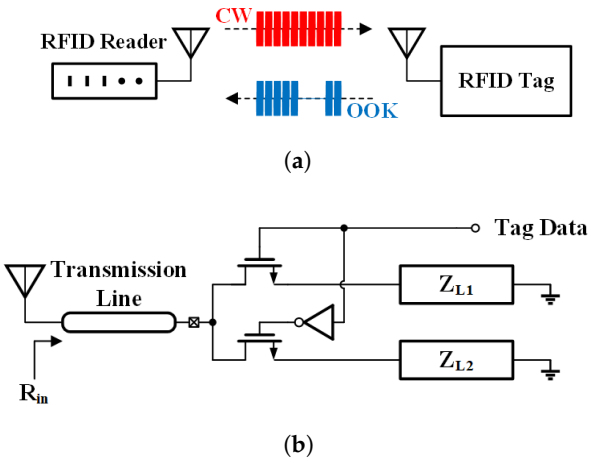


Figure 29. (**a**) RFID tags. (**b**) Methods to perform OOK backscatter modulation in RFID tags.

When combined with WuRX, backscatter modulation can achieve ultra-low-power always-on listening, while activating the backscatter communication module only upon detection of a valid wake-up signal. Figure 30 illustrates the bi-directional communication between wireless interfaces and IoT devices with a low power backscatter tag, which is designed to operate with minimal power consumption. Since backscatter communication modulates incident RF signals purely by adjusting reflection characteristics, it eliminates the

need for conventional RF transmission and significantly extends device lifetime. A Wi-Fi compatible system proposed in [52], shown in Figure 31, the WuRX continuously monitors Wi-Fi beacon packets with only 2.8 µW of power consumption. Upon successful detection, a crystal-based local oscillator drives a backscatter modulator to perform QPSK modulation, enabling compliant communication with standard Wi-Fi access points. This approach offers a scalable solution for future large-scale, energy-constrained wireless systems by balancing protocol compatibility, low latency, and high energy efficiency.

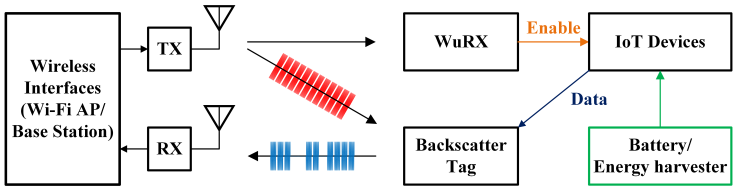


Figure 30. Bi-directional communication with a low power backscatter tag.

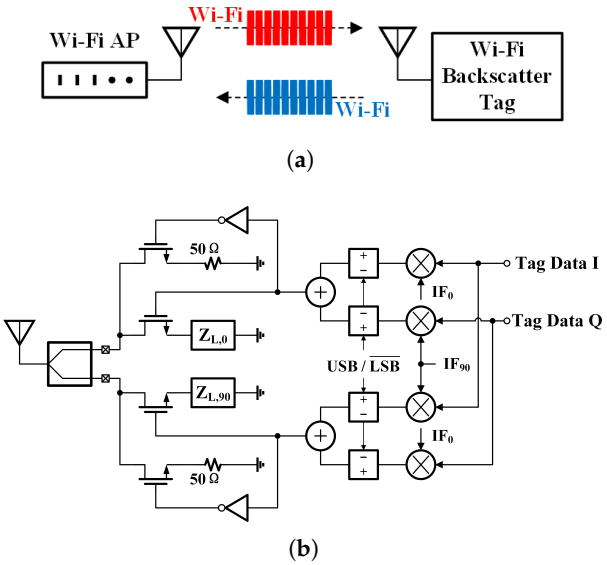


Figure 31. (**a**) Wi-Fi compatible backscatter tags. (**b**) Methods to perform QPSK backscatter modulation in Wi-Fi compatible backscatter tags.

9. Figure-of-Merit for Wake-Up Receivers

Power consumption is a critical metric for WuRX due to its continuous operation and reliance on limited energy sources. Sensitivity is equally crucial as it determines the communication range and thus the supported applications. Additionally, data rate serves as a critical performance metric that significantly impacts both interference immunity and latency in WuRX systems. For the various WuRX architectures mentioned earlier, each involves distinct trade-offs across these three aspects. Therefore, it is necessary to establish standardized metrics for quantitative comparison. Fundamentally, a receiver's core function is to extract useful signals from noise. Therefore, we can develop evaluation criteria based on noise characteristics. In circuit design, noise typically shows an inverse linear relationship with current. Consequently, sensitivity and power consumption can be normalized using the following expression:

$$FoM_{SEN,power} = -P_{SEN} - 10\log\frac{P_{dc}}{1mW} \tag{34}$$

The study in [5] identifies two primary noise sources in receiver front ends: in-band RF channel noise and baseband circuit noise. Notably, the former undergoes further

decomposition after the ED, resulting in two distinct components: self-mixed noise and the noise generated by mixing with the input signal.

All three noise components exhibit strong bandwidth dependence. As shown previously in (8) and (9), when the RF bandwidth (BW_{RF}) is much larger than the baseband bandwidth (BW_{BB}), the system noise is dominated by noise self-mixing, and the resulting SNR is primarily governed by the term $\sqrt{BW_{BB}}$. In contrast, when BW_{RF} is not significantly greater than BW_{BB}, noise–signal mixing becomes the dominant noise source, and the SNR scales more directly with BW_{BB} itself. To more precisely determine the boundary between the two regimes, equating (8) and (9) yields

$$BW_{RF} = 16 BW_{BB} SNR_{min} \tag{35}$$

According to [5,15,54], the minimum required SNR_{min} for OOK modulation is approximately 10–12 dB. Based on this, it can be derived that when the RF bandwidth satisfies $BW_{RF} \approx 200 \times BW_{BB}$, the contributions of noise self-mixing and noise–signal mixing to system sensitivity are approximately equal. Therefore, when $BW_{RF} < 20 \times BW_{BB}$, the system sensitivity is primarily determined by (8), indicating dominance of noise–signal mixing. Conversely, when $BW_{RF} > 2000 \times BW_{BB}$, sensitivity is governed by (8), where noise self-mixing dominates. In the intermediate region, both noise mechanisms must be considered simultaneously to accurately predict system performance.

It can be observed in (10) that the baseband noise also scales linearly with $\sqrt{BW_{BB}}$. Furthermore, as the pre-ED gain increases, the impact of baseband noise on overall system sensitivity decreases rapidly.

Therefore, different figure-of-merit (FoM) definitions can be applied to WuRX architectures depending on which type of noise dominates the system. It is important to note that the relationship between BW_{BB} and BW_{RF} largely determines the dominant noise source. Therefore, by normalizing both bandwidth and sensitivity, $P_{SEN,NORM}$ can be derived:

$$P_{SEN,NORM,1} = -P_{SEN} + 5 \log BW_{BB} \tag{36}$$

$$P_{SEN,NORM,2} = -P_{SEN} + 10 \log BW_{BB} \tag{37}$$

By substituting (36) and (37) into (34), a FoM that jointly accounts for data rate, power consumption and sensitivity can be derived as

$$FoM_1 = -P_{SEN} - 10 \log \frac{P_{dc}}{1mW} + 5 \log BW_{BB} \tag{38}$$

$$FoM_2 = -P_{SEN} - 10 \log \frac{P_{dc}}{1mW} + 10 \log BW_{BB} \tag{39}$$

Considering that most WuRX designs incorporate an ADC and/or digital correlator, and that sensitivity is typically defined as the input power required to achieve a 0.1% MDR (or BER), it is sometimes more appropriate to use latency as a substitute for BW_{BB} in the FoM calculation.

$$FoM_{L1} = -P_{SEN} - 10 \log \frac{P_{dc}}{1mW} - 5 \log(Latency) \tag{40}$$

$$FoM_{L2} = -P_{SEN} - 10 \log \frac{P_{dc}}{1mW} - 10 \log(Latency) \tag{41}$$

For designs where the latency is not explicitly reported, it can be estimated using the following expression:

$$Latency = \frac{Bit_{code}}{BW_{BB}} \tag{42}$$

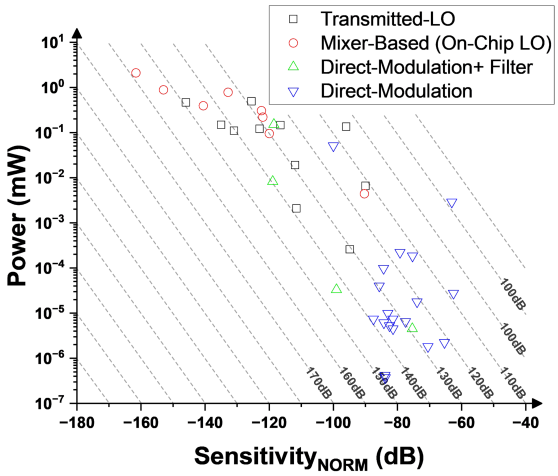
where Bit_{code} denotes the number of bit-code used in the digital correlator. It should be noted that the result of (42) represents only a lower bound on the actual latency. In some practical implementations, the latency can be significantly higher. For example, when Manchester encoding is used, the effective data bandwidth is halved, which correspondingly increases the latency.

Following and simplifying the classification proposed in [4], WuRX architectures can be grouped based on the presence of mixers, active gain, and filtering strategies, each with distinct noise dominance and sensitivity scaling:

1. RF envelope detection (ED-first with passive gain and LNA-ED-first): Both of these architectures lack RF filtering, making the impact of noise self-mixing significantly greater than that of signal-noise mixing [13,29,30,41]. In the ED-first architecture, the gain before the ED is provided solely by the passive matching network, which means that baseband noise also limits the achievable sensitivity. Although LNA-ED-first architectures are typically not limited by baseband noise due to the presence of active RF gain, it is important to note that both baseband noise and noise self-mixing scale linearly with $\sqrt{BW_{BB}}$. Therefore, both architectures are applicable to the model described in (38) and (40).
2. RF envelope detection with filtering (e.g., MEMS): Adding a high-Q MEMS filter allows pre-ED filtering to be narrow enough that convolution (signal-noise mixing) noise dominates, making sensitivity scale with BW_{BB} instead [28,32,46,55]. This architecture is applicable to the model described in (39) and (41).
3. On-chip LO (heterodyne, zero IF, or uncertain IF, with narrow BW_{RF}): Mixers provide strong pre-ED gain and filtering, resulting in convolution noise dominance. Sensitivity in these systems is proportional to BW_{BB} [7,10,34]. This architecture is applicable to the model described in (39) and (41).
4. On-chip LO (uncertain IF with large BW_{RF}): In uncertain-IF architectures with wide pre-ED bandwidths, noise self-mixing dominates, and sensitivity scales with $\sqrt{BW_{BB}}$. This architecture is applicable to the model described in (38) and (40).
5. Transmitted-LO: Since transmitted-LO architectures typically employ two EDs, the multiple stages of nonlinear demodulation make the overall noise behavior quite complex. In most WuRX implementations of transmitted-LO architectures [17,22,36], each frequency conversion stage introduces a small change in bandwidth. Therefore, the BW_{RF} is not significantly larger than the $IFBW_{IF}$, and BW_{IF} is likewise not significantly larger than BW_{BB}. Under these conditions, signal-noise mixing dominates in both conversion stages, making (39) and (41) applicable. However, there are a few cases where (38) and (40) are more appropriate. For example, when the two-tone spacing is small, the IF bandwidth becomes very narrow and close to DC. In certain extreme scenarios, such as when both ED stages are dominated by noise self-mixing or when the overall system noise is determined primarily by the baseband noise of the second ED stage, the coefficient may even need to be set to 2.5.

Figure 32 presents the survey between power consumption and normalized sensitivity, along with the corresponding normalized FoM defined in (38), (41). The plotted data summarizes representative WuRX architectures from recent literature. It can be observed that most reported designs achieve a normalized FoM in the range of 130–140 dB. The on-chip LO (mixer-based) architectures are typically located in the upper-left region of the plot. These designs offer strong sensitivity but often consume hundreds of microwatt-level power. Some works have adopted uncertain-IF architectures by removing the PLL and retaining only the VCO, thereby reducing power at the cost of some sensitivity degradation. In addition, certain designs discard the ED entirely, relying instead on traditional architectures that support a wider range of modulation schemes. These appear at the very

top-left of the plot, with power consumption approaching 1 mW, making them unsuitable for highly energy-constrained applications. On the opposite end, RF envelope detection architectures occupy the lower-right region. These achieve the lowest power consumption, usually below 100 nW, at the cost of relatively poor normalized sensitivity. Such designs typically rely on simple envelope detection and omit frequency-selective filtering or active gain stages. Techniques such as super-cutoff biasing or operation at higher frequencies can further reduce power, though at the expense of sensitivity. Conversely, integrating an LNA or RF filtering can improve performance, albeit with increased power consumption. This category has attracted the most research interest in recent years due to its ultra-low-power potential. Transmitted-LO architectures strike a good balance between power consumption and sensitivity. They also offer a certain degree of compatibility with existing communication protocols and provide inherent suppression of RF noise. However, their overall system architecture is relatively complex, making them one of the current hotspots in WuRX research.



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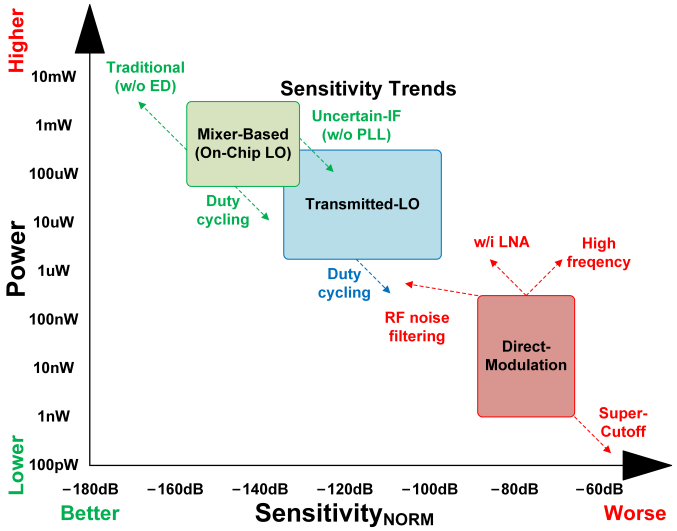


(**b**)

Figure 32. (**a**) Power versus normalized sensitivity with normalized FoM. (**b**) Sensitivity trends across different architectures.

Another key factor influencing WuRX performance is the choice of RF carrier frequency. Figure 33 shows the relationship between the reported FoM and carrier frequency across previously published WuRX designs. For RF envelope detection architectures, a clear downward trend in FoM with increasing frequency can be observed. This is largely attributed to the degradation of passive gain at higher frequencies [12,51,56]. For the other two categories, the number of reported designs is limited, and most operate within narrow frequency ranges—primarily within the ISM and 2.4 GHz bands. Although FoM also tends to decrease with increasing frequency, the variation is relatively small.

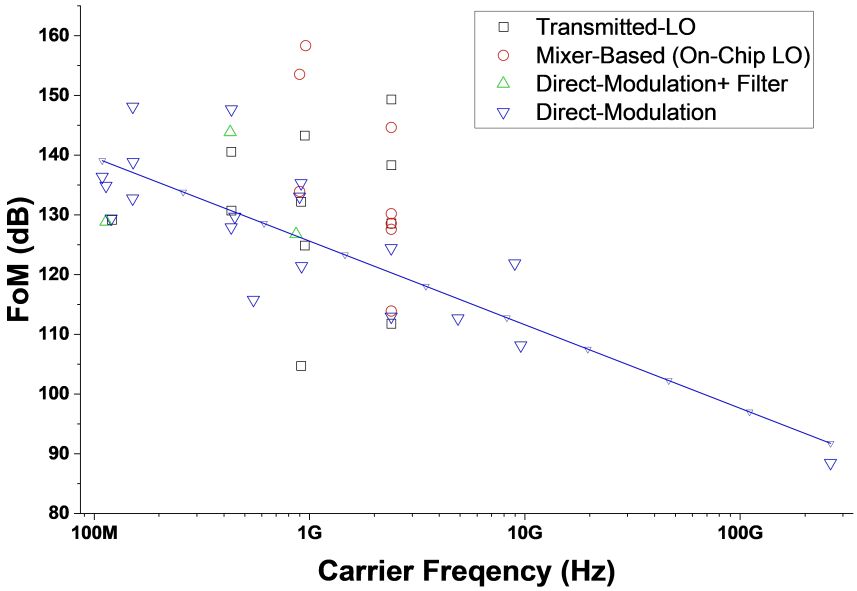


Figure 33. FoM versus carrier frequency.

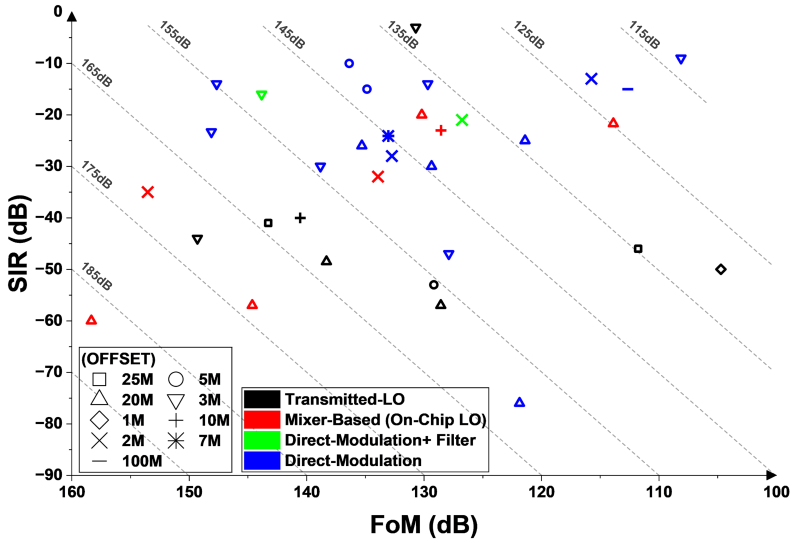
With the continued advancement of WuRX technology, interference robustness, quantified by the signal-to-interference ratio (SIR), has become an increasingly important design consideration. However, there is currently no standardized method for incorporating SIR into a unified FoM. This is primarily because definitions of interference vary across different communication protocols, and most WuRX architectures do not adhere to a common standard. Moreover, the widespread use of EDs in WuRXs, due to their simplicity and ultra-low-power operation, introduces additional complexity in interference analysis. The non-linear characteristics of EDs make it challenging to model how out-of-band or in-band interferers propagate through the front end.

Inspired by the methodology in [26], this work proposes an exploratory FoM formulation that explicitly considers SIR. As shown in (3), the behavior of an interferer passing through the ED is analogous to that of a desired signal—both undergo self-mixing. Under ideal conditions, a 1 dB increase in the input interference power results in a 2 dB increase at the ED output due to the squaring effect. Based on this principle, we propose the following expression:

$$FoM_{SIR} = FoM - \frac{SIR}{2} \tag{43}$$

Figure 34 presents the SIR versus FoM, along with the normalized FoM_{SIR} in (43). For the 2.4 GHz band, a 20 MHz offset defined by common communication protocols is typically used as the standard for interference separation. In contrast, for the sub-GHz ISM band, a 3 MHz offset is more commonly adopted. Among the various designs, on-chip LO architectures achieve the best SIR performance, primarily due to the ability to implement high-quality filtering at the IF or baseband. Although uncertain-IF architectures typically use wideband matching, they can still achieve good selectivity through frequency down-

conversion and baseband filtering. As a result, they generally exhibit better interference rejection compared to RF envelope detection architectures. RF envelope detection architectures lack frequency selectivity and RF filtering. When an LNA is included, applying high gain prior to interference filtering deteriorates SIR due saturation of interferers. A straightforward way to enhance the SIR of ED-first and LNA-ED-first designs is to incorporate a high-Q input matching network or an off-chip MEMS filter. Both approaches improve selectivity but they typically require external components, increasing cost and form factor. Transmitted-LO architectures offer a middle ground, achieving effective interference suppression through the controlled interaction between the received signal and the transmitted local oscillator, which inherently performs filtering in the frequency domain.



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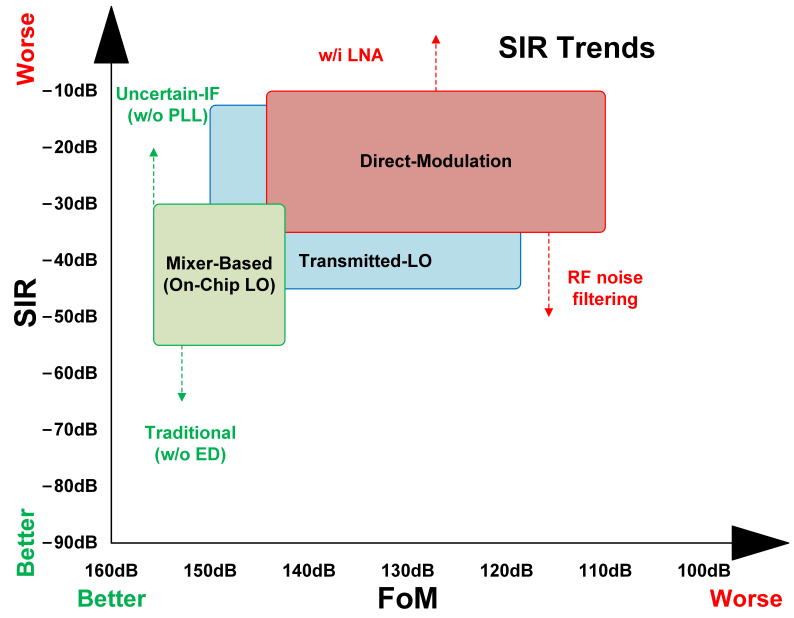
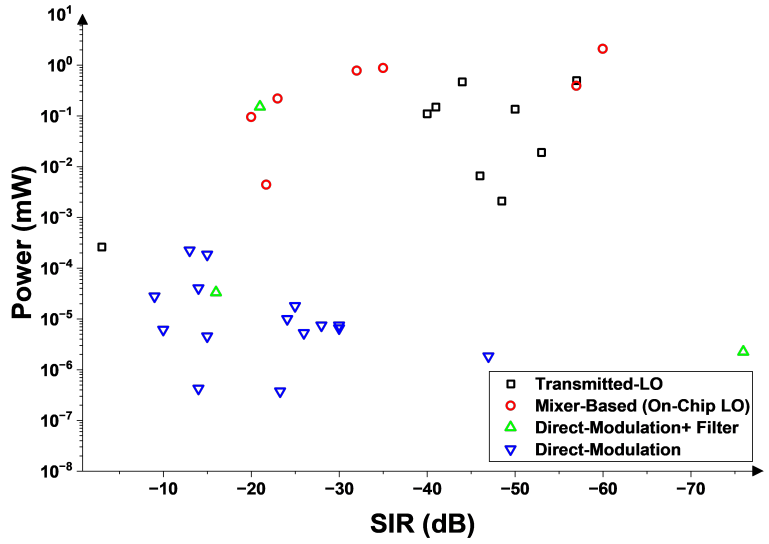


(**b**)

Figure 34. (**a**) SIR versus normalized FoM. (**b**) SIR trends across different architectures.

Figure 35 highlights the trade-off between SIR and power consumption across different WuRX architectures. Direct-modulation designs generally achieve the lowest power, often

in the nanowatt range, but suffer from limited SIR performance, typically worse than −30 dB. The addition of an LNA not only increases power dissipation but can also degrade the SIR. On-chip LO architectures occupy an intermediate position, consuming higher power in the microwatt to milliwatt range but achieving significantly better interference rejection. Transmitted-LO architectures eliminate the need for an on-chip LO and can thus achieve superior SIR at comparable power levels, while requiring higher complexity and power consumption on the transmitter side. Overall, the figure highlights that achieving strong interference rejection typically requires higher power budgets, and that different architectural choices reflect distinct compromises between robustness and energy efficiency.



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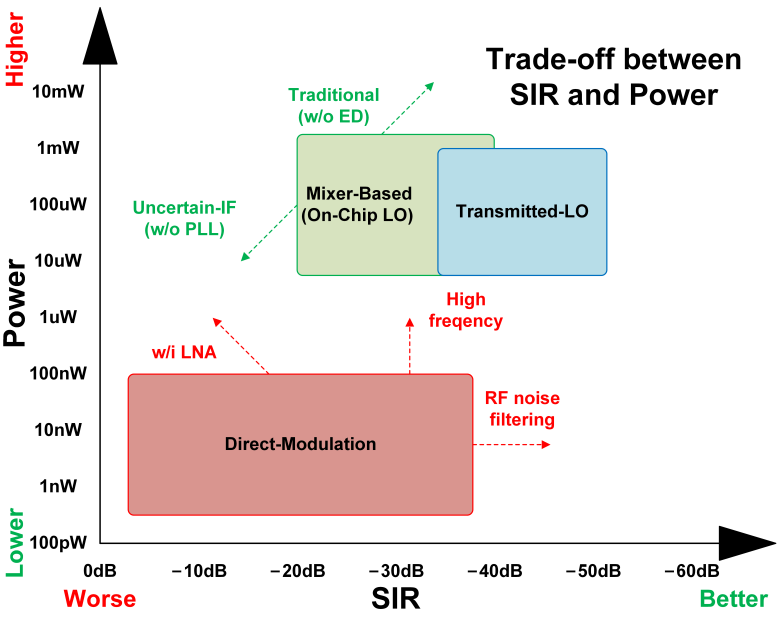

(**b**)

Figure 35. (**a**) Power versus SIR. (**b**) Trade-off between SIR and power.

10. Conclusions

WuRXs have become a key enabling technology for ultra-low-power wireless systems, offering always-on listening capabilities with minimal energy cost. They are essential for

battery-less operation, large-scale sensor deployments, and energy-efficient connectivity in IoTs and WSNs era.

Despite notable progress, WuRX design still involves fundamental trade-offs across multiple performance metrics like sensitivity, latency and power. Achieving sub-µW power consumption while maintaining high sensitivity, low latency, and strong interference rejection remains challenging, especially when aiming for compatibility with standard wireless protocols. Architectural choices such as the inclusion of LNA, LO, PLL or duty-cycle must be carefully balanced against system complexity, power, and robustness. Recent developments have addressed many of these issues through circuit and system-level innovations.

Looking forward, future WuRX research is expected to focus on tighter integration with mainstream communication standards such as BLE and Wi-Fi, improved filtering and interference suppression in congested bands, and the development of ultra-low-power, temperature-stable clock generators [14]. In addition, further co-design of antennas, matching networks, and RF front ends will help minimize external component dependence and enhance performance at the system level. These innovations will be crucial for pushing WuRX technology from research prototypes into widespread commercial adoption.

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